2N7002FN3

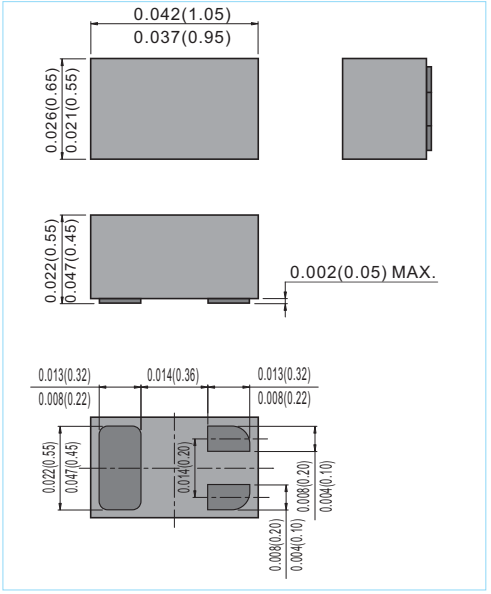
60V N-CHANNEL ENHANCEMENT MODE MOSFET

FEATURES

- $R_{DS(ON)}$, V_{GS}@10V,I_{DS}@500mA=5Ω
- $R_{DS(ON)}$, V_{GS}@4.5V,I_{DS}@50mA=7.5Ω

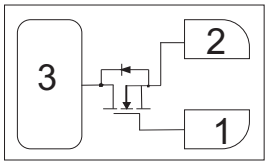
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers : Relays, Displays, Lamps, Solenoids, Memories, etc.
- In compliance with EU RoHS 2002/95/EC directives

DFN 3L — Unit : inch(mm)



MECHANICAL DATA

- Case: DFN 3L, Plastic
- Terminals: Solderable per MIL-STD-750, Method 2026
- Marking: AH



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V_{DS}	60	V
Gats-Source Voltage	V_{GS}	±20	V
Continous Drain Current	I_D	115	mA
Pulsed Drain Current [1]	I_{DM}	800	mA
Maximum Power Dissipation	P_D	150	mW
Junction-to Ambient Thermal Resistance (PCB mounted)[2]	$R_{\theta JA}$	883	°C/W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 to +150	°C

Note 1 : Maximum DC current limited by the package

2 : Surface mounted on FR4 board,t<10 sec

PAN JIT RESERVES THE RIGHT TO IMPROVE PRODUCT DSEIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE

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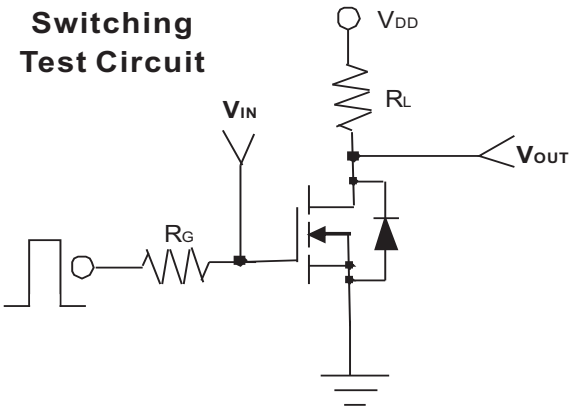
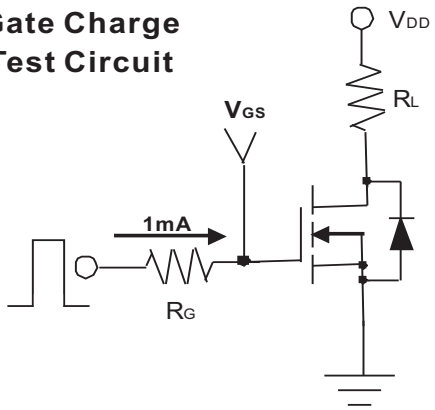
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=10mA	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250mA	1	-	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=50mA	-	-	7.5	W
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=500mA	-	-	5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	mA
Gate Body Leakage	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Forward Transconductance	g_{FS}	V_{DS}=15V, I_D=250mA	100	-	-	mS
Dynamic						
Total Gate Charge	Q_G	V_{DS}=15V, I_D=500mA, V_{GS}=4.5V	-	0.6	0.7	nC
Gate-Source Charge	Q_{GS}		-	0.1	-	
Gate-Drain Charge	Q_{GD}		-	0.08	-	
Turn-On Delay Time	t_{ON}	V_{DD}=10V,R_L=20W I_D=500mA,V_{GEN}=10V,R_G=10W	-	9	15	ns
Turn-Off Delay Time	t_{OFF}		-	21	26	
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	-	50	pF
Output Capacitance	C_{OSS}		-	-	25	
Reverse Transfer Capacitance	C_{RSS}		-	-	5	
Source-Drain Diode						
Max.Diode Forward Current	I_S	-	-	-	115	mA
Diode Foreard Voltage	V_{SD}	I_S=250mA,V_{GS}=0V	-	0.93	1.2	

Switching Test Circuit



Gate Charge Test Circuit



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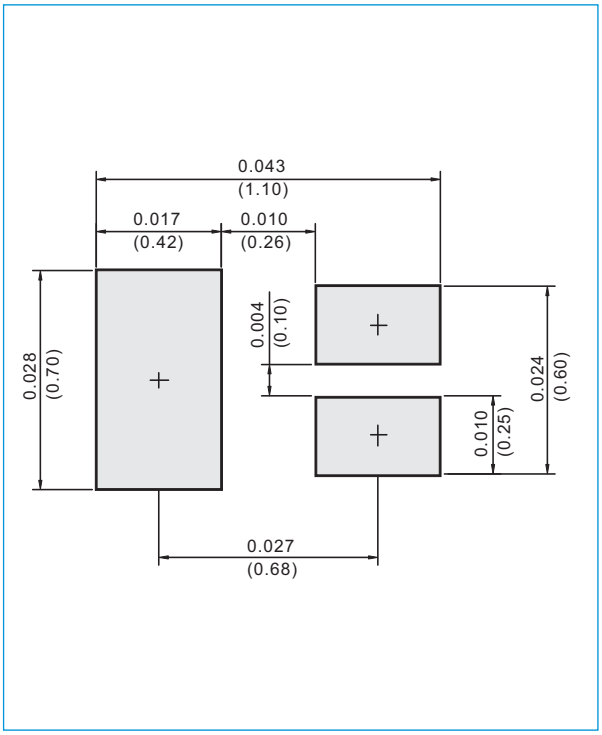
MOUNTING PAD LAYOUT

DFN 3L | Unit: inch (mm)



ORDER INFORMATION

- Packing information

  T/R - 8K per 7" plastic Reel

LEGAL STATEMENT