SP5669

2.7GHz I²C Bus Controlled Synthesiser

Preliminary Information

DS4852 ISSUE 2.1 May 1999

Features

- Complete 2.7GHz single chip system
- Compatible with UK DTT offset requirements
- Optimised for low phase noise
- Selectable divide by two prescaler
- Selectable reference division ratio
- Selectable reference/comparison frequency output
- Selectable charge pump current
- Four selectable I²C bus address
- 5–level ADC
- Pin compatible with the SP5658 3–wire bus controlled synthesiser and SP5659 I²C bus synthesiser and SP5659 I²C bus synthesiser ESD protection; (Normal ESD handling procedures should be observed)

Applications

- Complete 2.7GHz single chip system
- Optimised for low phase noise

Description

The SP5669 is a single chip frequency synthesiser designed for tuning systems up to 2.7GHz and offers step size compatible with DTT offset requirements.

The RF preamplifier drives a divide by two prescaler which can be disabled for applications up to 2GHz, allowing direct interfacing with the programmable divider so enabling a step size equal to the comparison frequency. For applications up to 2.7GHz the divide by two is enabled, giving a step size of twice the comparison frequency.

Ordering Information

SP5669/KG/MP1S (Tubes)
SP5669/KG/MP1T (Tape and reel)

The comparison frequency is obtained either from an on–chip crystal controlled oscillator, or from an external source. The oscillator frequency F_{ref} or the comparison frequency F_{comp} may be switched to the REF/COMP output. This feature is ideally suited to providing the reference frequency for a second synthesiser such as in a double conversion tuner (see Fig. 8).

The synthesiser is controlled via an I²C bus, and responds to one of four programmable addresses which are selected by applying a specific voltage to the ‘address’ input. This feature enables two or more synthesisers to be used in a system.

The device contains four switching ports P0–P3 and a 5–level ADC. The output of the ADC can be read via the I²C bus.

The device also contains a varactor line disable and chargepump disable facility.

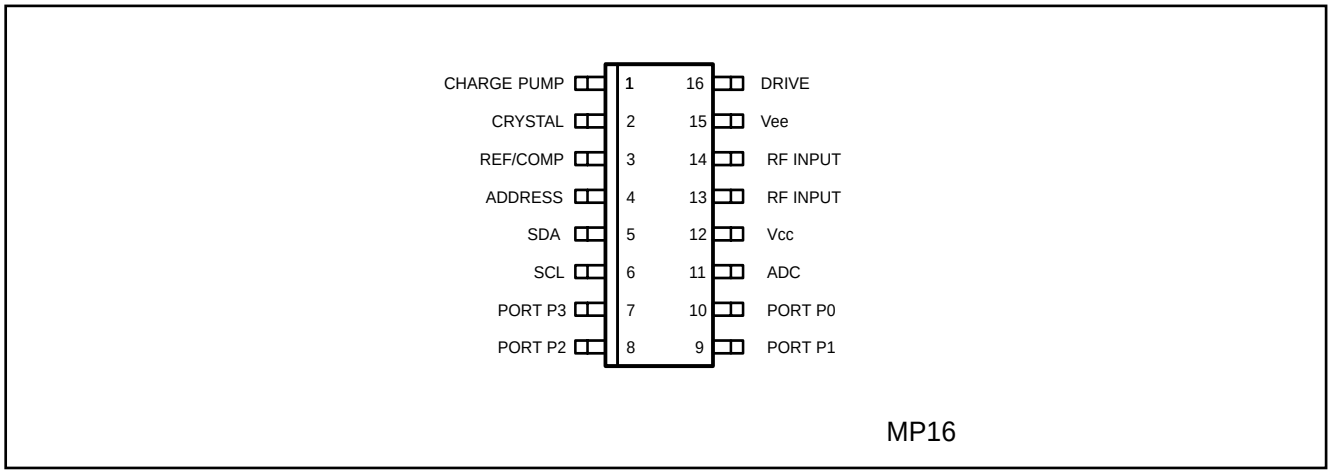


Figure 1 - Pin connections - top view

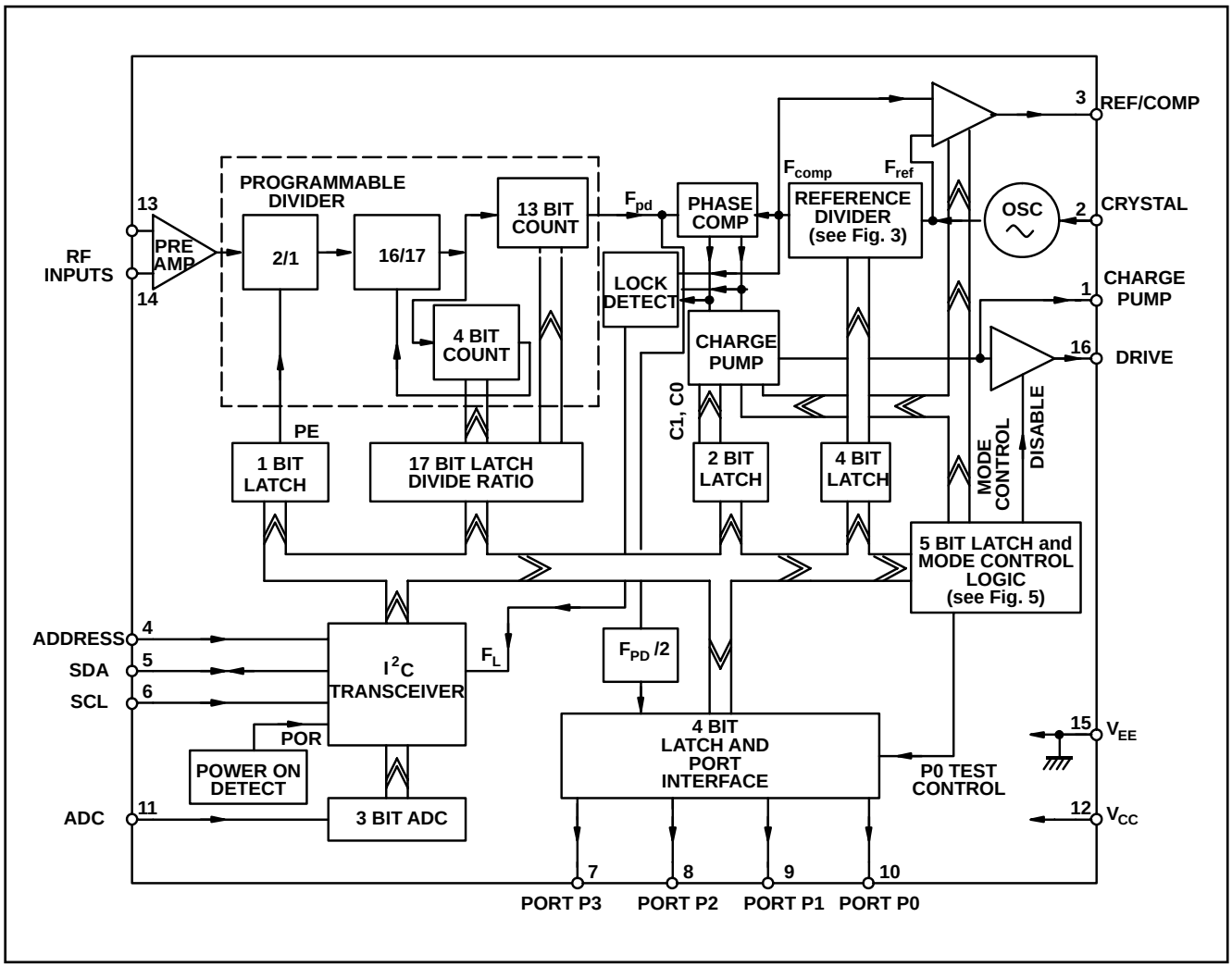


Figure 2 - Block diagram

Electrical Characteristics

T amb = –20°C to +80°C, V_{CC} = +4.5V to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current, I_{CC}	12		68	85	mA	V_{CC} = 5V prescaler enabled, PE = 1
			58	73	mA	V_{CC} = 5V prescaler disabled, PE = 0
RF input voltage	13, 14	40		300	mV rms	300MHz to 2.7GHz Prescaled enabled, PE = 1, See Fig. 7b.
13, 14100				300	mV rms	80MHz Prescaler enabled, PE=1, See Fig. 7b.
13,14 50				300	mV rms	80MHz to 2.0GHz Prescaler disabled, PE = 0, See Fig. 7a.
RF input impedance	13, 14		50		Ω	Refer to Fig. 13
RF input capacitance	13, 14		2		pF	Refer to Fig. 13
SDA, SCL	5, 6					
Input High voltage		3		5.5	V	
Input Low voltage		0		1.5	V	
Input High current				10	µA	Input voltage = V_{CC}
Input Low Current				–10	µA	Input voltage = V_{EE}
LeakageCurrent				10	µA	V_{CC} = V_{EE}
Input hysteresis			0.8		V	
SDA Output voltage	5			0.4	V	I sink = 3mA
Charge pump output current	1					See Fig. 6, V pin = 2V
Charge pump output leakage	1		± 3	± 10	nA	V pin1 = 2V
Charge pump drive output current		16	1			mAV pin16 = 0.7V
Drive output saturation voltage when disabled	16			350	mV	
External reference input frequency		2	2		20	MHzAC coupled sinewave
External reference input ampltude		2	200		500	mV p–pAC coupled sinewave
Crystal frequency	2	4		16	MHz	
Crystal oscillator drive level	2		35		mV p–p	
Recommended crystal series resistance		10		200	Ω	Applies to 4MHz crystal only. 'Parallel resonant' crystal. Figure quoted is under all conditions including start up.
Crystal oscillator negative resistance		2	400		Ω	Includes temperature and process tolerances.
REF/COMP output Voltage	3		350		mV p–p	AC coupled output. Output enabled,RE=1. See Note 1.

Electrical Chacteristics (cont.)

T amb = –20°C to 80 °C, V_{CC} =+ 4.5V to + 5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Comparison frequency				2	MHz	
Equivalent phase noise at phase detector			–148		dBC/Hz	6kHz loop BW, phase comparator freq 250kHz. Figure measured @ 1kHz offset, SSB (within loop band width).
RF division ratio	240		131071			Prescaler disabled, PE = 0
	480		262142			Prescaler enabled, PE = 1
Reference division ratio						See Fig. 3
Output ports P0, P1, P2, P3	7,8,9, 10					
Sink current			10		mA	V port = 0.7V
Leakage current				10	µA	V port = 13.2V
ADC input voltage	11					See Table 4, Fig 4
ADC input current	11			±10	µA	$V_{CC} \geq V$ input $\geq V_{EE}$
Address input current High	4			1	mA	Input voltage =V_{CC}
Address input current Low	4			–0.5	mA	Input voltage =V_{EE}

Note 1: If the REF/COMP output is not used, the output should be left open circuit or connected to V_{CC} , and disabled by setting RE=0.

Absolute Maximum Ratings

All voltages are referred to V_{EE} at 0V.

Characteristics	Pin	Value		Units	Conditions
		Min	Max		
Supply Voltage, V_{CC}	12	0.3	7	V	
RF input voltage	13,14		2.5	V p–p	AC coupled as per application
RF input DC offset	13,14	–0.3	V_{CC} +0.3	V	
Port voltage	7–10	–0.3	14	V	Port in off state
	7–10	–0.3	6	V	Port in on state
Total port current	7–10		50	mA	
ADC input DC offset	11	–0.3	V_{CC} +0.3	V	
REF/COMP output DC offset	3	–0.3	V_{CC} +0.3	V	
Charge pump DC offset	1	–0.3	V_{CC} +0.3	V	
Drive DC offset	16	–0.3	V_{CC} +0.3	V	
Crystal oscillator DC offset	2	–0.3	V_{CC} +0.3	V	
Address DC offset	4	–0.3	V_{CC} +0.3	V	
SDA and SCL DC offset	5, 6	–0.3	6V	V	
Storage temperature		–55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance					
chip to ambient			111	°C/W	
chip to case			41	°C/W	
Power consumption at V CC =5.5V			468	mW	All ports off, prescaler enabled
ESD protection	All	4		kV	Mil Std 883 TM 3015

Functional Description

The SP5669 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. The block diagram is shown in Fig. 2.

The RF input signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces with the 17–bit fully programmable divider via a divide–by–two prescaler. For applications up to 2GHz RF input, the prescaler may be disabled so eliminating the degradation in phase noise due to prescaler action. The divider is of MN+A architecture, where the dual modulus prescaler is 16/17, the A counter is 4–bits, and the M counter is 13–bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on–board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 15 ratios as detailed in Fig. 3.

The output of the phase detector feeds a charge pump and loop amplifier section, which when used with an external voltage transistor and loop filter, integrates the current pulses into the varactor line voltage. By invoking the device test modes as described in Fig. 5, the varactor drive output can be disabled so switching the external transistor 'off' and allowing an external voltage to be written to the varactor line for tuner alignment purposes. Similarly, the charge pump may be also disabled to a high impedance state.

The programmable divider output Fpd/2 can be switched to port P0 by programming the device into test mode. The test modes are described in Fig. 5 high

Programming

The SP5669 is controlled by an I^2C data bus. Data and Clock are fed in on the SDA and SCL lines respectively as defined by I^2C bus format. The synthesiser can either accept data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. Tables 1 and 2 in Fig. 4 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C bus system. Table 3 in Fig.4 shows how the address is selected by applying a voltage to the 'address' input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

Write Mode

With reference to Table 1, bytes 2 and 3 contain frequency information bits 2 14 –2 0 inclusive. Auxillary frequency bits 2 16 –2 15 are in byte 4. For most frequencies only bytes 2 and 3 will be required. The remainder of byte 4 and byte 5 control the prescaler enable, reference divider ratio (see Fig. 3), charge pump, REF/COMP output (see Fig. 5), output ports and test modes (see Fig. 5).

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or 4, a logic '0' indicating byte 2 and a logic '1' indicating byte 4. Having interpreted this byte as either byte 2 or 4 the following data byte will be interpreted as byte 3 or 5 respectively. Having received two complete data bytes, additional data bytes can be entered, where byte interpretation follows the same procedure, without readdressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous data is retained.

To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 17 bits of frequency data have been received, or after the generation of a STOP condition. Repeatedly sending bytes 2 and 3 only will not change the frequency. A frequency change occurs when one of the following data sequences is sent to an addressed device;

Bytes 2, 3, 4, 5
Bytes 4, 5, 2, 3

or when a STOP condition follows valid data bytes as follows;

Bytes 2, 3, 4, STOP
Bytes 4, 5, 2 STOP
Bytes 2, 3, STOP
Bytes 2, STOP
Bytes 4, STOP

It should be noted that the device must be initially addressed with both frequency AND control byte data, since the control byte contains reference divider information which must be provided before a chosen frequency can be synthesised. This implies that after initial turn on, bytes 2, 3, 4 must be sent followed by a STOP condition as a minimum requirement. Alternatively bytes 2, 3, 4, 5 must be sent if port information is also required.

Read Mode

When the device is in read mode, the status byte read fromthe device takes the form shown in Table 2, Fig. 4.

Bit 1 (POR) is the power–on reset indicator, and this is set to a logic '1' if the V_{CC} supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked.

Bits 6,7 and 8 (A2, A1, A0) combine to give the output of the ADC. The ADC can be used to feed AFC information to the microprocessor via the I^2C bus.

Additional Programmable Features

Prescaler enable

The divide by two prescaler is enabled by setting bit PE within byte 4 to a logic '1'. A logic '0' disables the prescaler, directly passing the RF input frequency to the 17–bit programmable counter. Bit PE is a static select only.

Charge pump current

The charge pump current can be programmed by bits C1 and C0 within data byte 5, as defined in Fig. 6.

Test mode

The test modes are invoked by setting bits RE=0 and RTS=1 within the programming data, and are selected by bits TS2, TS1 and TS0 as shown in Fig. 5. When TS2, TS1 and TS0 are received, the device retains previously received P2, P1 and P0 data.

Reference/Comparison frequency output

The reference frequency F ref can be switched to the REF/COMP output, pin 3, by setting bit RE=1 and RTS=0 within byte 5. The comparison frequency F comp can be switched to the REF/COMP output, pin 3, by setting bit RE=1 and RTS=1 within byte 5. For RE set to logic '0', the output is disabled and set to a high state. RE and RTS default to logic '1' during device power up, thus enabling the comparison frequency F comp at the REF/COMP output.

R3	R2	R1	R0	Ratio	Comparison frequency with a 4MHz external reference
0	0	0	0	2	2MHz
0	0	0	1	4	1MHz
0	0	1	0	8	500kHz
0	0	1	1	16	250kHz
0	1	0	0	32	125kHz
0	1	0	1	64	62.5kHz
0	1	0	0	128	31.25kHz
0	1	1	1	256	15.625kHz
1	0	0	0	Not Allowed	-
1	0	0	1	6	666.67kHz
1	0	1	0	12	333.33kHz
1	0	1	1	24	166.67kHz
1	1	0	0	48	83.33kHz
1	1	0	1	96	41.67kHz
1	1	1	0	192	20.83kHz
1	1	1	1	384	10.42kHz

Figure 3 - Reference division ratios

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
CONTROL DATA	1	2^{16}	2^{15}	PE	R3	R2	R1	R0	A	Byte 4
CONTROL DATA	C1	C0	RE	RTS	P3	P2/TS2	P1/TS1	P0/TS0	A	Byte 5

Table 1 - Write data format (MSB is transmitted first)

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	1	A	Byte 1
STATUS BYTE	POR	FL	X	X	X	A2	A1	A0	A	Byte 2

Table 2 - Read data format (MSB is transmitted first)

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 3)
2 16 –2 0	:	Programmable division ratio control bits
PE	:	Prescaler enable
R3,R2,R1,R0	:	Reference division ratio select (see Fig. 3)
C1, C0	:	Charge pump current select (see Fig.6)
RE	:	Reference oscillator output enable
RTS	:	REF/COMP output select when RE=1 (see Fig.5)
RTS	:	Test mode enable when RE=0 (see Fig.5)
TS2, TS1, TS0	:	Test mode control bits (valid when RE=0, RTS=1, see Fig. 5)
P0	:	P0 port output state (always valid except when RE=0, RTS=1)
P3, P2, P1	:	P3, P2 and P1 port output states
POR	:	Power On Reset indicator
FL	:	Phase Lock Flag
A2, A1, A0	:	ADC data (see Table 4)
X	:	Don't care

MA1	MA0	Address input voltage level
0	0	0 – 0.1V_{CC}
0	1	Open circuit
1	0	0.4V CC – 0.6V_{CC} #
1	1	0.9V CC – V_{CC}

Programmed by connecting a 15kΩ resistor between pin 4 and V_{CC}

Table 3 - Address selection

A2	A1	A0	Voltage on ADC input
1	0	0	0.6V_{CC} toV_{CC}
0	1	1	0.45V_{CC} to 0.6V_{CC}
0	1	0	0.3V_{CC} to 0.45V_{CC}
0	0	1	0.15V_{CC} to 0.3V_{CC}
0	0	0	0 to 0.15V_{CC}

Table 4 - ADC levels

Figure 4 - Data formats

RE	RTS	TS2	TS1	TS0	REF/COMP OUTPUT MODE	Test mode description
0	0	X	X	X	Disabled to high state	Normal operation
0	1	X	0	0	Disabled to high state	Charge pump sink. Status byte FL = logic '1'
0	1	X	0	1	Disabled to high state	Charge pump source. Status byte FL = logic '0'
0	1	X	1	0	Disabled to high state	Charge pump disabled. Status byte FL=logic '0'
0	1	X	1	1	Disabled to high state	Port P0 = F pd /2
0	1	1	X	X	Disabled to high state	Varactor Drive Output disabled
1	0	X	X	X	F_{ref} switched	Normal operation
1	1	X	X	X	F_{comp} switched	Normal operation

X=don't care

Figure 5 - REF/COMP output mode and Test modes

C1 byte 5, bit 1	C0 byte 5, bit 2	Current in µA		
		min	typ	max
0	0	±90	±120	±150
0	1	±195	±260	±325
1	0	±416	±555	±694
1	1	±900	±1200	±1500

Figure 6 - Charge pump current

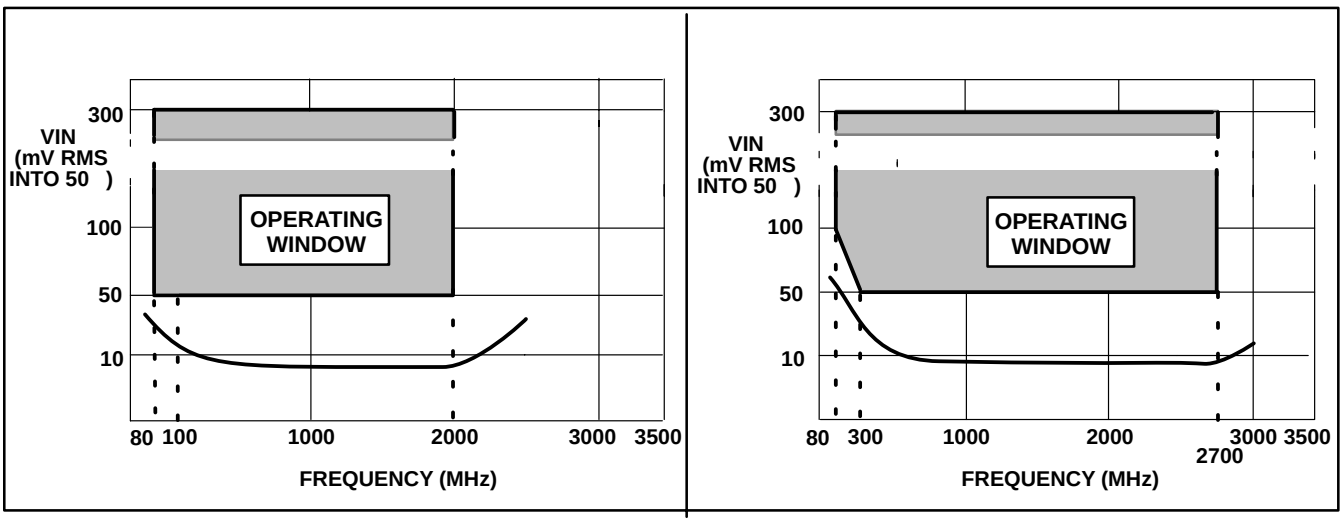


Figure 7a - Typical input sensitivity (prescaler disabled, PE=0)

Figure 7b - Typical input sensitivity (prescaler enabled, PE=1)

Double Conversion Tuner Systems

The high 2.7GHz maximum operating frequency and excellent noise characteristics of the SP5669 enables the construction of double conversion high IF tuners.

A typical system shown in Fig.8 will use the SP5669 as the first LO control for full band upconversion to an IF of greater than 1GHz.

The wide range of reference division ratios allows the SP5669 to be used both for the up converter LO with a high phase comparator frequency (hence low phase noise) and the down converter which utilises the device in a lower comparison frequency mode (which offers a fine step size).

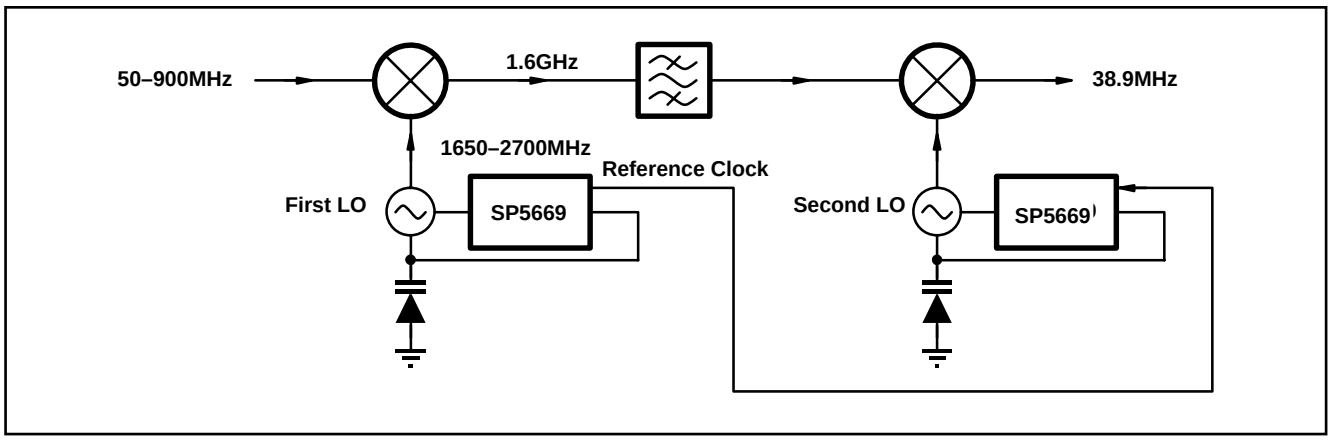


Figure 8 - Example of double conversion from VHF/UHF frequencies to TV IF

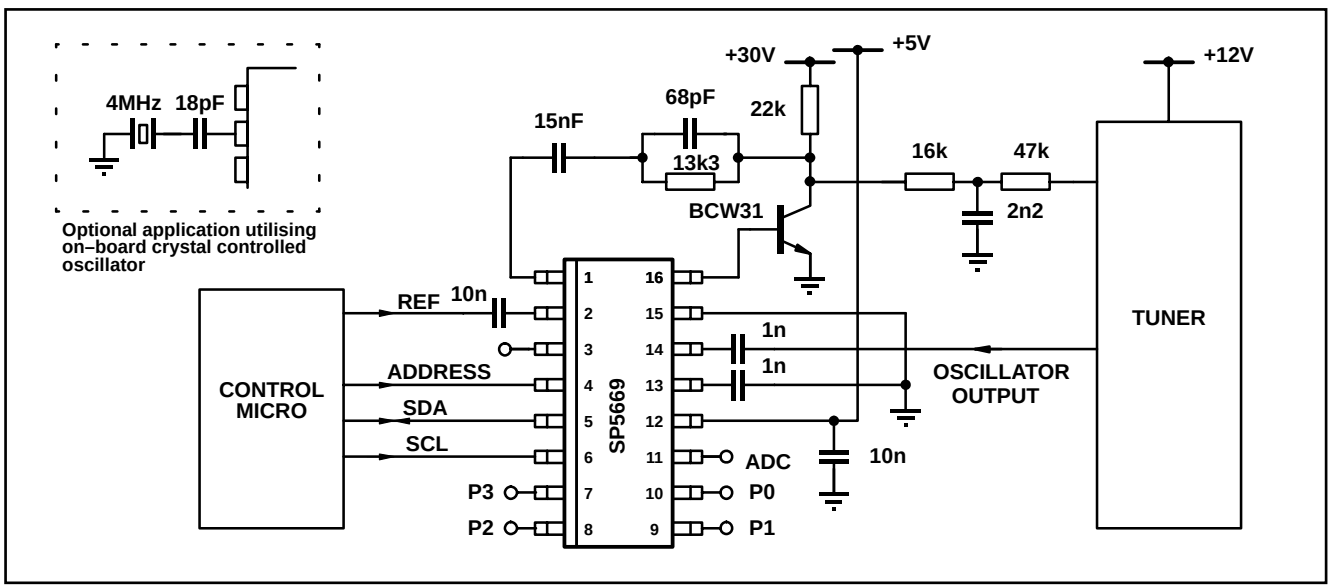


Figure 9 - Typical appliction

Application Notes

A generic set of application notes AN168 for designing with synthesisers such as the SP5659 has been written. This covers aspects such as loop filter design and decoupling. This application note is also featured in the Media Data Book, or refer to the Zarlink Semicondor Internet Site http://www.zarlink.com.

A generic test/demo board has been produced which can be used for the SP5669. A circuit diagram and list of components for the board is shown in Figs. 10 and 11.

The board can be used for the following purposes:

(A) Measuring RF sensitivity performance.
(B) Indicating port function.
(C) Synthesising a voltage controlled oscillator.
(D) Testing of external reference

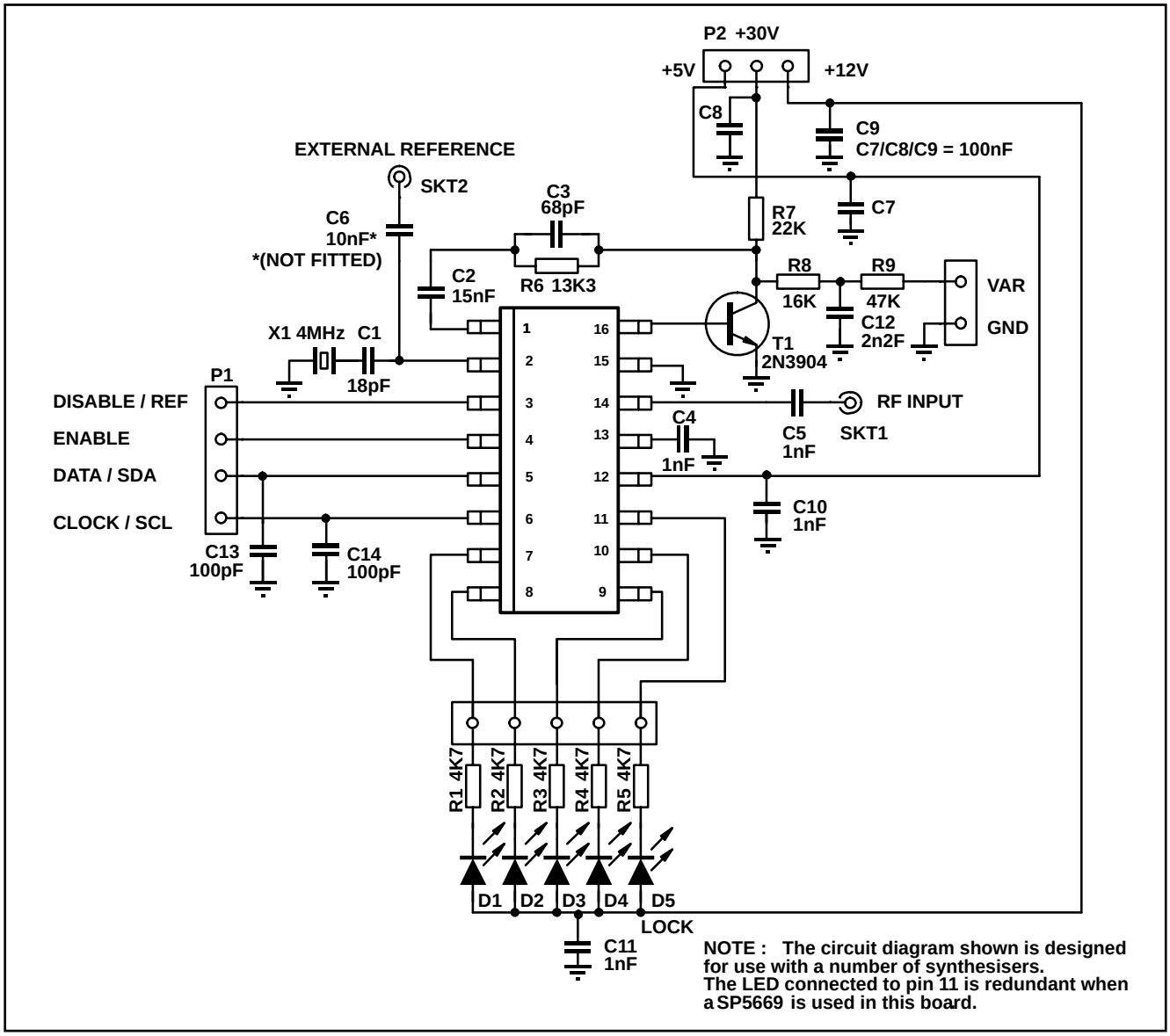


Figure 10 - Test board

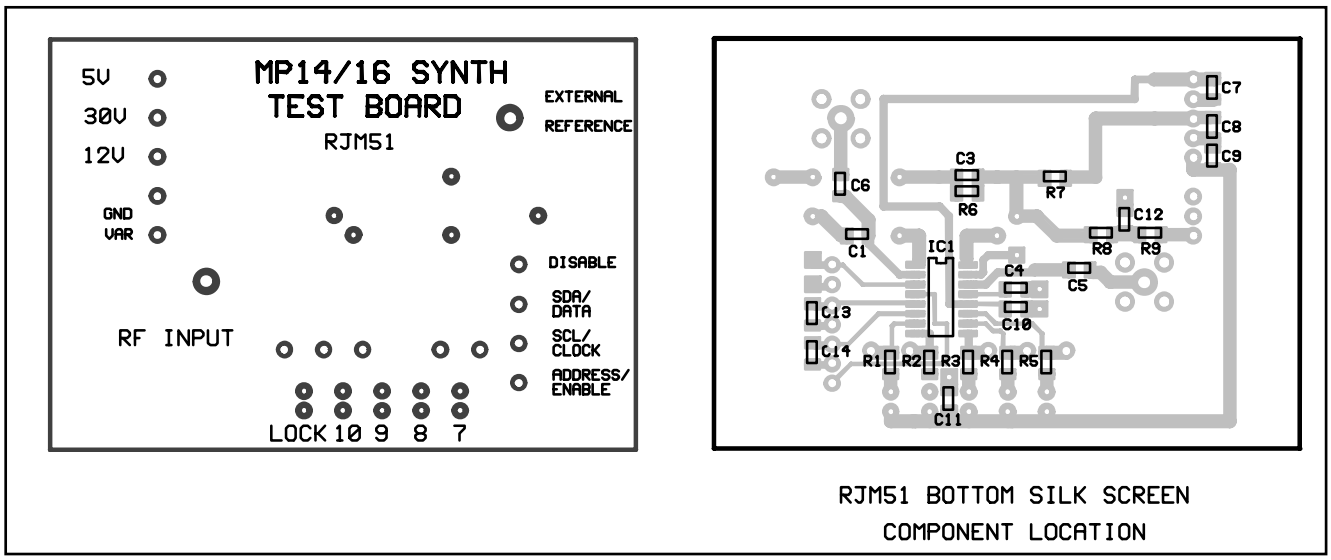


Figure 11 - Test board (layout)

Loop Bandwidth

The majority of applications for which the SP5669 is intended require a loop filter bandwidth of between 2kHz and10kHz.

Typically the VCO phase noise will be specified at both 1kHz and10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. Thus the phase noise depends on the synthesiser comparator noise floor, rather than the VCO.

The 10kHz offset figure should depend on the VCO providing the loop is designed correctly, and is not underdamped.

Reference Source

The SP5669 offers optimal LO phase noise performance when operated with a large step size. This is due to the fact that the LO phase noise within the loop bandwidth is:

$$\text{phase comparator noise floor} + 20 \log_{10} \left(\frac{\text{LO frequency}}{\text{phase comparator frequency}} \right)$$

Assuming the phase comparator noise floor is flat irrespective of sampling frequency, this means that the best performance will be achieved when the overall LO to phase comparator division ratio is a minimum.

There are two ways of achieving a higher phase comparator sampling frequency:–

A) Reduce the division ratio between the reference source and the phase comparator

B) use a higher reference source frequency.

Approach B) may be preferred for best performance since it is possible that the noise floor of the reference oscillator may degrade the phase comparator performance if the reference division ratio is very small.

Driving Two Devicesfrom A Common Reference

As mentioned earlier in the Datasheet, the SP5669 has a REF/COMP output which allows two synthesisers to be driven from a common reference. To do this, the ‘‘Master” should be programmed by setting RE = 1 and RTS = 0. The driven device should be programmed for normal operation i.e. RE = 0, and RTS = 0. The two devices should be connected as shown below.

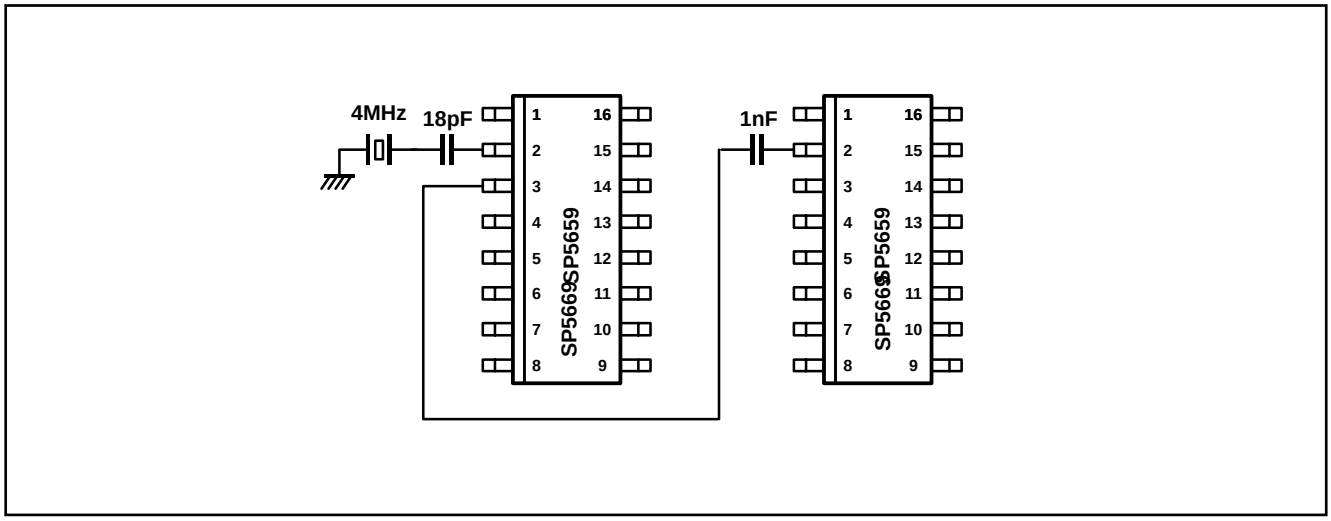


Figure 12 - Driving two devices from a common reference

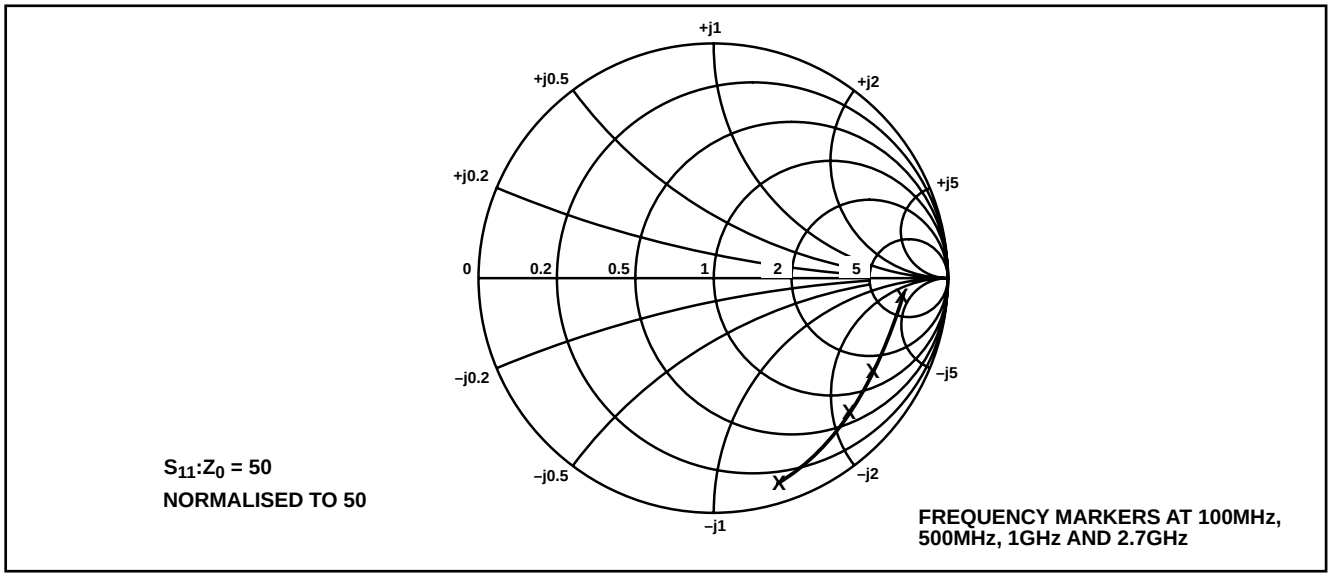


Figure 13 - typical RF input impedance

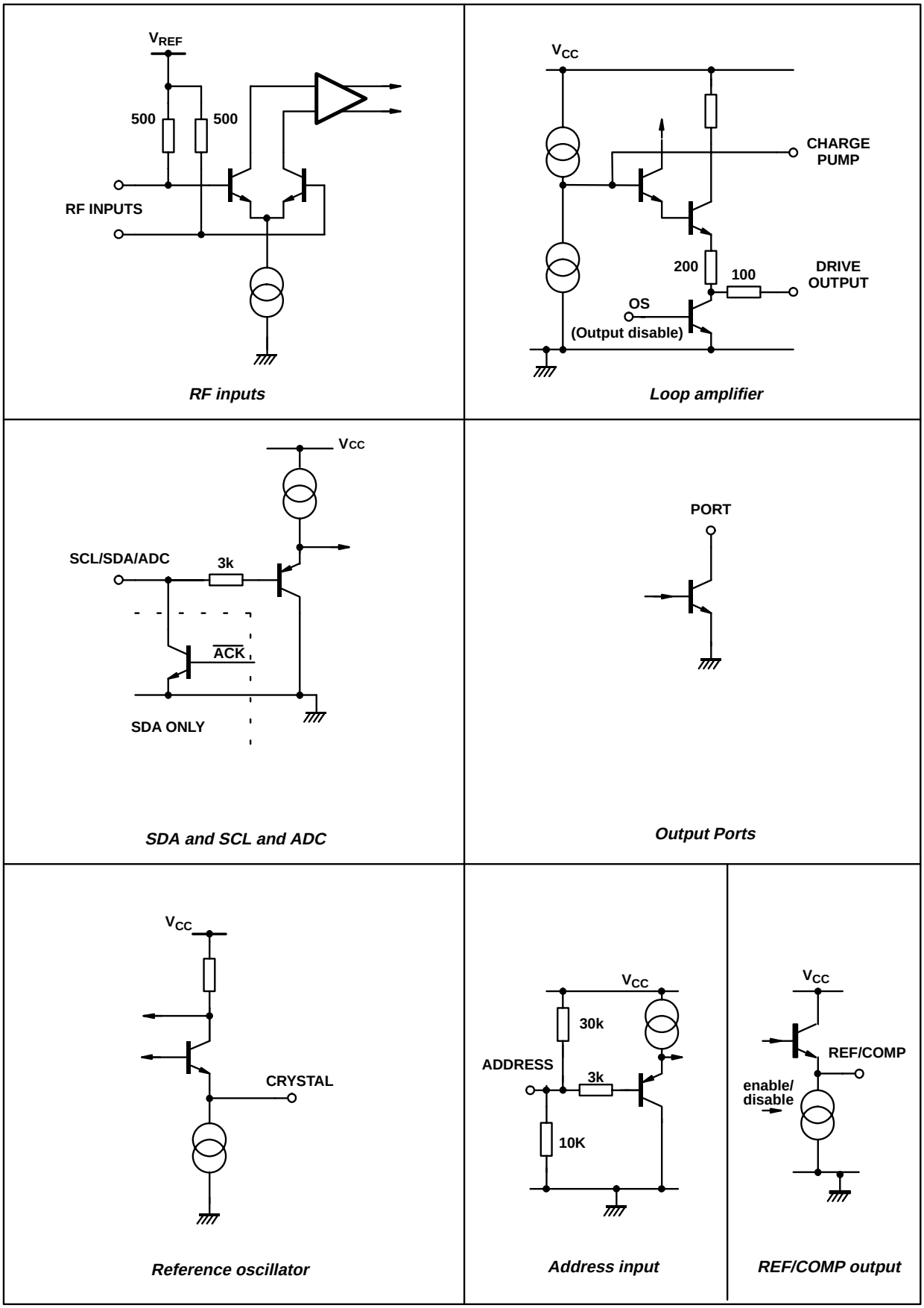
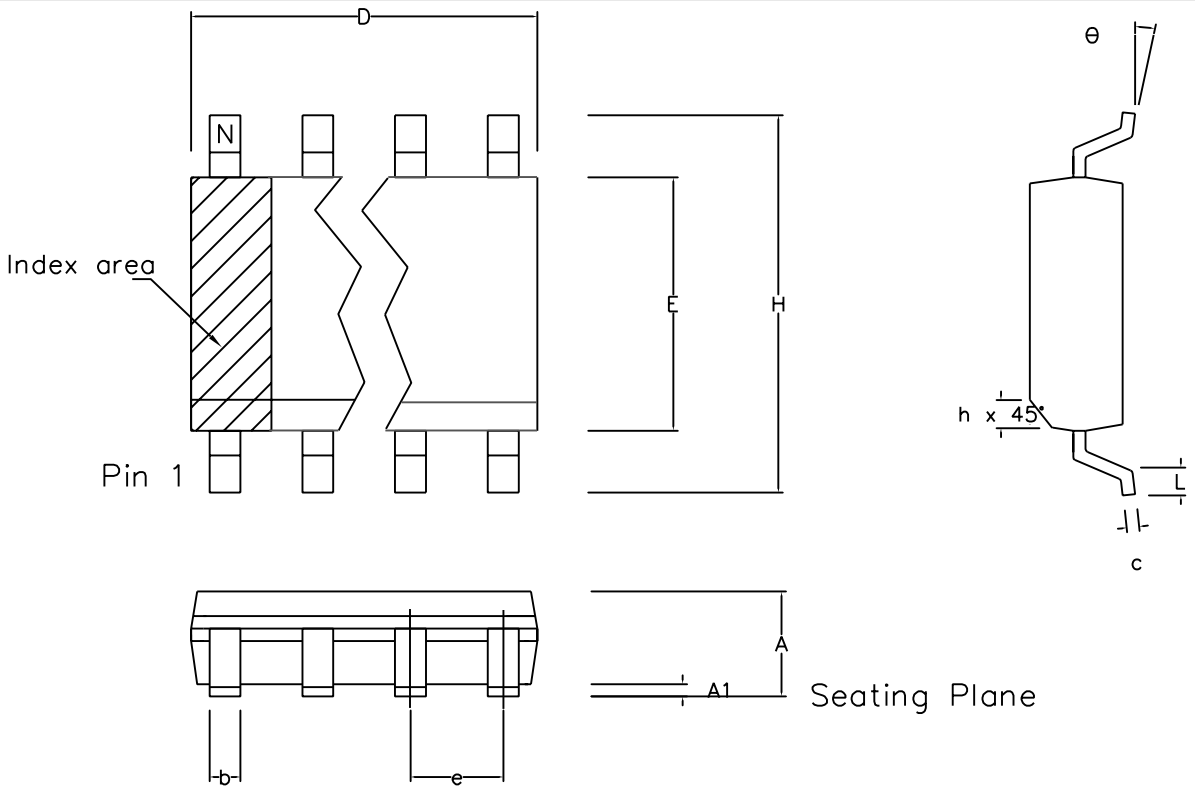


Figure 14 - Input/Output interface circuits



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201938	202597	203706	212431
DATE	7Apr95	27Feb97	12Jun97	9Dec97	25Mar02
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MP / S

Package Code DC

Package Outline for
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