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VCJ5

Description

Vectron's VCJ5 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off either 2.5 or 3.3 volt supply, in a hermetically sealed 9x15 ceramic package.

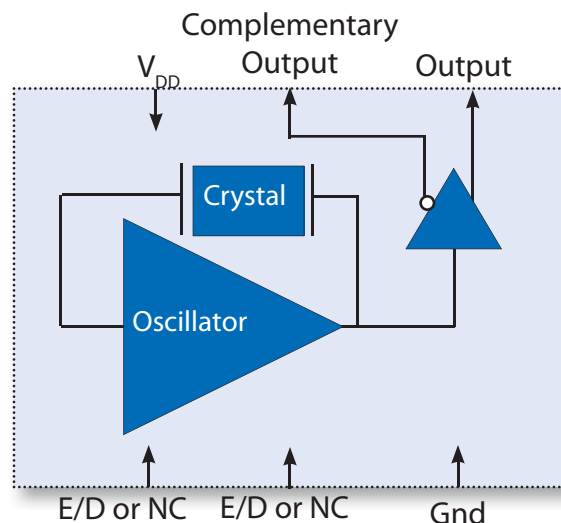
Features

- 3.3V or 2.5V Operation
- Output Frequencies to 260MHz
- <0.7 ps RMS jitter, 12k-20MHz
- Differential Output
- Enable/Disable
- -10/70°C or -40/85°C Operation
- Hermetically Sealed 9x14 Ceramic Package
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

Applications

- Storage Area Networking
- Telecom
- Ethernet, GE, SynchE
- Fiber Channel
- PON
- Driving A/D's, D/A's, FPGA's
- Test and Measurement
- Medical
- COTS

Block Diagram



Performance Specifications

Table 1. Electrical Performance, LVPECL Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V
Current (No Load)	I_{DD}		50	98	mA
Frequency					
Nominal Frequency ²	f_N	10		260	MHz
Stability ^{2,3} (Ordering Options)		±25, ±50, ±100			ppm
Outputs					
Output Logic Levels ⁴ , -10/70°C Output Logic High Output Logic Low	V_{OH} V_{OL}	$V_{DD}-1.025$ $V_{DD}-1.810$		$V_{DD}-0.880$ $V_{DD}-1.620$	V
Output Logic Levels ⁴ , -40/85°C Output Logic High Output Logic Low	V_{OH} V_{OL}	$V_{DD}-1.085$ $V_{DD}-1.830$		$V_{DD}-0.880$ $V_{DD}-1.555$	V
Output Rise and Fall Time ⁴ Rise Time Fall Time	t_R/t_F			1 1	ns ns
Load		50 ohms into $V_{DD}-1.3V$			
Duty Cycle ⁵		45	50	55	%
Jitter (12 kHz - 20 MHz BW) 155.52MHz ⁶	ϕ_J		0.3	0.7	ps
Period Jitter ⁷ RMS P/P	ϕ_J		2.7 23		ps ps
Enable/Disable					
Output Enabled ⁸ Output Disabled	V_{IH} V_{IL}	$0.7*V_{DD}$		$0.3*V_{DD}$	V V
Enable/Disable Time	t_D			200	ns
Enable/Disable Leakage Current				±200	uA
Enable Pull-Up Resistor Output Enabled Output Disabled			33 1		kOhm MOhm
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		9x14x4.5			mm

1. The VCJ5 power supply pin should be filtered, eg, a 0.1 and 0.01 uf capacitor.
2. See Standard Frequencies and Ordering Information for more information.
3. Includes calibration tolerance, operating temperature, supply voltage variations,, aging and IR reflow.
4. Figure 2 defines these parameters and Figure 1 defines the test circuit.
5. Duty Cycle is defines as the On/Time Period.
6. Measured using an Agilent E5052, 155.520MHz.
7. Measured using a LeCroy 8600, 25K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

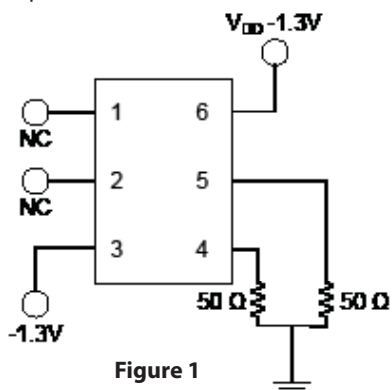


Figure 1

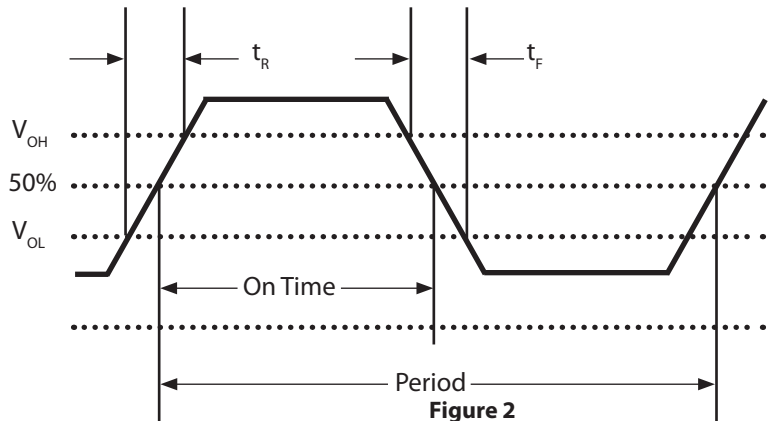


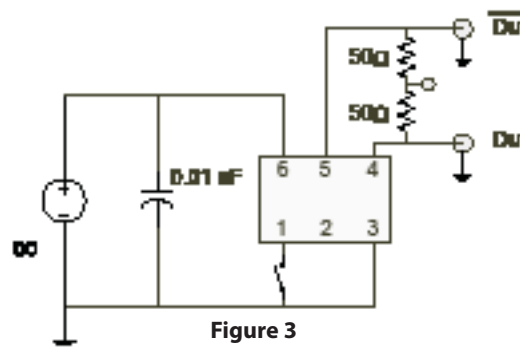
Figure 2

Performance Specifications

Table 2. Electrical Performance, LVDS Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage ¹	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V
Current (No Load)	I_{DD}			60	mA
Frequency					
Nominal Frequency ²	f_N	10		260	MHz
Stability ^{2,3} . (Ordering Options)			±25, ±50, ±100		ppm
Outputs					
Output Logic Levels ⁴ Output Logic High Output Logic Low	V_{OH} V_{OL}	0.9	1.43 1.10	1.6	V
Differential Output		247	330	454	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error				50	mV
Output Leakage Current				10	uA
Output Rise and Fall Time ⁴ Rise Time Fall Time	t_R/t_F			1 1	ns ns
Load		100 ohms differential			
Duty Cycle ⁵		45	50	55	%
Jitter (12 kHz - 20 MHz BW) 155.52MHz ⁶	ϕJ		0.3	0.7	ps
Period Jitter ⁷ RMS P/P	ϕJ		2.7 23		ps ps
Enable/Disable					
Output Enabled ⁸ Output Disabled	V_{IH} V_{IL}	0.7* V_{DD}		0.3* V_{DD}	V V
Enable/Disable Time	t_D			200	ns
Enable/Disable Leakage Current				±200	uA
Enable Pull-Up Resistor Output Enabled Output Disabled			33 1		kOhm MOhm
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		9x14x4.5			mm

1. The VCJ5 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. See Standard Frequencies and Ordering Information for more information.
3. Includes calibration tolerance, operating temperature, supply voltage variations,, aging and IR reflow.
4. Figure 2 defines these parameters and Figure 3 defines the test circuit.
5. Duty Cycle is defines as the On/Time Period.
6. Measured using an Agilent E5052, 155.520MHz.
7. Measured using a LeCroy 8600, 25K samples.
8. Outputs will be Enabled if Enable/Disable is left open.



Package and Pinout

Table 3. Pinout

Pin #	Symbol	Function
1	E/D or NC	Enable Disable or No Connection
2	E/D or NC	Enable Disable or No Connection
3	GND	Electrical and Lid Ground
4	f_o	Output Frequency
5	Cf_o	Complementary Output Frequency
6	V_{DD}	Supply Voltage

The Enable/Disable function is set at the factory on either pin 1 or pin 2 and is an ordering option

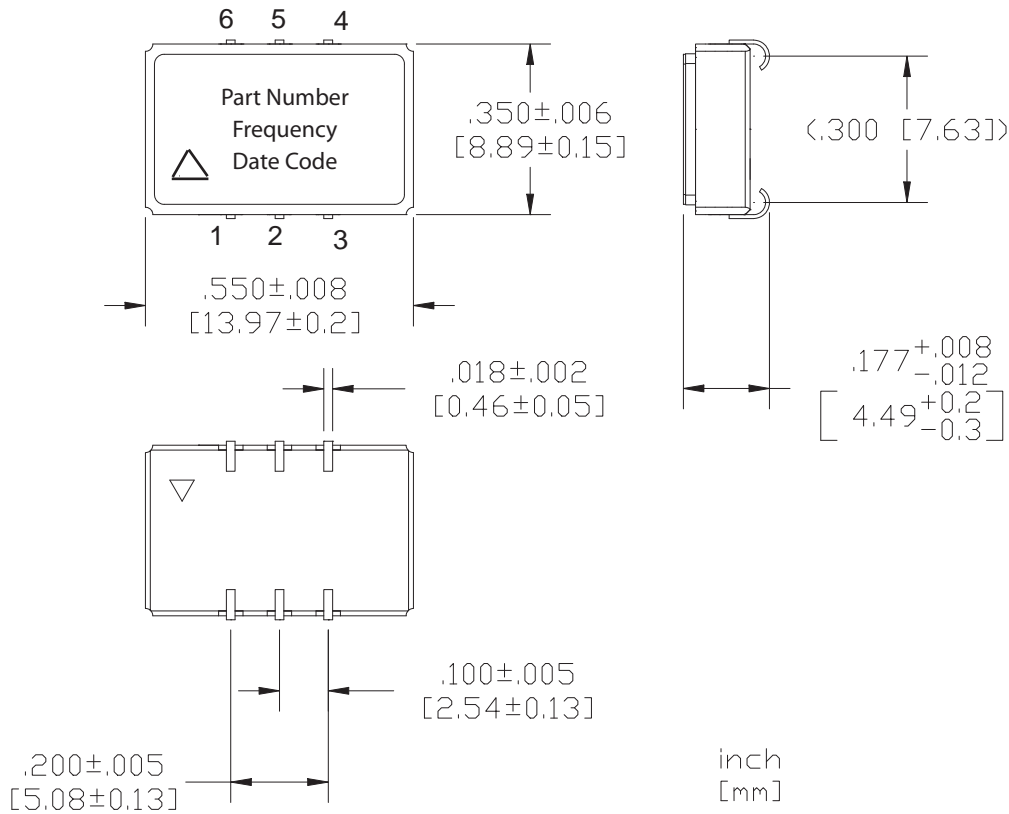


Figure 4 Package

LVPECL Application Diagrams

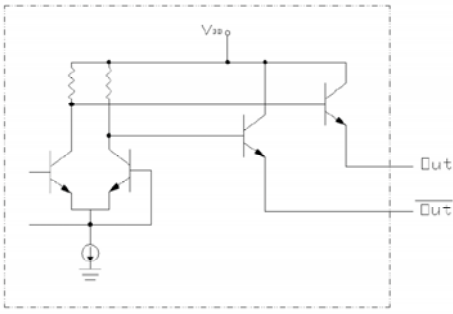


Figure 5 Standard PECL Output Configuration

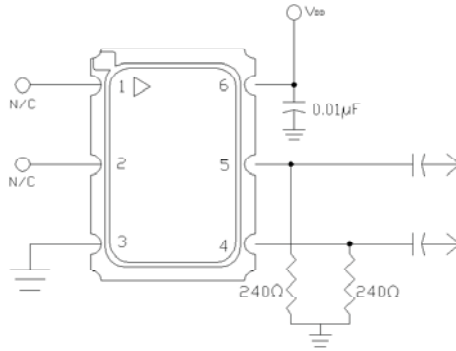


Figure 6 Single Resistor Termination Scheme

Resistor values are typically 120 to 240 ohms for 3.3V operation.
Resistor values are typically 82 to 120 ohms for 2.5V operation.

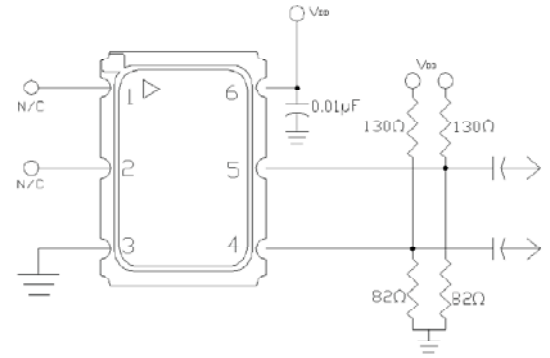


Figure 7 Pull-Up Pull Down Termination

Resistor values are typically for 3.3V operation
For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 240 ohms

The VCJ5 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 5. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 6, and a pull-up/pull-down scheme as shown in Figure 7. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

LVDS Application Diagrams

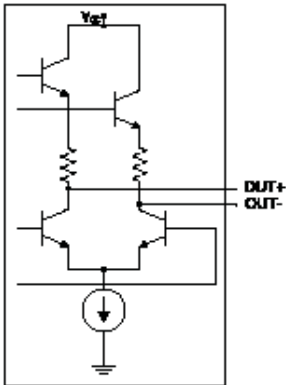


Figure 8 Standard LVDS Output Configuration

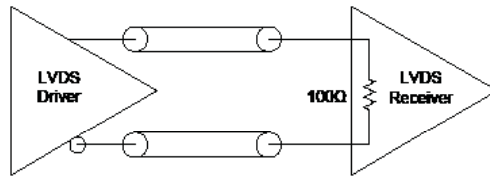


Figure 9 LVDS to LVDS Connection, Internal 100ohm

Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.

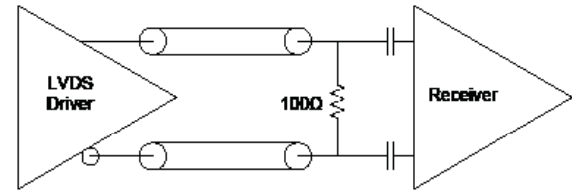


Figure 10 LVDS to LVDS Connection External 100ohm and AC blocking caps

Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

Environmental and IR Compliance

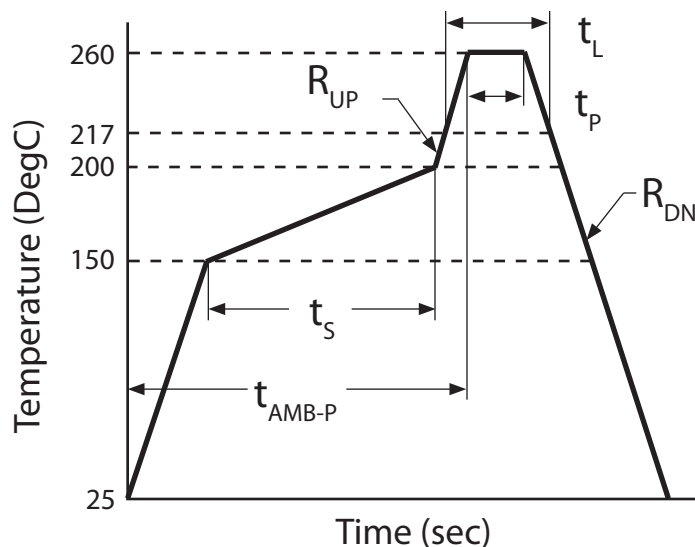
Table 4. Environmental Compliance	
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 2003
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold over Nickel

IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 5. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Parameter	Symbol	Value
PreHeat Time	t_s	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	t_L	150 sec Max
Time to Peak Temperature	t_{AMB-P}	480 sec Max
Time at 260°C	t_P	10 sec Max
Time at 240°C	t_{P2}	60 sec Max
Ramp down	R_{DN}	6°C/sec Max



Maximum Ratings, Tape & Reel

Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Although ESD protection circuitry has been designed into the VCJ5, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.

ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{STORE}	-55/125	°C
Supply Voltage	V_{DD}	-0.5 to 5.0	V
Enable Disable Voltage	$V_{E/D}$	-0.5 to $V_{DD}+0.5$	
ESD, Human Body Model		1000	V
ESD, Charged Device Model		1000	V

Table 7. Tape and Reel Information

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
24	11.5	1.5	4	12	330	1.78	13	21	100	25	30	200

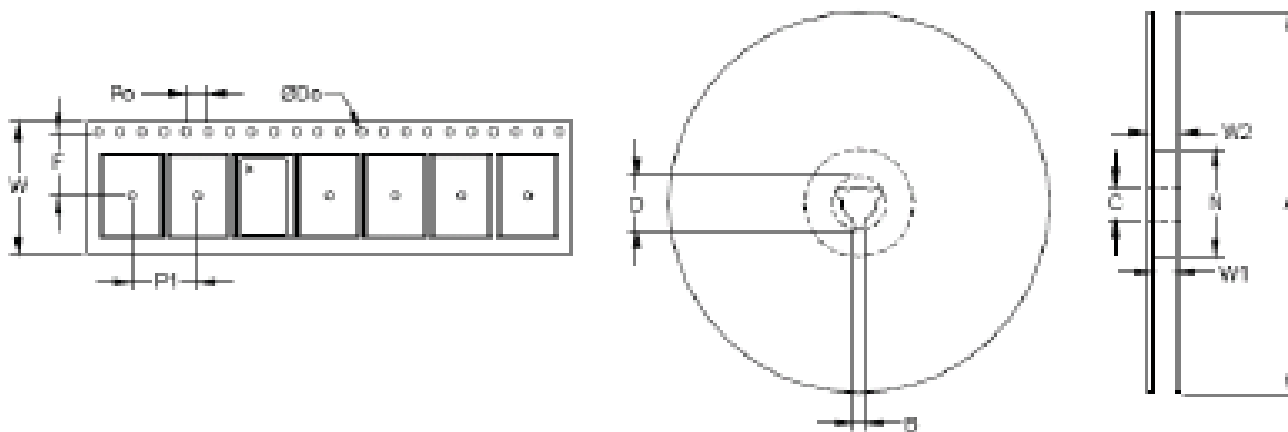


Table 8. Standard Frequencies (MHz)

19.4400	25.0000	27.1200	33.0000	33.3330	35.0000	35.5000	38.8800	40.0000	40.6800
43.7500	50.0000	53.1250	56.0000	61.4400	62.2080	62.5000	66.0000	68.0000	70.0000
71.5000	74.1758	74.2500	75.0000	75.4000	77.7600	78.1250	80.0000	81.2500	83.3330
84.0000	86.0000	90.0000	95.0000	100.0000	105.0000	106.2500	110.0000	112.0000	112.5000
114.2850	120.0000	124.4160	125.0000	125.0093	128.0000	130.0000	130.5882	133.0000	135.0000
136.0000	140.0000	142.5408	143.0000	148.7500	150.0000	153.6000	153.8500	155.5200	156.1734
156.2500	156.2539	156.2740	156.2930	159.3750	160.0000	161.1328	162.3250	164.3555	165.0000
166.0000	166.5600	166.6286	166.6667	167.3317	167.4100	168.2009	168.6997	172.6423	173.3708
173.4380	175.0000	176.0950	176.8382	177.3437	180.0000	187.0177	187.5000	190.0000	192.4560
195.3125	200.0000	212.4840	212.5000	225.0000	250.0000	260.0000			

Ordering Information

VCJ5 - X X X - 000M000000

Product

XO, 9x14x4.5 Package

Output and Voltage

Q: +3.3 Vdc 5%, LVPECL
 R: +3.3 Vdc 5%, LVPECL
 L: +3.3 Vdc 5%, LVDS
 V: +2.5 Vdc 5%, LVDS

Enable/Disable

A: E/D is on Pin 2, Active High or Open
 C: E/D is on Pin 1, Active High or Open

Frequency in MHz

Stability/Temp Range

A: ±100 ppm over -10/70°C
 B: ±50 ppm over -10/70°C
 C: ±100 ppm over -40/85°C
 D: ±50 ppm over -40/85°C
 E: ±25ppm over -10/70°C
 F: ±25ppm over -40/85°C

**Note: not all combination of options are available.
 Other specifications may be available upon request.*

Example: VCJ5-QAA-155M520000

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