8-PIN SINGLE PFC CONTROLLER WITH 50% PWM CLOCK SIGNAL

GENERAL DESCRIPTION

The 8 pin single PFC controller with 50% PWM clock , CM6503/4 is a space-saving controller for power factor corrected, switched mode power supplies that offers very low start-up and operating currents. For the power supply less than 500Watt, its performance could be very close to CM6800 or ML4800 architecture. Its IAC has dual function. 8 pin CM6503/4 does not require and bleed resistors. It use IAC pin during the start up condition to start up CM6503/4. After CM6503/4 is on, IAC will switch itself back to the IAC function.

Power Factor Correction (PFC) offers the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply fully compliant to IEC1000-3-2 specifications. The CM6503/4 includes circuits for the implementation of a leading edge, average current “boost” type PFC and a trailing edge, PWM Clock signal which will not turn on until PFC boost output reaches steady state.

The CM6503’s PFC and PWM Clock operate at the same frequency, 67kHz. The PFC frequency of the CM6504 is automatically set at half that of the 134kHz PWM. This higher frequency allows the user to design with smaller PWM components while maintaining the optimum operating frequency for the PFC. An PFC OVP comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting for enhanced system reliability.

FEATURES

- Enable lowest BOM for power supply with PFC
- Patented slew rate enhanced voltage error amplifier with advanced input current shaping technique
- Universal Line Input Voltage
- No bleed resistor required
- CCM boost or DCM boost with leading edge modulation PFC using Input Current Shaping Technique
- Feedforward IAC pin to do the automatic slope compensation
- PFCOVP, TriFault Detect, PFC VCCOVP, Precision -1V PFC ILIMIT
- Low supply currents; start-up: 100uA typical, operating current: 2mA typical.
- Synchronized leading PFC and trailing edge modulation PWM Clock for the down stream DC to DC stage to reduce ripple current in the storage capacitor between the PFC and PWM sections and to reduce switching noise in the system
- VINOK Comparator to guarantee to enable PWM Clock when PFC reach steady state
- UVLO, VREFOK, and brownout protection

24 Hours Technical Support---WebSIM

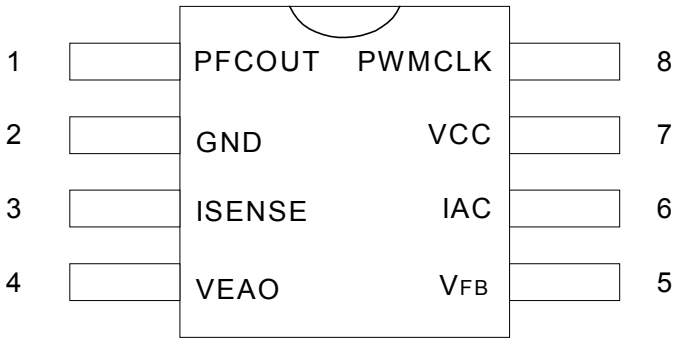
Champion provides customers an online circuit simulation tool called WebSIM. You could simply logon our website at www.champion-micro.com for details.

APPLICATIONS

- Desktop PC Power Supply
- AC Adaptor
- Internet Server Power Supply
- IPC Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

PIN CONFIGURATION

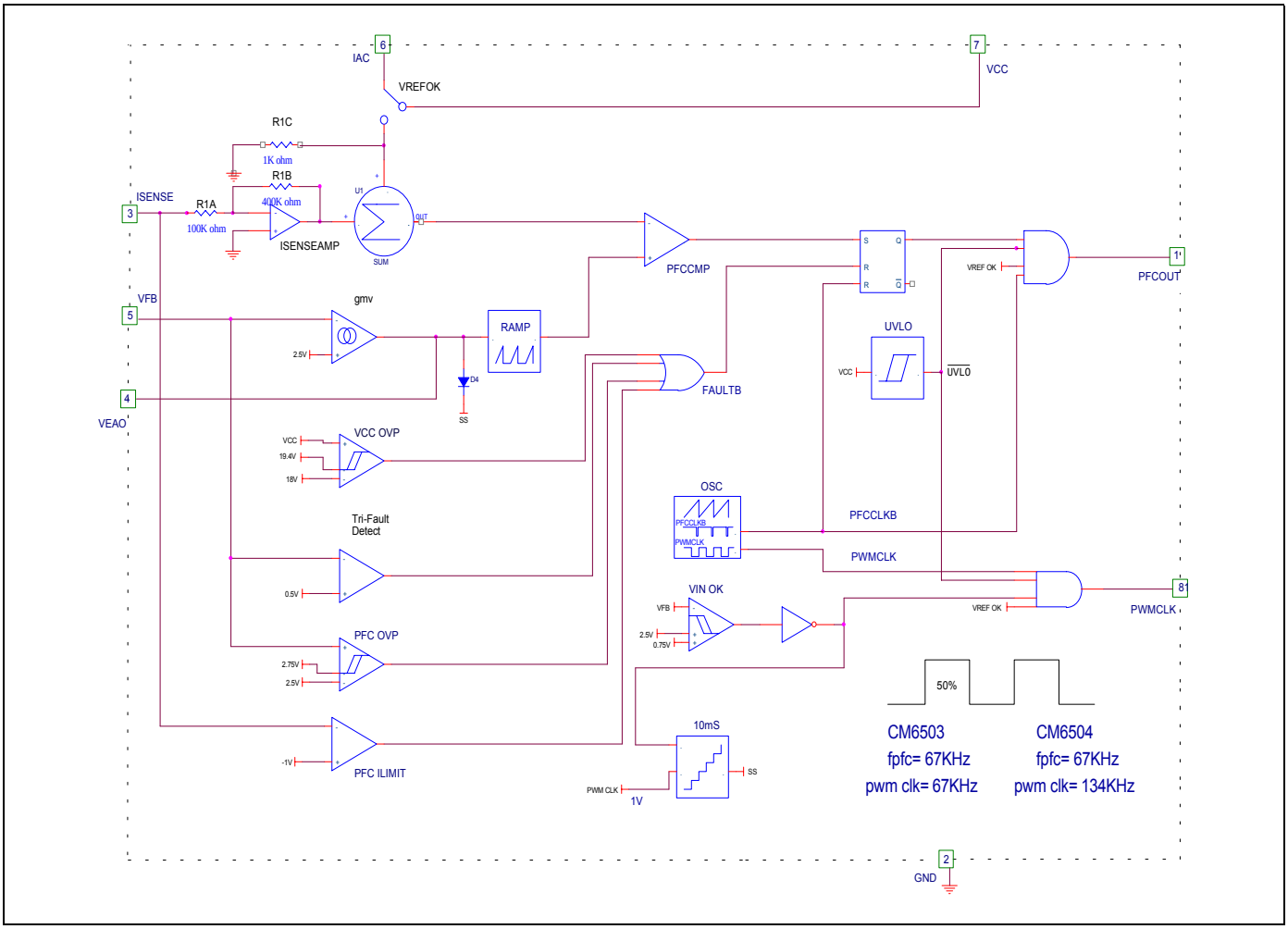
DIP-08 (P08)
Top View



PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	PFC OUT	PFC driver output	0		VCC	V
2	GND	Ground				
3	I_{SENSE}	Current sense input to the PFC current limit comparator	-5		0.7	V
4	VEAO	PFC transconductance voltage error amplifier output	0		6	V
5	V_{FB}	PFC transconductance voltage error amplifier input	0	2.5	3	V
6	IAC	Feedforward input to do slope compensation and to start up the system	0		1	V
7	V_{CC}	Positive supply	10	15	23	V
8	PWM CLK					

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6503IP	-40℃ to 125℃	8-Pin PDIIP (P08)
CM6504IP	-40℃ to 125℃	8-Pin PDIP (P08)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V_{CC} MAX		23	V
IAC (after start up)	GND-0.3	1.0	V
I_{SENSE} Voltage	-5	0.7	V
PFC OUT	GND – 0.3	VCC + 0.3	V
PWM Clock	GND – 0.3	VCC + 0.3	V
VEAO	0	6.3	V
Voltage on Any Other Pin	GND – 0.3	VREF + 0.3	V
I_{CC} Current (Average)		40	mA
Peak PFC OUT Current, Source or Sink		0.5	A
Peak PWM OUT Current, Source or Sink		0.5	A
PFC OUT, PWM OUT Energy Per Cycle		1.5	μJ
Junction Temperature		150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA}) PDIP-08 SOP-08		80	℃/W

ELECTRICAL CHARACTERISTICS **Unless otherwise stated, these specifications apply Vcc=+15V, T_A=Operating Temperature Range (Note 1)**

Symbol	Parameter	Test Conditions	CM6503/4			Unit
			Min.	Typ.	Max.	
Voltage Error Amplifier (g_{mv})						
	Input Voltage Range		0		5	V
	Transconductance	V_{NONINV} = V_{INV}, VEAO = 3.75V	30	65	90	μmho
	Feedback Reference Voltage		2.45	2.5	2.55	V
	Input Bias Current	Note 2		-0.5	-1.0	μA
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Sink Current	V_{FB} = 3V, VEAO = 6V	-20	-35		μA
	Source Current	V_{FB} = 1.5V, VEAO = 1.5V	30	40		μA
	Open Loop Gain		50	60		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	50	60		dB
IAC						
	Input Impedance	ISENSE = 0V	850	1000	1150	Ohm

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply

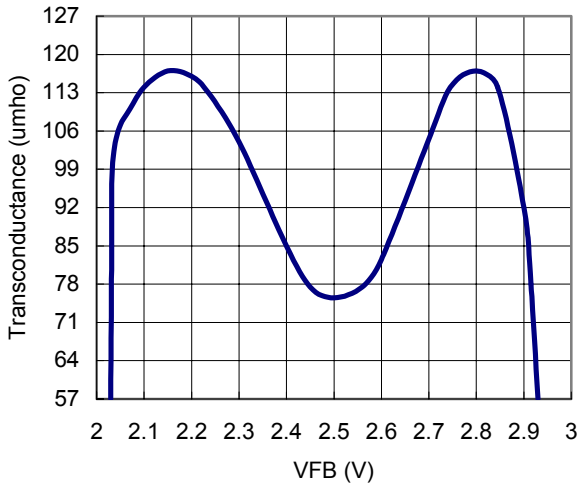
Vcc=+15V, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6503/4			Unit
			Min.	Typ.	Max.	
VCC OVP Comparator						
	Threshold Voltage		19	19.4	20	V
	Hysteresis		1.4	1.5	1.65	V
PFC I_{LIMIT} Comparator						
	Threshold Voltage		-0.9	-1	-1.15	V
	Delay to Output			150	300	ns
Oscillator						
	Initial Accuracy	T_A = 25℃	62	67	74	kHz
	Voltage Stability	10V < V_{CC} < 15V		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	60	67	74.5	kHz
	PFC Dead Time (Note 2)		0.3	0.45	0.65	μs
PFC						
	Minimum Duty Cycle	I_{AC}=100uA,V_{FB}=2.55V, I_{SENSE} = 0V			0	%
	Maximum Duty Cycle	I_{AC}=0uA,V_{FB}=2.0V, I_{SENSE} = 0V	90	95		%
	Output Low Impedance			8	15	ohm
	Output Low Voltage	I_{OUT} = -100mA		0.8	1.5	V
		I_{OUT} = -10mA, V_{CC} = 8V		0.4	0.8	V
	Output High Impendence			8	15	ohm
	Output High Voltage	I_{OUT} = 100mA, V_{CC} = 15V	13.5	14.2		V
	Rise/Fall Time (Note 2)	C_L = 1000pF		50		ns
PWM Clock						
	Duty Cycle Range	CM6503	49.5		50	%
		CM6504	49.5		50	%
	Output Low Impedance			8	15	ohm
	Output Low Voltage	I_{OUT} = -100mA		0.8	1.5	V
		I_{OUT} = -10mA, V_{CC} = 8V		0.7	1.5	V
	Output High Impendence			8	15	ohm
	Output High Voltage	I_{OUT} = 100mA, V_{CC} = 15V	13.5	14.2		V
	Rise/Fall Time (Note 2)	C_L = 1000pF		50		ns
Supply						
	Start-Up Current	V_{CC} = 11V, C_L = 0		100	150	uA
	Operating Current	V_{CC} = 15V, C_L = 0		2.5	4.0	mA
	Undervoltage Lockout Threshold		14.7	15	15.3	V
	Undervoltage Lockout Hysteresis		4.85	5	5.15	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Guaranteed by design, not 100% production test.

TYPICAL PERFORMANCE CHARACTERISTIC



Voltage Error Amplifier (g_{mv}) Transconductance

Functional Description

The CM6503/4 consists of an ICST (Input Current Shaping Technique), CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode) boost PFC (Power Factor Correction) front end and a synchronized PWM Clock to synchronize the down stream DC to DC PWM stage.. The CM6503/4 is pin to pin compatible with FAN6503/4. It is distinguished from earlier combo controllers by its low count, innovative input current shaping technique, and very low start-up and operating currents. PWM clock is to synchronize the conventional trailing-edge modulation DC to DC PWM stage, while the PFC uses leading-edge modulation. This patented Leading Edge/Trailing Edge (LETE) modulation technique helps to minimize ripple current in the PFC DC buss capacitor.

Key features of CM6503/4:

1.) Voltage Error Amplifier is the slew rate enhancement transconductance amplifier, gmv. This transconductance amplifier will increase the transient response 5 to 10 times from the conventional OP
2.) VFB PFC OVP comparator
3.) Tri-fault Detect for UL1950 compliance and enhanced safety
4.) A feedforward signal from IAC pin is added to do the automatic slope compensation. This increases the signal to noise ratio during the light load; therefore, THD is improved at light load and high input line voltage.
5.) CM6503 does not require the bleed resistor and it uses the less than 500k ohm resistor between IAC pin and rectified line voltage to feed the initial current before the chip wakes up.
6.) VINOK comparator is added to guaranteed PWM Clock cannot turn on until VFB reaches 2.5V in which PFC boost output is about steady state, typical 380V.
7.) 8 pin packages
8.) No internal Zener which has been replaced with VCCOVP comparator

The CM6503 operates both PFC and PWM sections at 67kHz, while the CM6504 operates the PWM section at twice the frequency (134kHz) of the PFC. This allows the use of smaller PWM magnetic and output filter components, while minimizing switching losses in the PFC stage.

Several protection features have been built into the CM6503/4. These include soft-start, redundant PFC overvoltage protection, Tri-Fault Detect, VINOK, peak current limiting, duty cycle limiting, under-voltage lockout, reference ok comparator and VCCOVP.

Detailed Pin Descriptions

PFC OUT (Pin 1)

PFC OUT is the high-current power driver capable of directly driving the gate of a power MOSFET with peak currents up to -1A and +0.5A. Both outputs are actively held low when VCC is below the UVLO threshold level which is 15V or VREFOK comparator is low.

GND (Pin 2)

GND is the return point for all circuits associated with this part. Note: a high-quality, low impedance ground is critical to the proper operation of the IC. High frequency grounding techniques should be used.

ISENSE (Pin 3)

This pin ties to a resistor which senses the PFC input current. This signal should be negative with respect to the IC ground. It internally feeds the pulse-by-pulse current limit comparator and the current sense feedback signal. The ILIMIT trip level is –1V. The ISENSE feedback is internally multiplied by a gain of four and compared against the internal programmed ramp to set the PFC duty cycle. The intersection of the boost inductor current downslope with the internal programming ramp determines the boost off-time.

It requires a RC filter between ISENSE and PFC boost sensing resistor.

VEAO (Pin 4)

This is the PFC slew rate enhanced transconductance amplifier output which needs to connected with a compensation network.

VFB (Pin 5)

Besides this is the PFC slew rate enhanced transconductance input, it also tie to a couple of protection comparators, PFCOVP, and Tri-Fault Detect.

IAC (pin 6)

Typically, it has a feedforward resistor, RAC, less than 500K ohm resistor connected between this pin and rectified line input voltage.

This pin serves 2 purposes:

1.) During the startup condition, it supplies the startup current; therefore, the system does not requires additional bleed resistor to start up the chip.
2.) The current of RAC will program the automatic slope compensation for the system. This feedforward signal can increase the signal to noise ratio for the light load condition or the high input line voltage condition.

VCC (Pin 7)

VCC is the power input connection to the IC. The VCC start-up current is 100uA. The no-load ICC current is 2mA. VCC quiescent current will include both the IC biasing currents and the PFC output currents. Given the operating frequency and the MOSFET gate charge (Qg), average PFC output currents can be calculated as IOUT = Qg x F. The average magnetizing current required for any gate drive transformers must also be included. The VCC pin is also assumed to be proportional to the PFC output voltage. Internally it is tied to the VCC OVP comparator (19.4V) providing redundant high-speed over-voltage protection (OVP) of the PFC stage. VCC also ties internally to the UVLO circuitry and VREFOK comparator, enabling the IC at 15V and disabling it at 10V. VCC must be bypassed with a high quality ceramic bypass capacitor placed as close as

possible to the IC. Good bypassing is critical to the proper operation of the CM6503/4.

VCC is typically produced by an additional winding off the boost inductor or PFC Choke, providing a voltage that is proportional to the PFC output voltage. Since the VCC OVP max voltage is 19.4V, an internal shunt limits VCC overvoltage to an acceptable value. An external clamp, such as shown in Figure 1, is desirable but not necessary.

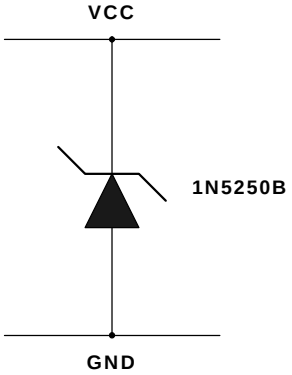


Figure 1. Optional VCC Clamp

This limits the maximum VCC that can be applied to the IC while allowing a VCC which is high enough to trip the VCC OVP. An RC filter at VCC is required between boost trap winding and VCC.

PWMCLK (Pin 8)

PWMCLK is the PWM Clock signal for the down stream DC to DC PWM stage. This signal will not be on until the PFC boost output reaches steady state which means VFB has reaches 2.45V. (Typical PFC boost output is around 380V. Then PWMCLK will send out 50% clock signal which has been perfectly aligned with PFCOUT signal which is leading edge modulation.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6503/4 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero.

By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current draws from the power line matches the instantaneous line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VFB, to allow for a high line of 270VAC_{rms}. The other condition is that the current that the converter is allowed to draw from the line at any given instant must be proportional to the line voltage.

PFC Control: Leading Edge Modulation with Input Current Shaping Technique (I.C.S.T.)

The only differences between the conventional PFC control topology and I.C.S.T. is:
the current loop of the conventional control method is a close loop method and it requires a detail understanding about the system loop gain to design. With I.C.S.T., since the current loop is an open loop, it is very straightforward to implement it.

The end result of the any PFC system, the power supply is like a pure resistor at low frequency. Therefore, current is in phase with voltage.
In the conventional control, it forces the input current to follow the input voltage. In CM6503, the chip thinks if a boost converter needs to behave like a low frequency resistor, what the duty cycle should be.

The following equations is CM6503 try to achieve:

$$R_e = V_{in} / I_{in} \quad (1)$$

$$\bar{I}_l = I_{in} \quad (2)$$

Equation 2 means: average boost inductor current equals to input current.

$$\therefore V_{in} \times \bar{I}_l \approx V_{out} \times \bar{I}_d \quad (3)$$

Therefore, input instantaneous power is about to equal to the output instantaneous power.

For steady state and for the each phase angle, boost converter DC equation at continuous conduction mode is:

$$V_{out}/V_{in} = 1/(1-d) \quad (4)$$

Rearrange above equations, (1), (2),(3), and (4) in term of Vout and d, boost converter duty cycle and we can get average boost diode current equation (5):

$$\bar{I}_d = (1-d)^2 \times V_{out}/R_e \quad (5)$$

Also, the average diode current can be expressed as:

$$\bar{I}_d = \frac{1}{T_{sw}} \int_0^{T_{off}} I_d(t) \cdot dt \quad (6)$$

If the value of the boost inductor is large enough, we can assume $I_d(t) \sim I_d$. It means during each cycle or we can say during the sampling, the diode current is a constant.

Therefore, equation (6) becomes:

$$\bar{I}_d = I_d \times t_{off}/T_{sw} = I_d \times d' = I_d \times (1-d) \quad (7)$$

Combine equation (7) and equation (5), and we get:

$$I_d \times d' = (d')^2 \times V_{out}/R_e$$

$$\therefore I_d = d' \times V_{out}/R_e \quad (8)$$

$$\therefore I_d = \frac{V_{out}}{R_e} \times \frac{t_{off}}{T_{sw}}$$

From this simple equation (8), we implement the PFC control section of the CM6503.

Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn ON right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 2 shows a typical trailing edge control scheme.

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch. Figure 3 shows a leading edge control scheme.

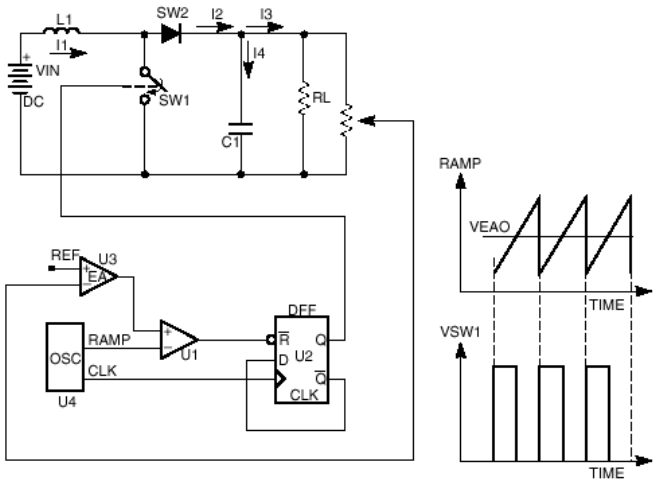


Figure 2. Typical Trailing Edge Control Scheme.

One of the advantages of this control technique is that it required only one system clock. Switch 1(SW1) turns OFF and switch 2 (SW2) turns ON at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method, substantially reducing dissipation in the high-voltage PFC capacitor.

Typical Applications

PFC Section:

PFC Voltage Loop Error Amp, VEAO

The ML4803 utilizes an one pin voltage error amplifier in the PFC section (VEAO). In the CM6503/4, it is using the slew rate enhanced transconductance amplifier, which is the same as error amplifier in the CM6800. The unique transconductance profile can speed up the conventional transient response by 10 times. The internal reference of the VEAO is 2.5V. The input of the VEAO is VFB pin.

PFC Voltage Loop Compensation

The voltage-loop bandwidth must be set to less than 120Hz to limit the amount of line current harmonic distortion. A typical crossover frequency is 30Hz.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$

$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV}: Compensation Net Work for the Voltage Loop
GM_V: Transconductance of VEAO
P_{IN}: Average PFC Input Power
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V.
C_{DC}: PFC Boost Output Capacitor

ΔV_{EAO}: This is the necessary change of the VEAO to deliver the designed average input power. The average value is 6V-3V=3V since when the input line voltage increases, the delta VEAO will be reduced to deliver the same to the output. To over compensate, we choose the delta VEAO is 3V.

Internal Voltage Ramp

The internal ramp current source is programmed by way of VEAO pin voltage. When VEAO increases the ramp current source is also increase. This current source is used to develop the internal ramp by charging the internal 30pF +12/ -10% capacitor. The frequency of the internal programming ramp is set internally to 67kHz.

Design PFC ISENSE Filtering

ISENSE Filter, the RC filter between Rs and ISENSE:

There are 2 purposes to add a filter at ISENSE pin:

1.) Protection: During start up or inrush current conditions, it will have a large voltage cross Rs, which is the sensing resistor of the PFC boost converter. It requires the ISENSE Filter to attenuate the energy.
2.) Reduce L, the Boost Inductor: The ISENSE Filter also can reduce the Boost Inductor value since the ISENSE Filter behaves like an integrator before going ISENSE which is the input of the current error amplifier, IEAO.

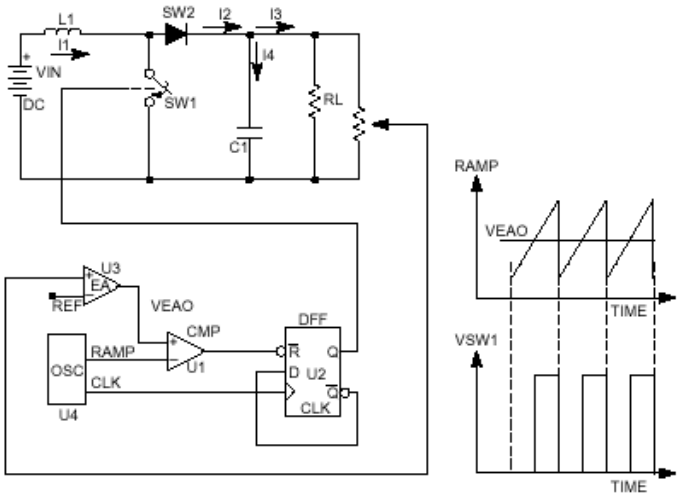


Figure 3 Typical Leading Edge Control Scheme

The I_{SENSE} Filter is a RC filter. The resistor value of the I_{SENSE} Filter is between 100 ohm and 50 ohm. By selecting R_{FILTER} equal to 50 ohm will keep the offset of the IEAO less than 5mV. Usually, we design the pole of I_{SENSE} Filter at fpfc/6, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the I_{SENSE} Filter, C_{FILTER}, will be around 283nF.

IAC, R_{AC}, Automatic Slope Compensation, DCM at high line and light load, and Startup current

There are 4 purposes for IAC pin:

1.) For the leading edge modulation, when the duty cycle is less than 50%, it requires the similar slope compensation, as the duty cycle of the trailing edge modulation is greater than 50%. In the CM6503/4, it is a relatively easy thing to design. Use an less than 500K ohm resistor, R_{AC} to connect IAC pin and the rectified line voltage. It will do the automatic slope compensation. If the input boost inductor is too small, the R_{AC} may need to be reduced more.
2.) During the startup period, Rac also provides the initial startup current, 100uA;therefore, the bleed resistor is not needed.
3.) Since IAC pin with R_{AC} behaves as a feedforward signal, it also enhances the signal to noise ratio and the THD of the input current.
4.) It also will try to keep the maximum input power to be constant. However, the maximum input power will still go up when the input line voltage goes up.

Start Up of the system, UVLO, and VREFOK
During the Start-up period, R_{AC} resistor will provide the start up current~100uA from the rectified line voltage to IAC pin. Inside of CM6503/4 during the start-up period, IAC is connected to VCC until the VCC reaches UVLO voltage which is 15V and internal reference voltage is stable, it will disconnect itself from VCC.

PFC section wakes up after Start up period
After Start up period, PFC section will softly start since VEAO is zero before the start-up period. Since VEAO is a slew rate enhanced transconductance amplifier (see figure 3), VEAO has a high impedance output like a current source and it will slowly charge the compensation net work which needs to be designed by using the voltage loop gain equation.
Before PFC boost output reaches its design voltage, it is around 380V and VFB reaches 2.5V, PWM Clock is low.

PWM clock starts function after PFC reaches steady state
PWM clock is off all the time before PFC VFB reaches 2.45V.

PFC OVP Comparator
PFC OVP Comparator sense VFB pin which is the same the voltage loop input. The good thing is the compensation network is connected to VEAO. The PFC OVP function is a relative fast OVP. It is not like the conventional error amplifier which is an operational amplifier and it requires a local feedback and it make the OVP action becomes very slow. The threshold of the PFC OVP is 2.5V+10% =2.75V with 250mV hysteresis.

Tri-Fault Detect Comparator

To improve power supply reliability, reduce system component count, and simplify compliance to UL1950 safety standards, the CM6503/4 includes Tri-Fault Detect. This feature monitors VFB (Pin 8) for certain PFC fault conditions.

In case of a feedback path failure, the output of the PFC could go out of safe operating limits. With such a failure, VFB will go outside of its normal operating area. Should VFB go too low, too high, or open, Tri-Fault Detect senses the error and terminates the PFC output drive.

Tri-Fault detect is an entirely internal circuit. It requires no external components to serve its protective function.

VCC OVP and generate VCC
For the CM6503/4 system, if VCC is generated from a source that is proportional to the PFC output voltage and once that source reaches 19.4V, PFCOUT, PFC driver will be off.

The VCC OVP resets once the VCC discharges below 17.9V, PFC output driver is enabled. It serves as redundant PFC OVP function.
Typically, there is a bootstrap winding off the boost inductor. The VCC OVP comparator senses when this voltage exceeds 19.4V, and terminates the PFC output drive. Once the VCC rail has decreased to below 17.9V the PFC output drive be enabled. Given that 16V on VCC corresponds to 380V on the PFC output, 19.4V on VCC corresponds to an OVP level of 460V.
It is a necessary to put RC filter between bootstrap winding and VCC. For VCC=15V, it is sufficient to drive either a power MOSFET or a IGBT.

UVLO
The UVLO threshold is 15V providing 5V hysteresis.

PFCOUT and PWM Clock

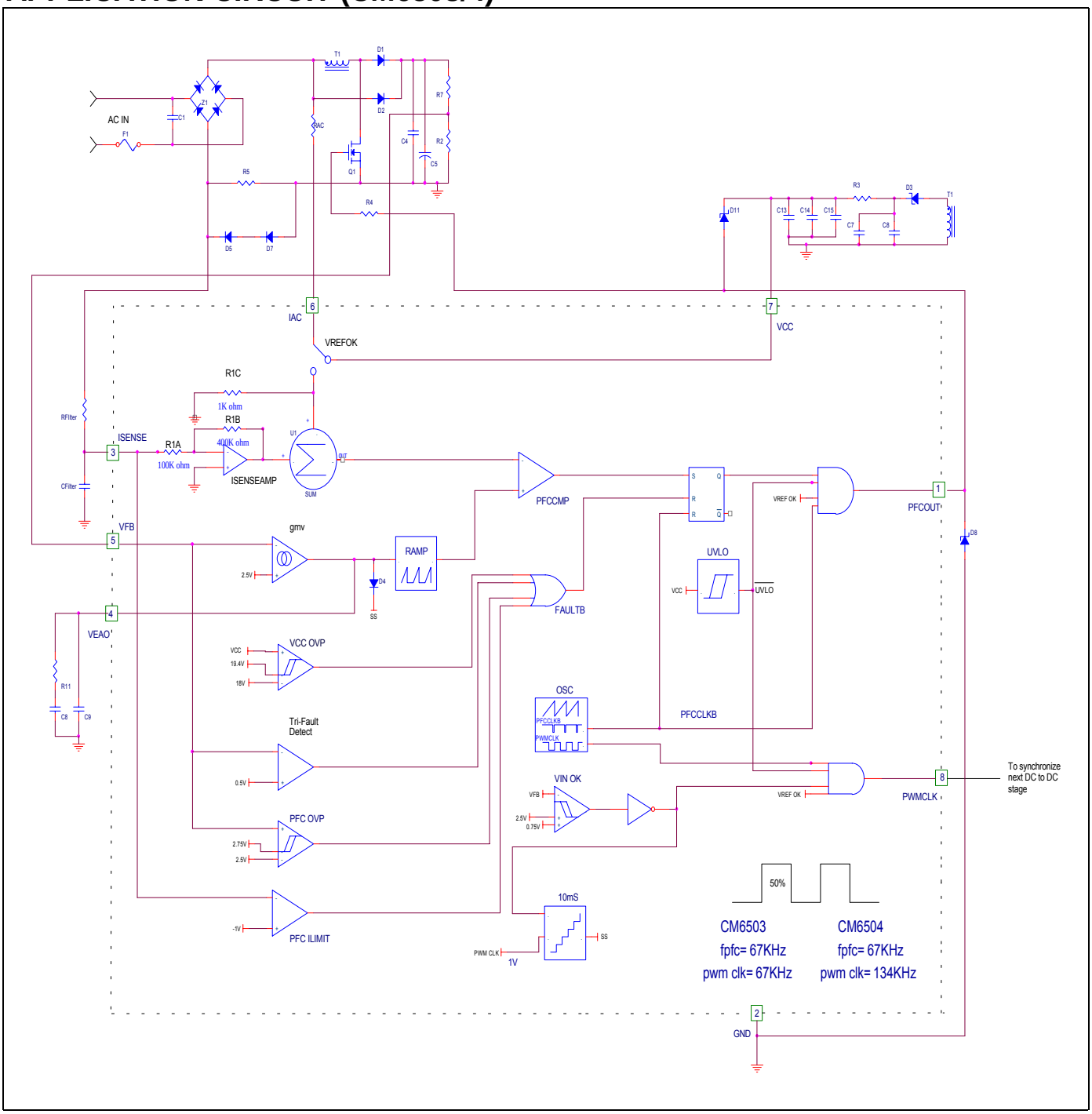
Both PFCOUT and PWMClock are CMOS drivers. They both have adaptive anti-shoot through to reduce the switching loss. Its pull-up is a 30ohm PMOS driver and its pull-down is a 15ohm NMOS driver. It can source 0.5A and sink 1A if the VCC is above 15V.

50% PWM Clock

PWMCLK is the PWM Clock signal for the down stream DC to DC PWM stage. This signal will not be on until the PFC boost output reaches steady state which means VFB has reaches 2.45V. (Typical PFC boost output is around 380V. Then PWMCLK will send out 50% clock signal which has been perfectly aligned with PFCOUT signal which is leading edge modulation.

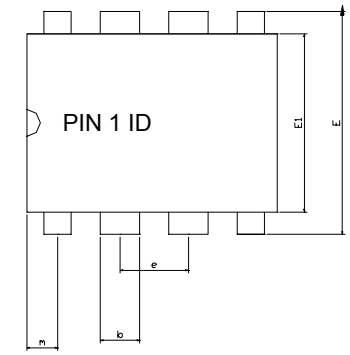
In CM6503, 50% PWM Clock is running at 67.5K hz. In CM6504, 50% PWM Clock is running at 135Khz.

APPLICATION CIRCUIT (CM6503/4)

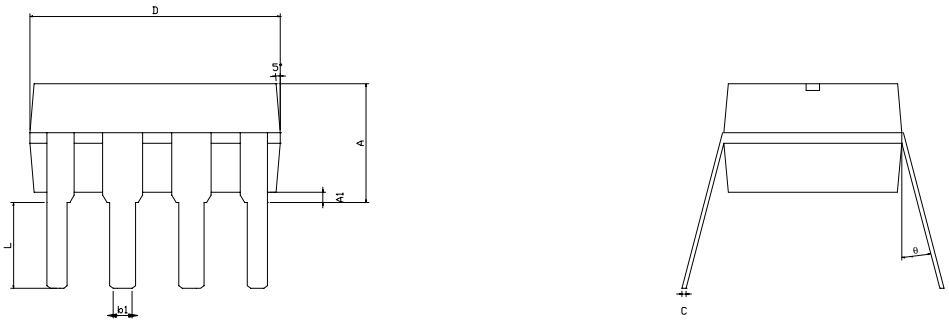


PACKAGE DIMENSION

8-PIN PDIP (P08)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	4.32	---	---	0.170
A1	0.38	---	---	0.015	---	---
b	1.40	---	1.65	0.055	---	0.065
b1	0.40	---	0.56	0.016	---	0.022
C	0.20	---	0.31	0.008	---	0.012
D	9.27	---	9.77	0.365	---	0.385
E	7.49	---	8.26	0.295	---	0.325
E1	6.09	---	6.61	0.240	---	0.260
e	---	2.54	---	---	0.100	---
L	3.18	---	---	0.125	---	---
m	0.50	---	---	0.02	---	---
θ	0	---	15	0	---	15



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