

74VHC00 Quad 2-Input NAND Gate

Features

- High Speed: $t_{PD} = 3.7\text{ns}$ (typ.) at $T_A = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min.)
- Power down protection is provided on all inputs
- Low noise: $V_{OLP} = 0.8\text{V}$ (max)
- Low power dissipation: $I_{CC} = 2\mu\text{A}$ (max.) at $T_A = 25^\circ\text{C}$
- Pin and function compatible with 74HC00


General Description

The VHC00 is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

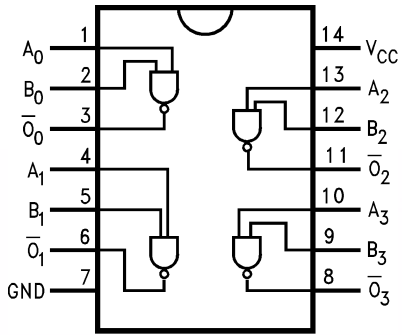
Ordering Information

| Order Number | Package Number | Package Description |
|--------------|----------------|------------------------------------------------------------------------------|
| 74VHC00M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHC00SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHC00MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHC00N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

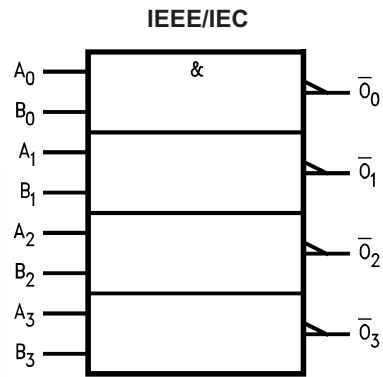
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

| Pin Names | Description |
|-------------|-------------|
| A_n, B_n | Inputs |
| \bar{O}_n | Outputs |

Truth Table

| A | B | \bar{O} |
|---|---|-----------|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|-----------|------------------------------------------|--------------------------|
| V_{CC} | Supply Voltage | -0.5V to +7.0V |
| V_{IN} | DC Input Voltage | -0.5V to +7.0V |
| V_{OUT} | DC Output Voltage | -0.5V to $V_{CC} + 0.5V$ |
| I_{IK} | Input Diode Current | -20mA |
| I_{OK} | Output Diode Current | $\pm 20mA$ |
| I_{OUT} | DC Output Current | $\pm 25mA$ |
| I_{CC} | DC V_{CC}/GND Current | $\pm 50mA$ |
| T_{STG} | Storage Temperature | -65°C to +150°C |
| T_L | Lead Temperature (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|------------|-----------------------------------------------------------------------------------|-----------------------------------|
| V_{CC} | Supply Voltage | 2.0V to +5.5V |
| V_{IN} | Input Voltage | 0V to +5.5V |
| V_{OUT} | Output Voltage | 0V to V_{CC} |
| T_{OPR} | Operating Temperature | -40°C to +85°C |
| t_r, t_f | Input Rise and Fall Time, $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$ | 0ns/V ~ 100ns/V 0ns/V ~ 20ns/V |

Note:

- Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | |
|-----------------|---------------------------|---------------------|---------------------------------------------------------|-------------------------|------|-----------------------|---------------------------------|-----------------------|-------|---|
| | | | | Min. | Typ. | Max. | Min. | Max. | | |
| V _{IH} | HIGH Level Input Voltage | 2.0 | | 1.50 | | | 1.50 | | V | |
| | | 3.0–5.5 | | 0.7 × V _{CC} | | | 0.7 × V _{CC} | | | |
| V _{IL} | LOW Level Input Voltage | 2.0 | | | | 0.50 | | 0.50 | V | |
| | | 3.0–5.5 | | | | 0.3 × V _{CC} | | 0.3 × V _{CC} | | |
| V _{OH} | HIGH Level Output Voltage | 2.0 | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50μA | 1.9 | 2.0 | | 1.9 | | V |
| | | 3.0 | | | 2.9 | 3.0 | | 2.9 | | |
| | | 4.5 | | | 4.4 | 4.5 | | 4.4 | | |
| | | 3.0 | | I _{OH} = -4mA | 2.58 | | | 2.48 | | |
| | | 4.5 | | I _{OH} = -8mA | 3.94 | | | 3.80 | | |
| V _{OL} | LOW Level Output Voltage | 2.0 | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50μA | | 0.0 | 0.1 | | 0.1 | V |
| | | 3.0 | | | | 0.0 | 0.1 | | 0.1 | |
| | | 4.5 | | | | 0.0 | 0.1 | | 0.1 | |
| | | 3.0 | | I _{OL} = 4mA | | | 0.36 | | 0.44 | |
| | | 4.5 | | I _{OL} = 8mA | | | 0.36 | | 0.44 | |
| I _{IN} | Input Leakage Current | 0–5.5 | V _{IN} = 5.5V or GND | | | ±0.1 | | ±1.0 | μA | |
| I _{CC} | Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | | | 2.0 | | 20.0 | μA | |

Noise Characteristics

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | Units |
|---------------------------------|----------------------------------------------|---------------------|-----------------------|-----------------------|--------|-------|
| | | | | Typ. | Limits | |
| V _{OLP} ⁽²⁾ | Quiet Output Maximum Dynamic V _{OL} | 5.0 | C _L = 50pF | 0.3 | 0.8 | V |
| V _{OLV} ⁽²⁾ | Quiet Output Minimum Dynamic V _{OL} | 5.0 | C _L = 50pF | -0.3 | -0.8 | V |
| V _{IHD} ⁽²⁾ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | C _L = 50pF | | 3.5 | V |
| V _{ILD} ⁽²⁾ | Maximum LOW Level Dynamic Input Voltage | 5.0 | C _L = 50pF | | 1.5 | V |

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

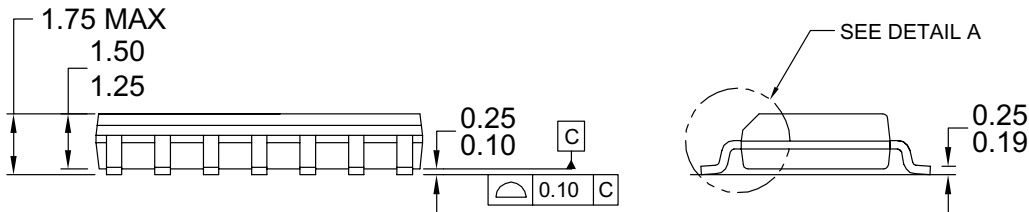
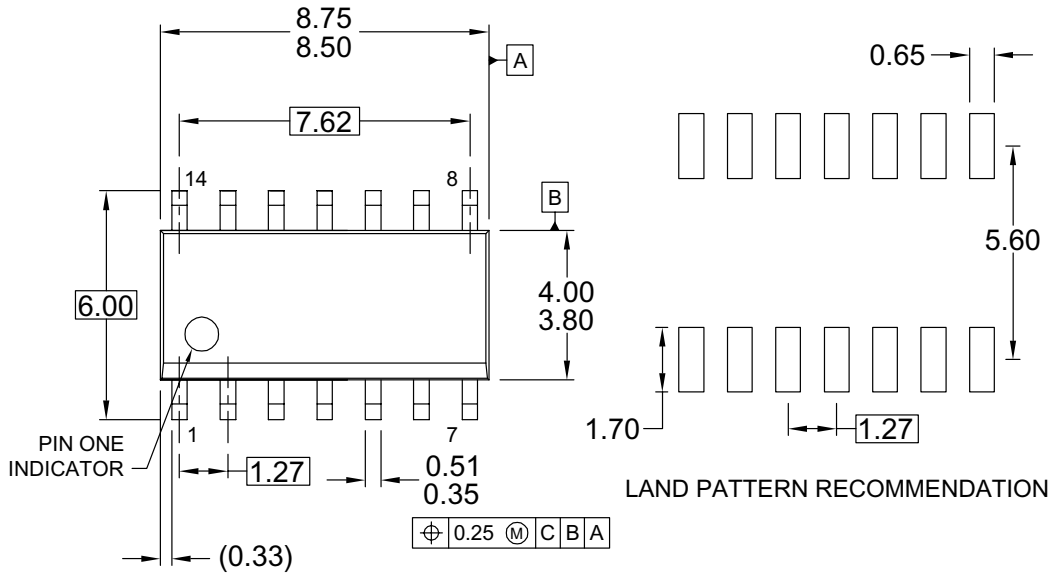
| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Units |
|-------------------------------------|-------------------------------|---------------------|------------------------|-----------------------|------|------|---------------------------------|------|-------|
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| t _{PLH} , t _{PHL} | Propagation Delay | 3.3 ± 0.3 | C _L = 15pF | | 5.5 | 7.9 | 1.0 | 9.5 | ns |
| | | | C _L = 50pF | | 8.0 | 11.4 | 1.0 | 13.0 | |
| | | 5.0 ± 0.5 | C _L = 15pF | | 3.7 | 5.5 | 1.0 | 6.5 | ns |
| | | | C _L = 50pF | | 5.2 | 7.5 | 1.0 | 8.5 | |
| C _{IN} | Input Capacitance | | V _{CC} = Open | | 4 | 10 | | 10 | pF |
| C _{PD} | Power Dissipation Capacitance | | ⁽³⁾ | | 19 | | | | pF |

Note:

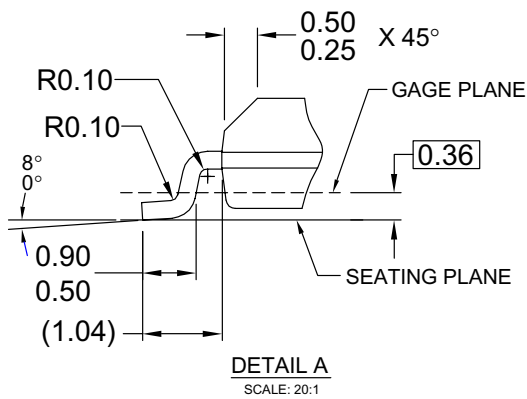
3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per gate).}$$

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

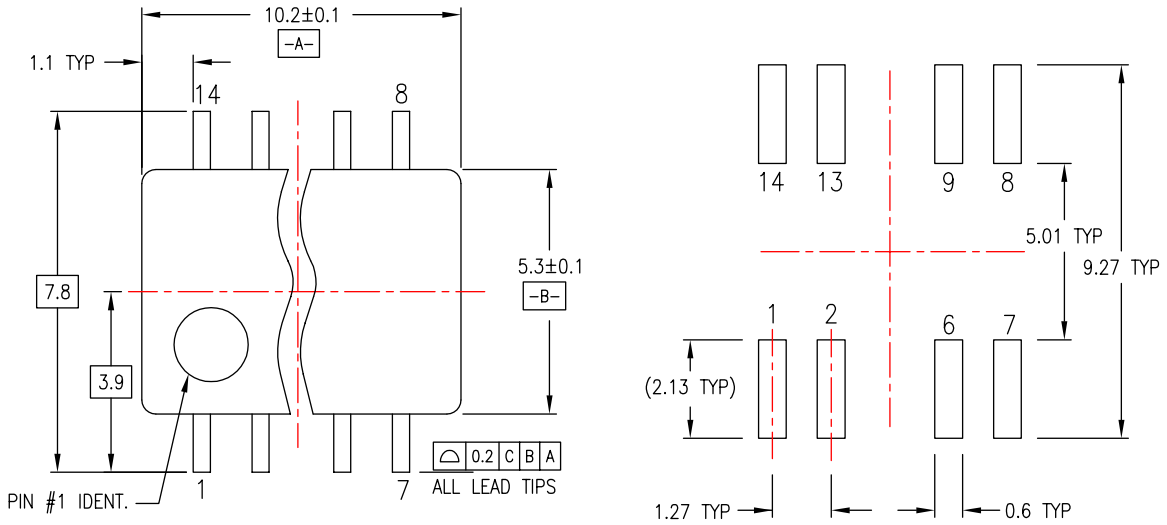
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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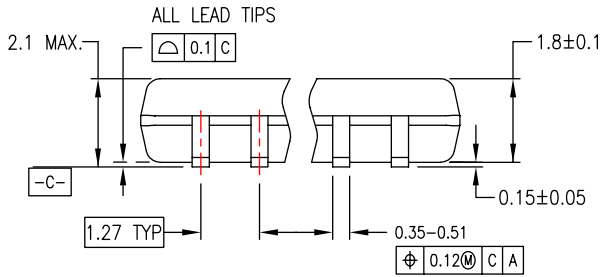
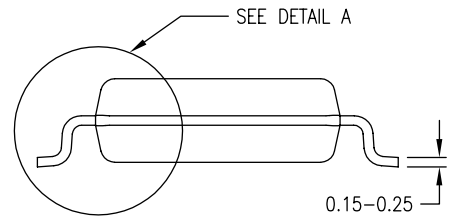
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Physical Dimensions (Continued)



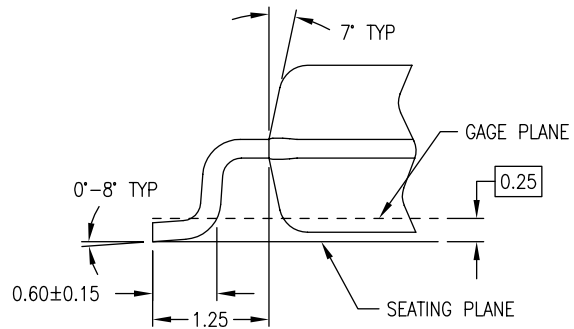
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DREVC

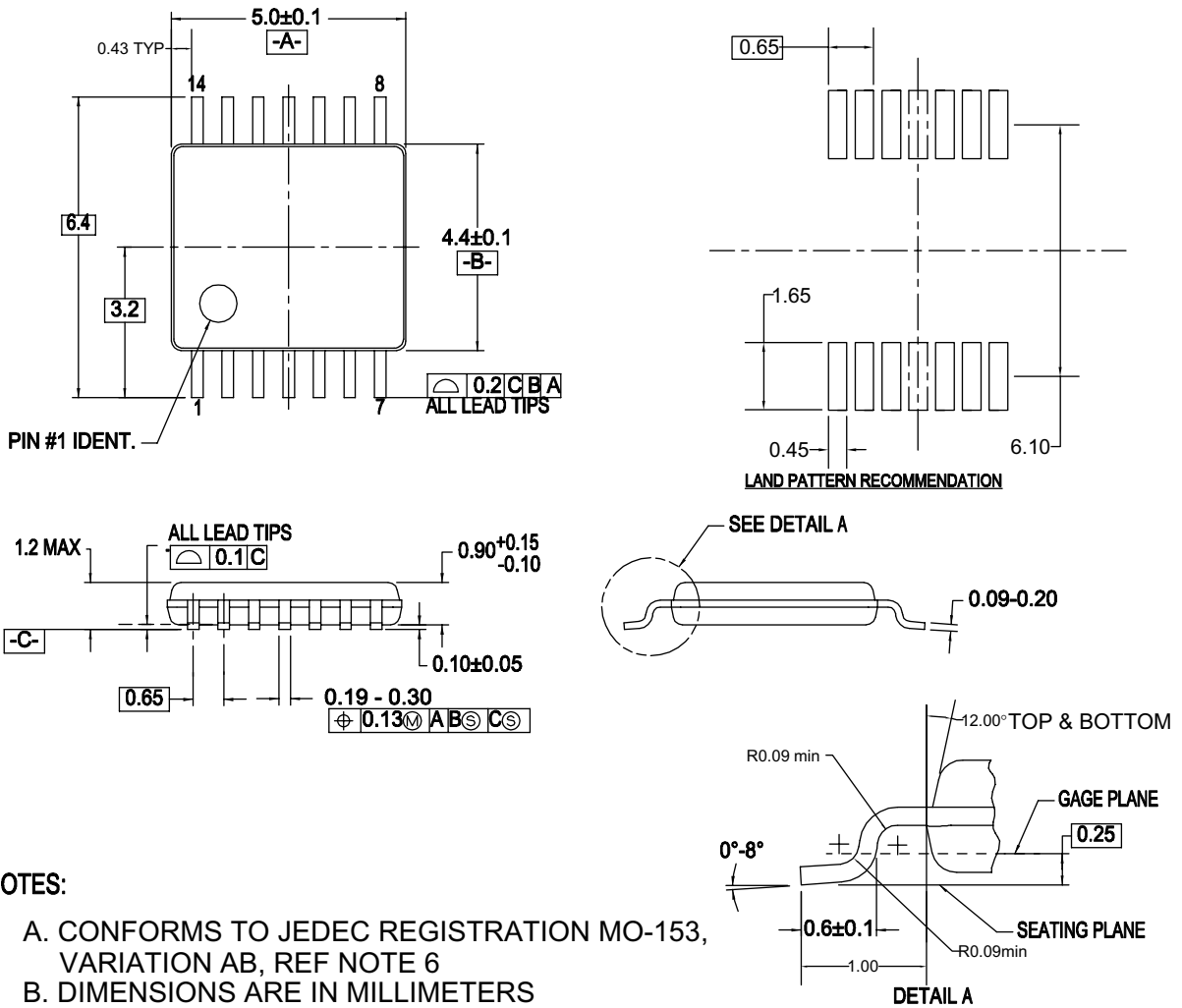
Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

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- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

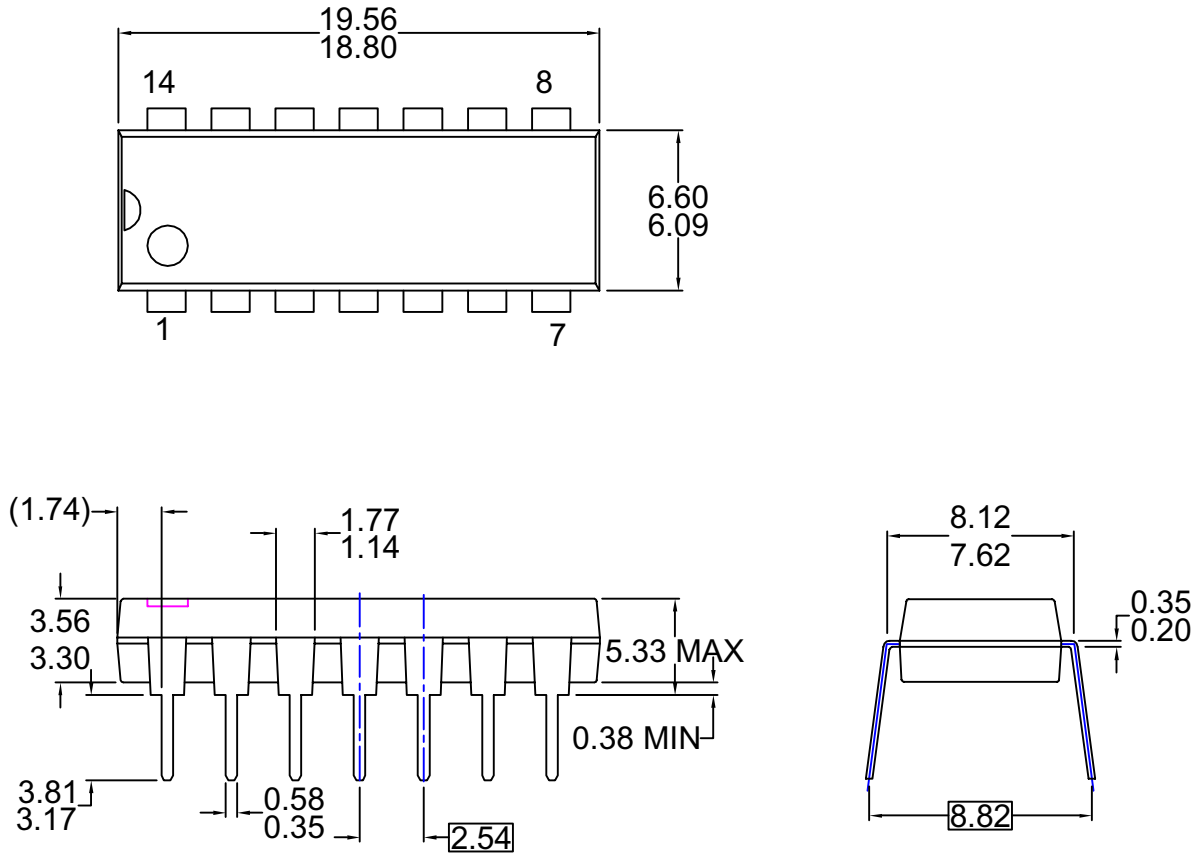
Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994
E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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

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