Rev 0; 11/08

NV, I²C, Stepper Potentiometer

DS3503

General Description

The DS3503 features two synchronized stepping digital potentiometers: one 7-bit potentiometer with RW as its output, and another potentiometer with Y as its output. Both potentiometers reference the RH and RL terminals and feature an output voltage range of up to 15.5V. In addition, both potentiometer outputs can be stepped up and down by configuring the control registers. Programming is accomplished by an I²C-compatible interface that can operate at speeds of up to 400kHz.

Applications

TFT-LCD V_{COM} Calibration

Instrumentation and Industrial Controls

Mechanical Potentiometer Replacement

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3503U+	-40°C to +100°C	10 µSOP
DS3503U+T&R	-40°C to +100°C	10 µSOP

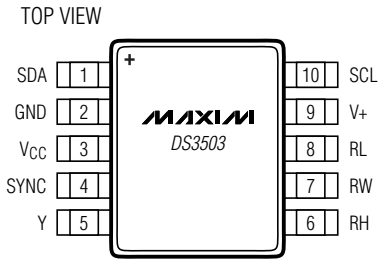
+Denotes a lead-free/RoHS-compliant package.
T&R = Tape and reel.

Typical Operating Circuit appears at end of data sheet.

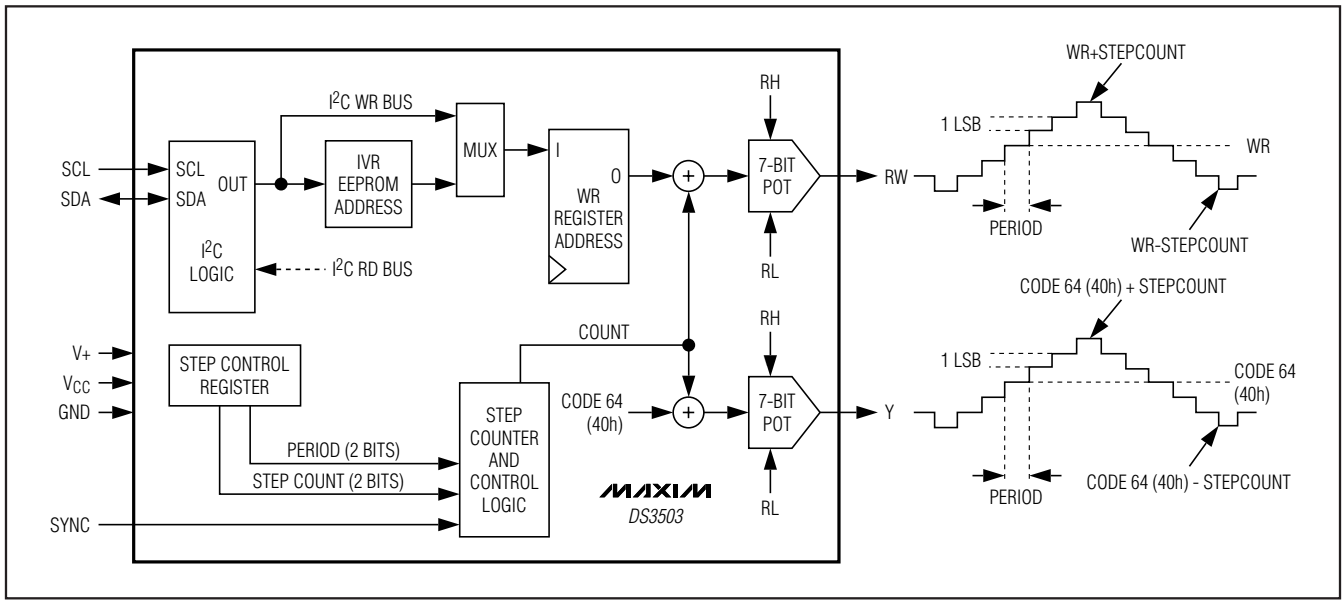
Features

- **128 Wiper Tap Points**
- **Full-Scale Resistance: 5kΩ**
- **Programmable Logic Lets WR Step Up and Down with Timing Controlled by SYNC Input**
- **Second Potentiometer Output Pin (Y) Centered at Position 40h**
- **I²C-Compatible Serial Interface**
- **Digital Operating Voltage: 2.7V to 3.6V**
- **Analog Operating Voltage: 4.5V to 15.5V**
- **Operating Temperature: -40°C to +100°C**
- **10-Pin µSOP Package**

Pin Configuration



Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Relative to GND .....-0.5V to +6.0V
Voltage Range on V+ Relative to GND .....-0.5V to +17V
Voltage Range on SDA, SCL, and SYNC
Relative to V_{CC}.....-0.5V to (V_{CC} + 0.5V), not to exceed 6.0V
Voltage Range on RH, RL, RW, and Y .....-0.5V to V+
Voltage Range Across RH and RL.....-0.5V to V+

Operating Temperature Range .....-40°C to +100°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +100°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	(Note 1)	+2.7		+3.6	V
V+ Voltage		V+ > V_{CC} (Note 1)	+4.5		+15.5	V
Input Logic 0 (SCL, SDA, SYNC)	V_{IL}	(Note 1)	-0.3		0.3 x V_{CC}	V
Input Logic 1 (SCL, SDA, SYNC)	V_{IH}	(Note 1)	0.7 x V_{CC}		V_{CC} + 0.3	V
Switch Current (All Switches)	I_{SW}				3	mA
Resistor Current	I_{RES}				3	mA
SYNC Frequency	f_{SYNC}				1	MHz

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Standby Current	I_{STBY}	V_{CC} = +3.6V, I²C inactive (Note 2)			10	µA
V_{CC} Supply Current (NV Read or Write)	I_{CC}	f_{SCL} = 400kHz (Note 3)			3	mA
V+ Bias Current	I_{V+}				+1	µA
Input Leakage (SDA, SCL, SYNC)	I_L		-1		+1	µA
Low-Level Output Voltage (SDA)	V_{OL}	3mA sink current	0		0.4	V
DCP Wiper Response Time	t_{DCP}				1	µs
I/O Capacitance	$C_{I/O}$			5	10	pF
Power-Up Recall Voltage	V_{POR}	Min V_{CC} when NV memory is recalled (Note 4)	1.2		2.6	V
Power-Up Memory Recall Delay	t_D	V_{CC} > V_{POR} to initial memory recall done (Note 5)			3	ms
Wiper Resistance	R_W	V+ = 15.0V			5000	Ω
End-to-End Resistance (RH to RL)	R_{TOTAL}			5		kΩ
R_{TOTAL} Tolerance			-20		+20	%
CH, CL, CW Capacitance	C_{POT}			10		pF

VOLTAGE-DIVIDER CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, T_A = -40°C to +100°C, with RL = 0V, RH = V+, Y, and RW unloaded, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Integral Nonlinearity	INL	(Note 6)	-1		+1	LSB
Differential Nonlinearity	DNL	(Note 7)	-0.5		+0.5	LSB
Output Matching			-1		+1	LSB
Zero-Scale Error	ZS_{ERROR}	(Note 8)	0	0.5	2	LSB
Full-Scale Error	FS_{ERROR}	(Note 9)	-2	-1	0	LSB
Ratiometric Temp Coefficient	TCV	WR/IVR set to 40h		±4		ppm/°C

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, T_A = -40°C to +100°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$. See Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 10)	0		400	kHz
Bus-Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 11)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 11)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 11)			400	pF
EEPROM Write Time	t_W	(Note 12)		10	20	ms
Pulse-Width Suppression Time at SDA and SCL Inputs	t_{IN}	(Note 13)		50		ns
SDA and SCL Input Buffer Hysteresis				$0.05 \times V_{CC}$		V

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NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, unless otherwise noted.)

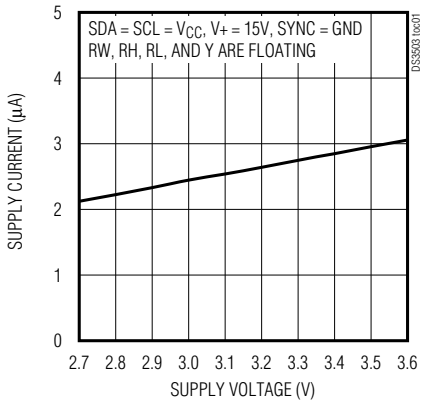
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		T_A = +70°C	30,000			Writes

Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive and currents exiting the IC are negative.
Note 2: I_{STBY} is specified with SDA = SCL = V_{CC} and resistor pins floating.
Note 3: I_{CC} is specified with the following conditions: SCL = 400kHz, SDA pulled up, and RL, RW, RH, and Y floating.
Note 4: This is the minimum V_{CC} voltage that causes NV memory to be recalled.
Note 5: This is the time from $V_{CC} > V_{POR}$ until initial memory recall is complete.
Note 6: Integral nonlinearity is the deviation of a measured resistor setting value from the expected values at each particular resistor setting. Expected value is calculated by connecting a straight line from the measured minimum setting to the measured maximum setting. INL = $[V(RW)_i - (V(RW)_0]/LSB(ideal) - i$, for i = 0...127.
Note 7: Differential nonlinearity is the deviation of the step-size change between two LSB settings from the expected step size. The expected LSB step size is the slope of the straight line from measured minimum position to measured maximum position. DNL = $[V(RW)_{i+1} - (V(RW)_i]/LSB(ideal) - 1$, for i = 0...126.
Note 8: ZS_{ERROR} = code 0 wiper voltage divided by one LSB (ideal).
Note 9: FS_{ERROR} = (code 127 wiper voltage - V+) divided by one LSB (ideal).
Note 10: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard mode timing.
Note 11: CB—total capacitance of one bus line in picofarads.
Note 12: EEPROM write time begins after a STOP condition occurs.
Note 13: Pulses narrower than max are suppressed.

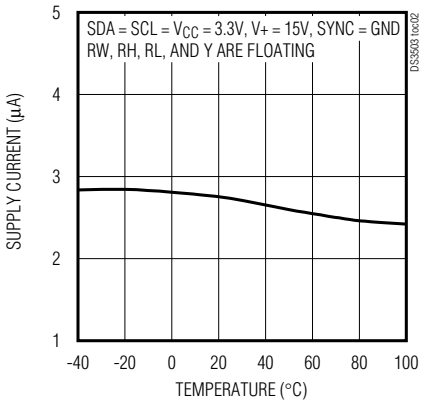
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

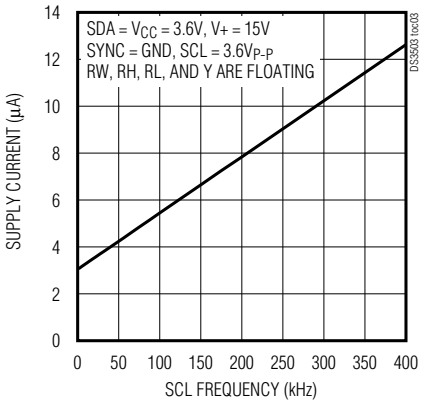
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



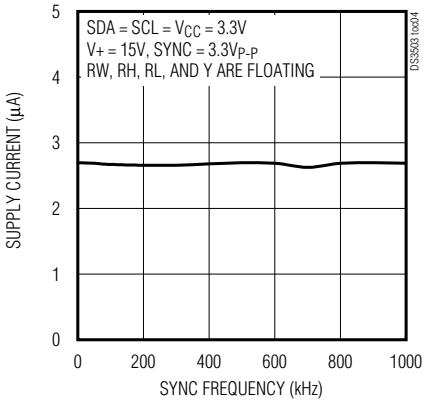
SUPPLY CURRENT vs. SCL FREQUENCY



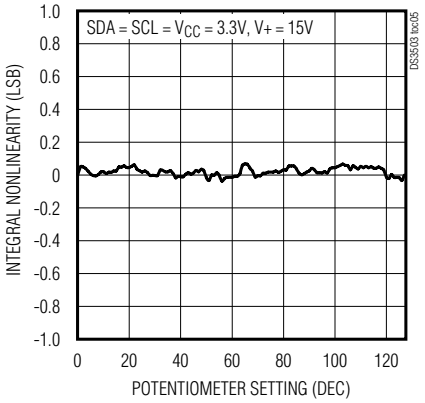
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

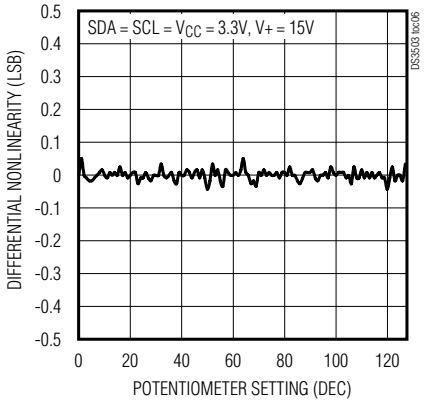
SUPPLY CURRENT vs. SYNC FREQUENCY



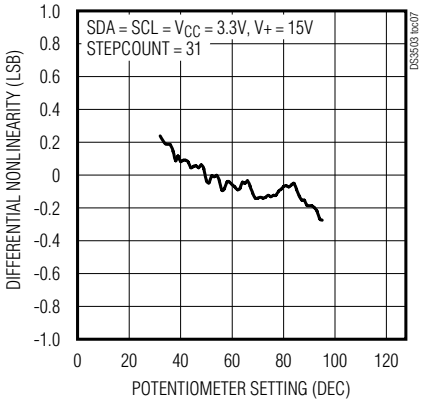
INTEGRAL NONLINEARITY vs. POTENTIOMETER SETTING



DIFFERENTIAL NONLINEARITY vs. POTENTIOMETER SETTING



DELTA BETWEEN RW AND Y vs. POTENTIOMETER SETTING



Pin Description

NAME	PIN	FUNCTION
SDA	1	I²C Serial Data. Input/output for I²C data.
GND	2	Ground Terminal
V_{CC}	3	Supply Voltage Terminal
SYNC	4	Stepping Clock Input. The rising edge updates the outputs.
Y	5	Code 40h Centered DAC Output
RH	6	High Terminal of Potentiometer
RW	7	Wiper Terminal of Potentiometer
RL	8	Low Terminal of Potentiometer
V+	9	Wiper Bias Voltage
SCL	10	I²C Serial Clock. Input for I²C clock.

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Detailed Description

The DS3503 contains two potentiometers whose outputs can be stepped up and down by configuring the control registers. One potentiometer, with output RW, is controlled by the Initial Value Register/Wiper Register (IVR/WR). The other potentiometer is fixed at setting 40h, and its output is on the Y pin. By using the configuration registers and the SYNC pin, the outputs from these two potentiometers can be stepped up and down.

Digital Potentiometers

The RW potentiometer consists of 127 resistors in series connected between the RH and RL pins. Between each resistance and at the two end points, RH and RL, solid-state switches enable RW to be connected within the resistive network. The wiper position and the output on RW are decoded based on the value in WR. If RH, RL, and RW are externally connected in a voltage-divider configuration, the voltage on RW can be easily calculated using the following equation:

$$V_{RW} = V_{RL} + \frac{WR}{127} \times (V_{RH} - V_{RL})$$

Where WR is the wiper position in decimal (0–127). The factory default setting for this potentiometer is 40h.

The Y potentiometer is also referenced to the RH and RL terminals, but is centered at a 40h setting.

Memory Map

The DS3503 contains three registers for controlling the outputs of the two potentiometers, pins RW and Y. Table 1 shows the memory map. IVR/WR is accessed at register address 00h and contains the power-on and current values of the RW potentiometer. The Step Control Register (SCR) controls the stepping function for both potentiometers. The Control Register (CR) controls the write functionality of the IVR/WR.

Initial Value Register/Wiper Register (IVR/WR)

Programming IVR sets the initial power-up value of the RW wiper position. IVR/WR can be visualized as a volatile register (WR) in parallel with a nonvolatile register (IVR). On power-up, the data stored in IVR is loaded into WR, which sets the position of the potentiometer's wiper. The factory default value for IVR is 40h. See the *Stepping* section for information about clamping.

Table 1. Memory Map

NAME	ADDRESS (HEX)	ACCESS	NONVOLATILE	VOLATILE
IVR/WR	00h	R/W	Initial Value Register (IVR), factory setting = 40h	Wiper Register (WR)
SCR	01h	R/W	Step Control Register, factory setting = 00h	—
CR	02h	R/W	Control Register	—
Soft-POR	AAh	R/W	—	Soft Power-On Reset Register

Step Control Register (SCR)

SCR determines the stepping functionality for the RW and Y potentiometers (see the *Stepping* section). The five LSBs, bits 4:0, control the STEPCOUNT, which is the number of steps up and down the wiper moves when stepping is enabled. Bits 5 and 6 control the PERIOD, which is the number of pulses of the SYNC pin required to perform one step.

Setting STEPCOUNT to all zeros disables stepping for the DS3503.

Control Register (CR)

CR located at register address 02h determines how I²C data is written to IVR/WR at 00h. When CR is set to a value of 00h, I²C writes to memory address 00h write to both WR and IVR. When CR is set to a value of 80h, I²C writes to memory address 00h write only to WR. Regardless of the CR setting, all I²C reads of address 00h return the contents of WR.

CR is volatile and powers up as 00h, so I²C writes are to both the IVR and WR locations. The data that is stored in EEPROM and SRAM remains unchanged if the value of CR is changed. Table 3 defines CR.

Stepping

The DS3503 can step the RW output up to WR+STEPCOUNT and down to WR-STEPCOUNT when stepping is enabled. Stepping is enabled when a nonzero STEPCOUNT value is programmed into SCR and pulses are applied to the SYNC input pin. Stepping is disabled when STEPCOUNT = 0 or no pulses are applied on the SYNC input pin. The falling edge of the SYNC pulse updates the outputs. The Y potentiometer output is created by adding to position 40h (code 64 decimal) the same counter value as is added to WR to form the input to the RW potentiometer.

The WR value is internally limited (clamped) to a minimum of STEPCOUNT and maximum of 127 - STEPCOUNT.

When stepping is enabled, the RW wiper position is controlled by WR plus a counter value (COUNT in the Functional Diagram). COUNT increments or decrements when the number of SYNC pulses received since the last COUNT change is equal to PERIOD. SCR bits 6:5 set PERIOD equal to 32, 64, 128, or 256 SYNC pulses (see Table 2).

After power-up or after any I²C write to IVR/WR, CR, or SCR, stepping is initially disabled until 512 plus

Table 2. Step Control Register Description (01h)

BIT	NAME	FUNCTION
4:0	STEPCOUNT	Bit 4 is the MSB; bit 0 is the LSB. These 5 bits define the number of steps in an up or down cycle. Maximum is 31, minimum is 0. A STEPCOUNT of zero corresponds to a disabled counter.
6:5	PERIOD	0, 0: PERIOD = 32 SYNC pulses
		0, 1: PERIOD = 64 SYNC pulses
		1, 0: PERIOD = 128 SYNC pulses
		1, 1: PERIOD = 256 SYNC pulses
7	—	Reserved

Table 3. Control Register Description (02h)

BIT	NAME	FUNCTION
6:0	—	Reserved
7	IVR/WR ADDRESS MODE	0: Read WR; write IVR and WR at address 00h. 1: Read WR; write WR at address 00h.

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PERIOD/2 pulses have been applied to the SYNC input. During this disable time, the power-up or new WR value is applied to the RW potentiometer and position 40h (code 64 decimal) is applied to the Y potentiometer. Additionally, the step counter is cleared during this disable time.

After the initialization pulses, stepping is enabled again. The RW potentiometer starts from the power-up or new WR value and the Y potentiometer starts from position 40h (code 64 decimal). The step counter starts from zero in the up direction.

The stepping function is further described as follows:

An internal counter called PERIODCOUNT is set equal to PERIOD.

The input to the RW potentiometer is WR + COUNT; the input to the Y potentiometer is code 64 + COUNT.

When a SYNC pulse is received:

PERIODCOUNT = PERIODCOUNT - 1

If PERIODCOUNT = 0 (underflow), the following actions occur:

If direction is UP:

COUNT = min (COUNT + 1, STEPCOUNT)

RW = min (127 - STEPCOUNT, WR + COUNT);
Y = 64 + COUNT

PERIODCOUNT is reset to PERIOD

If direction is DOWN:

COUNT = max (COUNT - 1, -STEPCOUNT)

RW = max (STEPCOUNT, WR - COUNT);
Y = 64 - COUNT

PERIODCOUNT is reset to PERIOD

If COUNT = STEPCOUNT, direction is changed from UP to DOWN.

If COUNT = -STEPCOUNT, direction is changed from DOWN to UP.

In this way the RW output steps up to WR+STEPCOUNT, then steps down to WR-STEPCOUNT, and then repeats the cycle. The outputs of the RW and Y DACs change by one LSB = (VRH - VRL)/127 per PERIOD.

STEPCOUNT and PERIOD are programmable from I²C and are stored in the nonvolatile SCR (Table 2).

The STEPCOUNT 5-bit value programmed into SCR<4:0> controls the stepping range reflected in the RW or Y outputs per Table 4, assuming STEPCOUNT < IVR < 127 - STEPCOUNT:

Table 4. DAC Stepping Range

SCR<4:0> (BINARY)	DAC RANGE
0 0000	Stepping disabled; WR is output
0 0001	WR-1 to WR+1
0 0010	WR-2 to WR+2
0 0011	WR-3 to WR+3
0 0100	WR-4 to WR+4
0 0101	WR-5 to WR+5
. . .	. . .
1 1110	WR-30 to WR+30
. . .	. . .
1 1111	WR-31 to WR+31

Example 1:

WR = 41h (65 decimal): SCR<4:0> = STEPCOUNT = 10000 (16 decimal)

RW range: 49 ↔ 81 (decimal)

Y range: 48 ↔ 80 (decimal)

Example 2:

WR = 50h (80 decimal): SCR<4:0> = STEPCOUNT = 11000 (24 decimal)

RW range: 56 ↔ 104 (decimal)

Y range: 40 ↔ 88 (decimal)

Example 3: Clamping at Lower Rail

WR = 10h (16 decimal): SCR<4:0> = STEPCOUNT = 11111 (31 decimal)

RW range: 0 ↔ 62 (decimal)

Y range: 33 ↔ 95 (decimal)

Example 4: Clamping at Upper Rail

WR = 70h (112 decimal): SCR<4:0> = STEPCOUNT = 11111 (31 decimal)

RW range: 65 ↔ 127 (decimal)

Y range: 33 ↔ 95 (decimal)

Table 5. Soft Power-On Reset Register Description (AAh)

BIT	NAME	FUNCTION
6:0	—	Reserved
7	SOFT POR	0: Default value. 1: Recalls values of IVR, CR, and SCR from EEPROM.

Soft Power-On Reset Register (Soft-POR)

By writing register AAh's MSB to 1, a soft power-on reset (soft-POR) can be generated. When the MSB is set to 1, the power-up default values of registers 00h, 01h, and 02h are recalled, and the MSB of AAh self-clears. This soft-POR can be used to recall power-on settings without cycling power to the DS3503.

___*I²C Serial Interface Description*

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. (See Figure 2 and the *I²C AC Electrical Characteristics* table for additional information.)

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

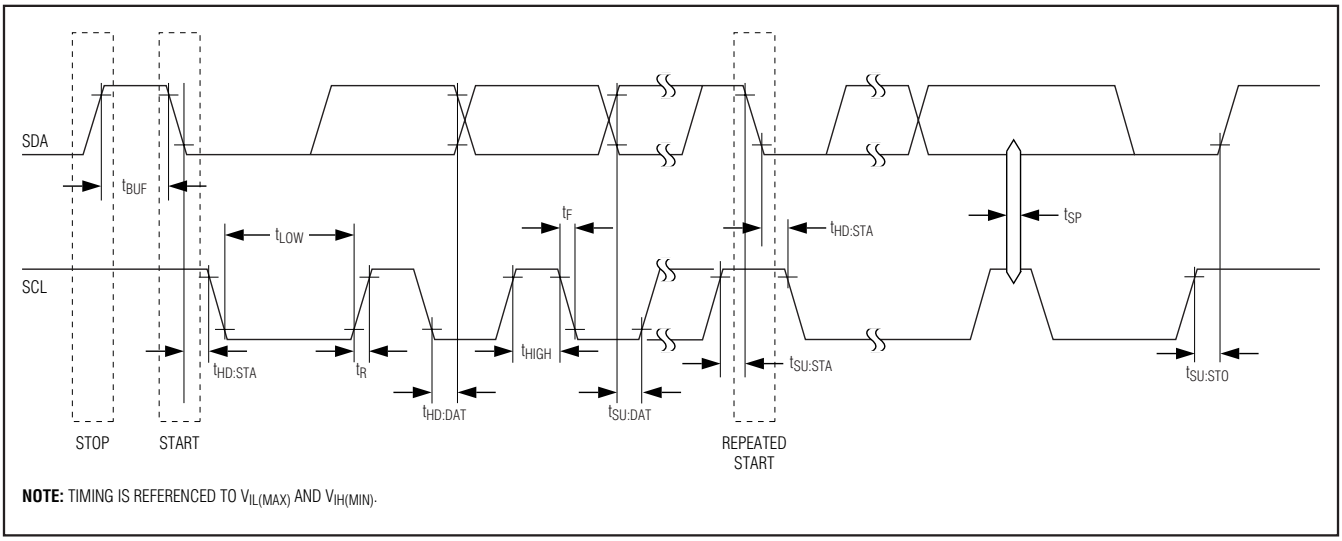


Figure 2. I²C Timing Diagram

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the 9th bit. A device performs a NACK by transmitting a 1 during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 2). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or indicates that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition and the acknowledgment is read using the bit-read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit-read definition, and the master transmits an ACK using the bit-write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The DS3503's slave address is 50h (see Figure 1).

When the R/$\overline{W}$ bit is 0 (such as in 50h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1 (51h in this case), the master is indicating it wants to read from the slave.

If an incorrect slave address is written, the DS3503 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

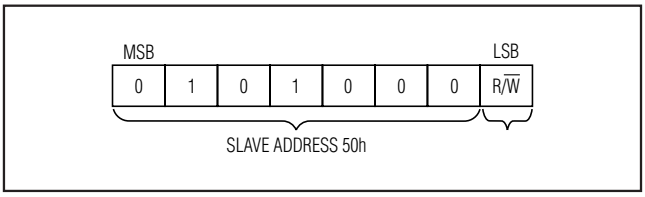


Figure 1. DS3503 Slave Address Byte

I²C Communication

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte-write operations.

When writing to the DS3503, the potentiometer adjusts to the new setting once it has acknowledged the new data that is being written, and the EEPROM is written following the STOP condition at the end of the write command. To change the setting without changing the EEPROM, terminate the write with a repeated START condition before the next STOP condition occurs. Using a repeated START condition prevents the t_W delay required for the EEPROM write cycle to finish.

Acknowledge polling: Any time a EEPROM byte is written, the DS3503 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3503, which allows communication to continue as soon as the DS3503 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM write cycles: The DS3503's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature (hot) as well as at room temperature. Writing to WR/IVR with CR = 80h does not count as a EEPROM write.

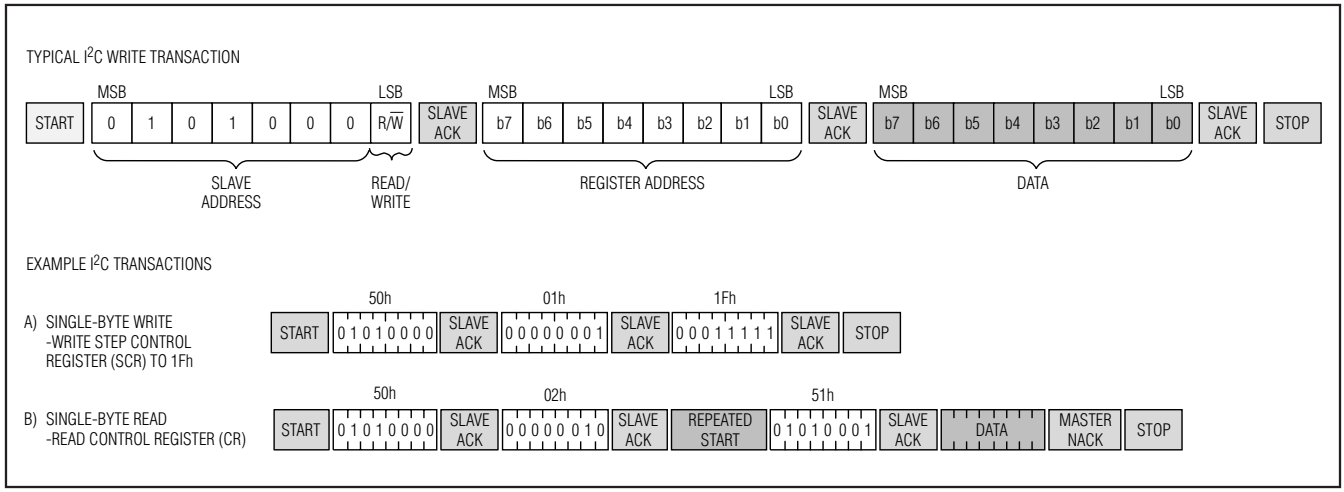


Figure 3. I²C Communication Examples

Reading a single byte from a slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, because requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

See Figure 3 for a read example using the repeated START condition to specify the starting memory location.

Applications Information

Power-Supply Decoupling

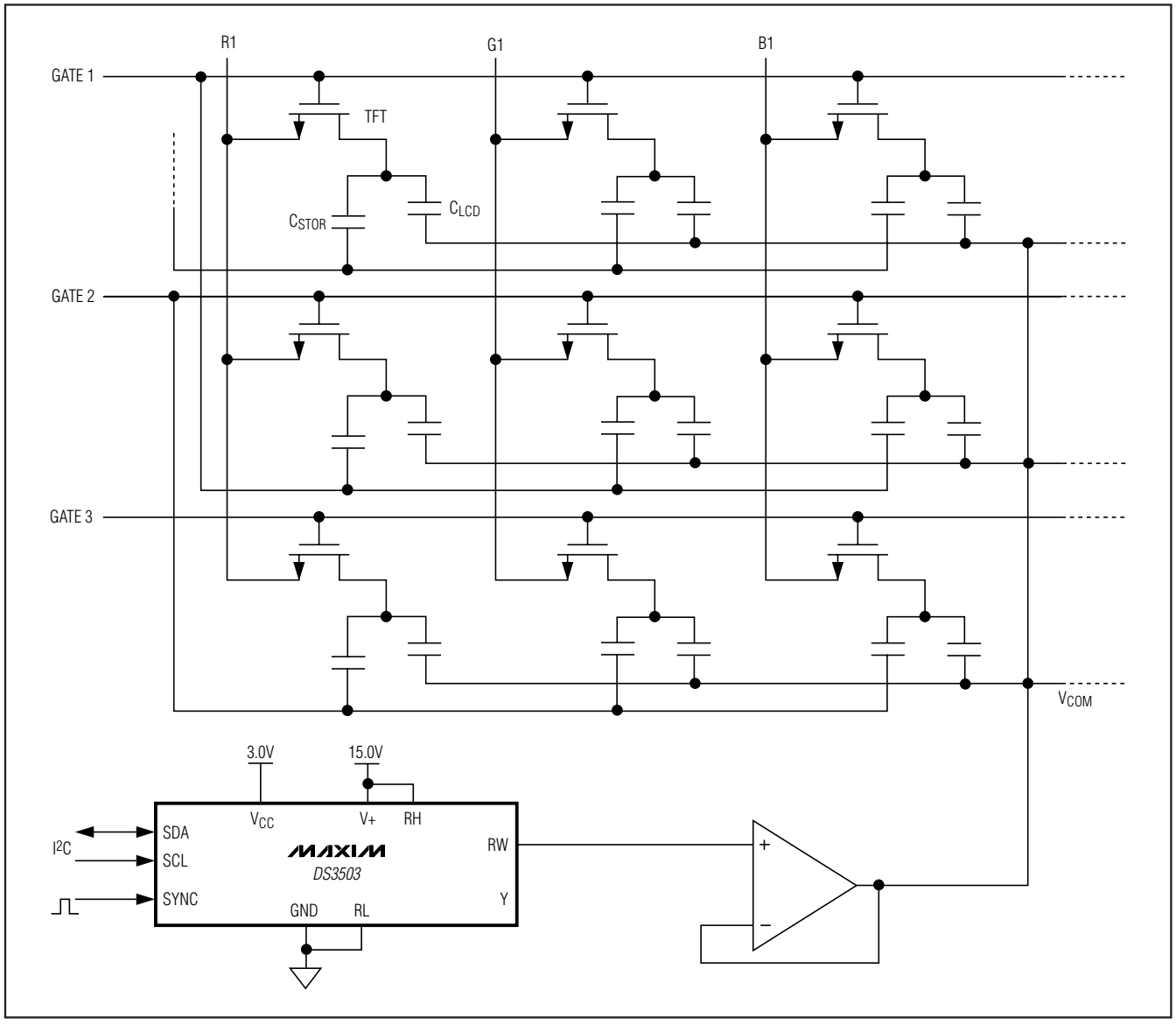
To achieve the best results when using the DS3503, decouple both the power-supply pin (V_{CC}) and the wiper-bias voltage pin (V+) with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

SDA and SCL Pullup Resistors

SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver must be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I²C AC Electrical Characteristics* are within specification. A typical value for the pullup resistors is 4.7kΩ.

NV, I²C, Stepper Potentiometer

Typical Operating Circuit



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 µSOP	U10+2	**21-0061**

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