

**Silicon NPN Power Transistors**

**BDW51C**

**DESCRIPTION**

- With TO-3 package
- Complement to type BDW52C
- Excellent safe operating area

**APPLICATIONS**

- For use in power linear and switching applications

**PINNING(see Fig.2)**

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

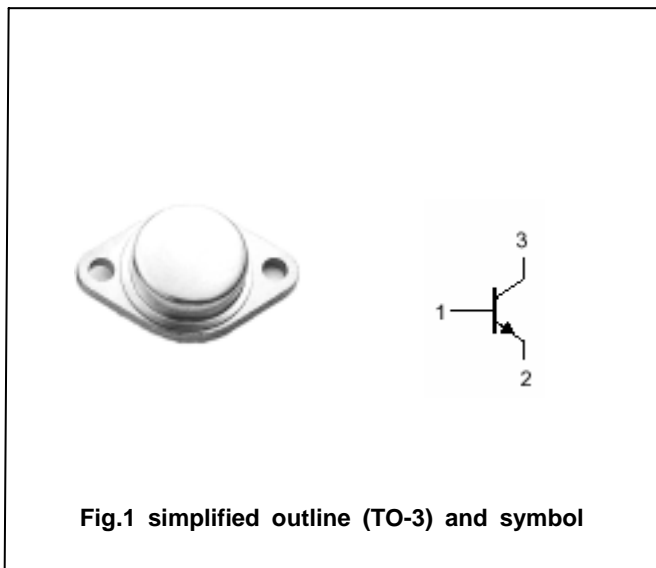


Fig.1 simplified outline (TO-3) and symbol

**Absolute maximum ratings(Ta= )**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$V_{CBO}$	Collector-base voltage	Open emitter	100	V
$V_{CEO}$	Collector-emitter voltage	Open base	100	V
$V_{EBO}$	Emitter-base voltage	Open collector	5	V
$I_C$	Collector current		15	A
$I_{CM}$	Collector current-peak		20	A
$I_B$	Base current		7	A
$P_C$	Collector power dissipation	$T_C=25$	125	W
$T_j$	Junction temperature		200	
$T_{stg}$	Storage temperature		-65~200	

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	MAX	UNIT
$R_{th\ j-c}$	Thermal resistance junction to case	1.4	/W

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## BDW51C

## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>CEO(SUS)</sub>	Collector-emitter sustaining voltage	I <sub>C</sub> =0.1A ; I <sub>B</sub> =0	100			V
V <sub>CEsat-1</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =5A; I <sub>B</sub> =0.5A			1.0	V
V <sub>CEsat-2</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =10A; I <sub>B</sub> =2.5A			3.0	V
V <sub>BEsat</sub>	Base-emitter saturation voltage	I <sub>C</sub> =10A; I <sub>B</sub> =2.5A			2.5	V
V <sub>BE</sub>	Base-emitter on voltage	I <sub>C</sub> =5A ; V <sub>CE</sub> =4V			1.5	V
I <sub>CEO</sub>	Collector cut-off current	V <sub>CE</sub> =50V; I <sub>B</sub> =0			1.0	mA
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =100V; I <sub>E</sub> =0 T <sub>C</sub> =150			0.5 5.0	mA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =5V; I <sub>C</sub> =0			2.0	mA
h <sub>FE-1</sub>	DC current gain	I <sub>C</sub> =5A ; V <sub>CE</sub> =4V	20		150	
h <sub>FE-2</sub>	DC current gain	I <sub>C</sub> =10A ; V <sub>CE</sub> =4V	5			
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =0.5A ; V <sub>CE</sub> =4V	3			MHz

PACKAGE OUTLINE

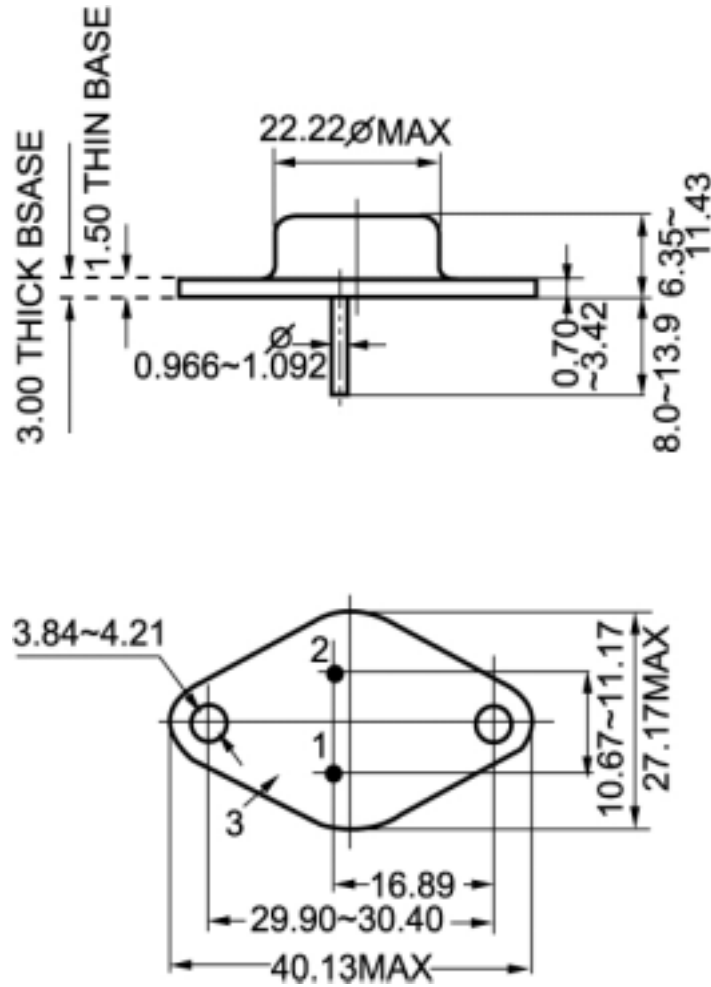


Fig.2 outline dimensions (unindicated tolerance:  $\pm 0.1\text{mm}$ )