

## General Description

The AOD407 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

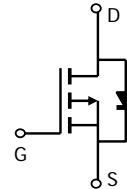
## Features

$V_{DS}$  (V) = -60V

$I_D$  = -12A ( $V_{GS}$  = -10V)

$R_{DS(ON)}$  < 115m $\Omega$  ( $V_{GS}$  = -10V)

$R_{DS(ON)}$  < 150m $\Omega$  ( $V_{GS}$  = -4.5V)



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	-12
		$T_C=100^\circ\text{C}$	-10
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-30	A
Avalanche Current <sup>C</sup>	$I_{AR}$	-12	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	23	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	50
		$T_C=100^\circ\text{C}$	25
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2.5
		$T_A=70^\circ\text{C}$	1.6
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	16.7	25	$^\circ\text{C}/\text{W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JC}$	2.5	3	$^\circ\text{C}/\text{W}$
Steady-State				
Maximum Junction-to-Case <sup>B</sup>				

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-48V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C		-0.003	-1	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.5	-2.1	-3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-12A T <sub>J</sub> =125°C		91	115	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-8A		114	150	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-12A		12.8		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.76	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-12	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-30V, f=1MHz		987	1185	pF
C <sub>oss</sub>	Output Capacitance			114		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			46		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		7	10	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge (10V)	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, I <sub>D</sub> =-12A		15.8	20	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge (4.5V)			7.4	9	nC
Q <sub>gs</sub>	Gate Source Charge			3		nC
Q <sub>gd</sub>	Gate Drain Charge			3.5		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-30V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		9		ns
t <sub>r</sub>	Turn-On Rise Time			10		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			25		ns
t <sub>f</sub>	Turn-Off Fall Time			11		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-12A, di/dt=100A/μs		27.5	35	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-12A, di/dt=100A/μs		30		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev 7 : May 2010

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

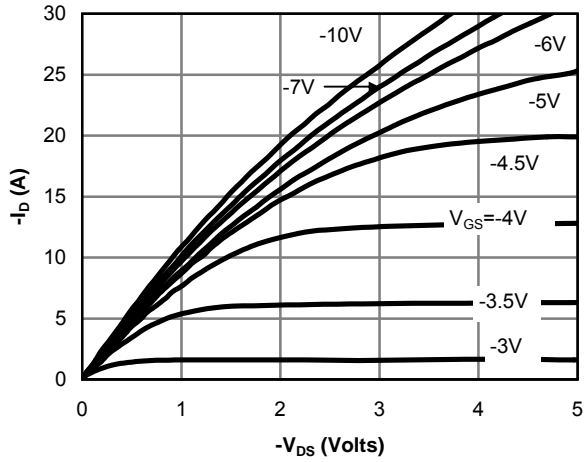


Fig 1: On-Region Characteristics

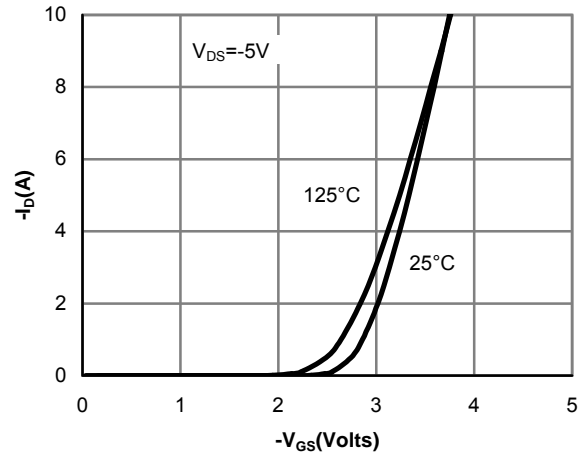


Figure 2: Transfer Characteristics

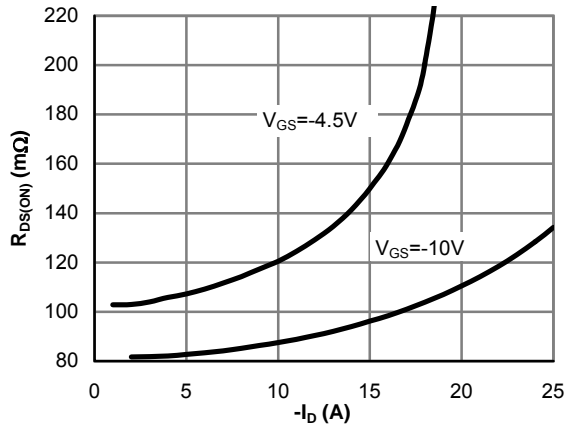


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

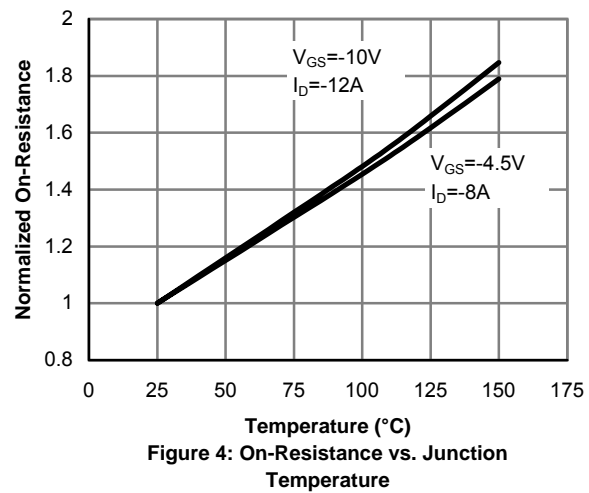


Figure 4: On-Resistance vs. Junction Temperature

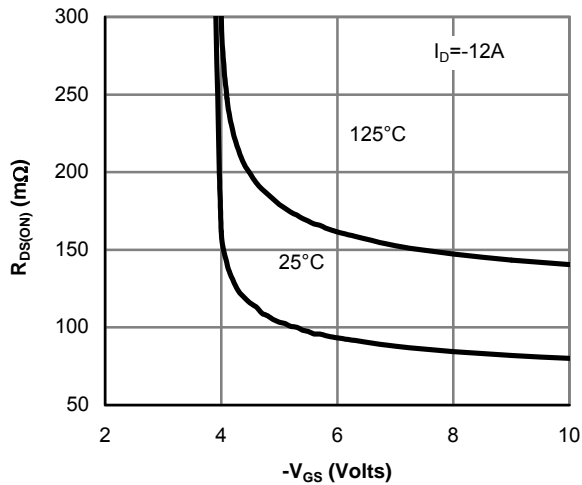


Figure 5: On-Resistance vs. Gate-Source Voltage

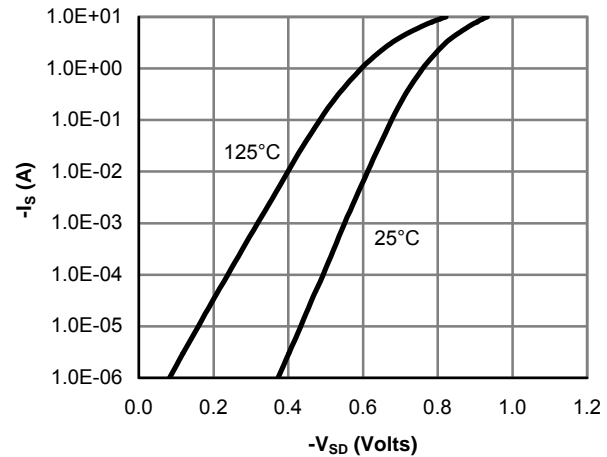


Figure 6: Body-Diode Characteristics

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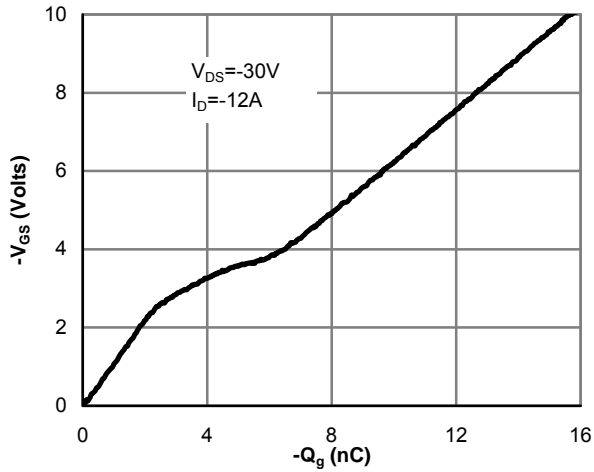


Figure 7: Gate-Charge Characteristics

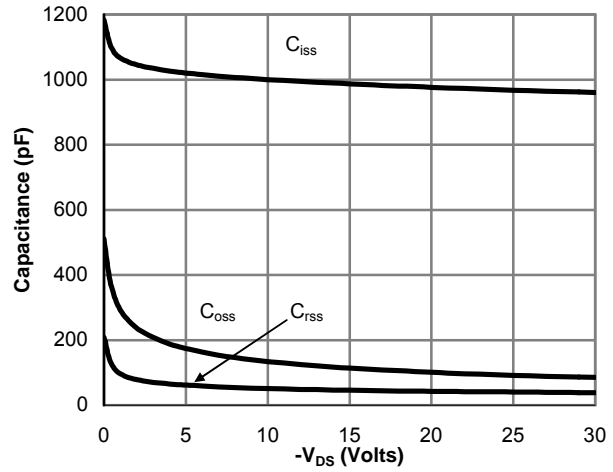


Figure 8: Capacitance Characteristics

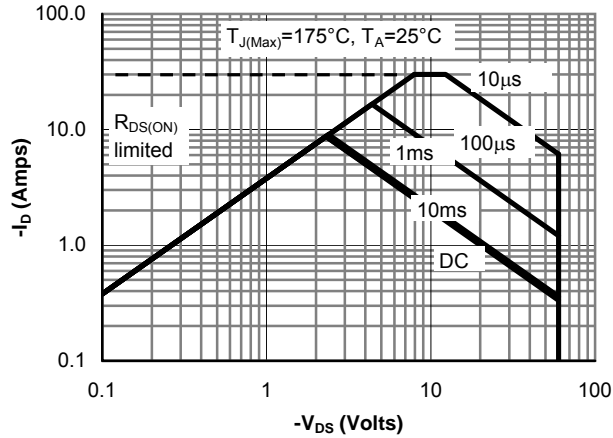


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

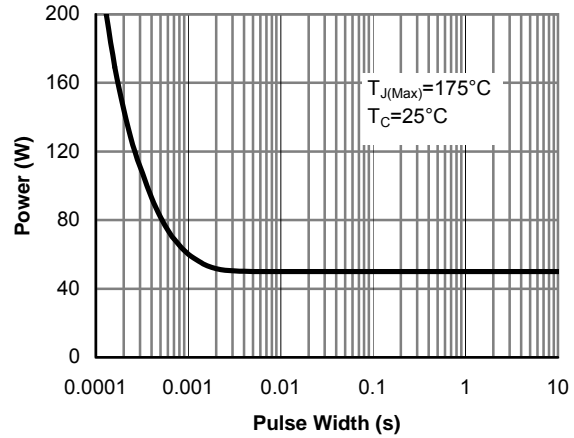


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

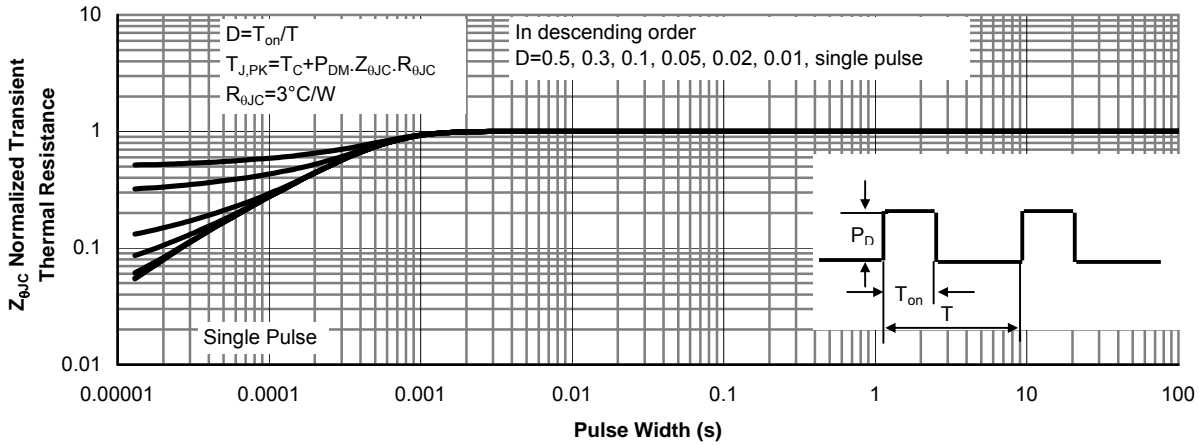


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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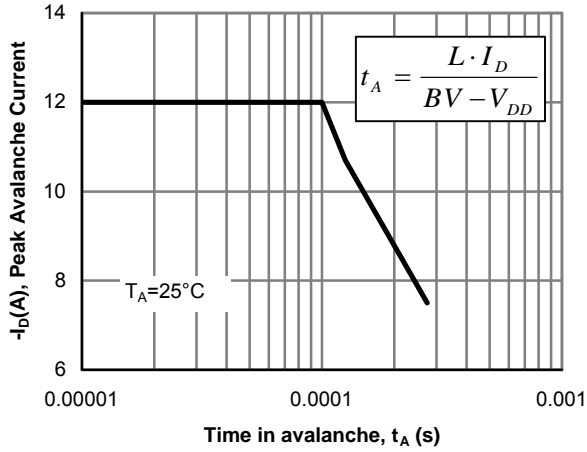


Figure 12: Single Pulse Avalanche capability

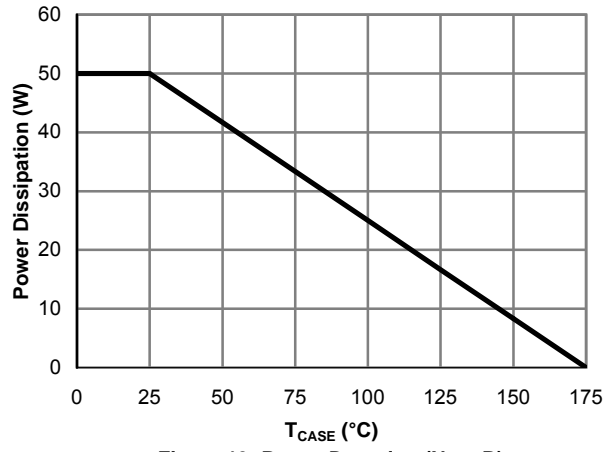


Figure 13: Power De-rating (Note B)

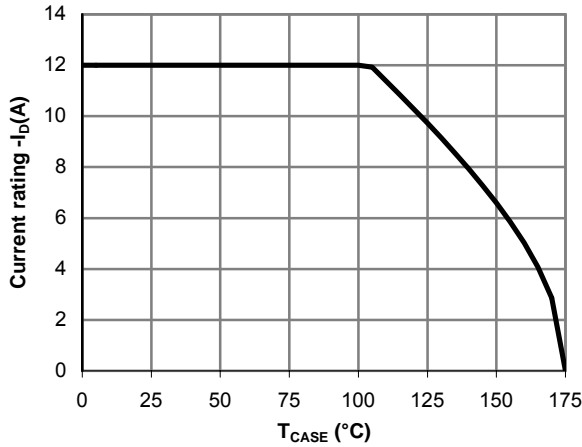


Figure 14: Current De-rating (Note B)

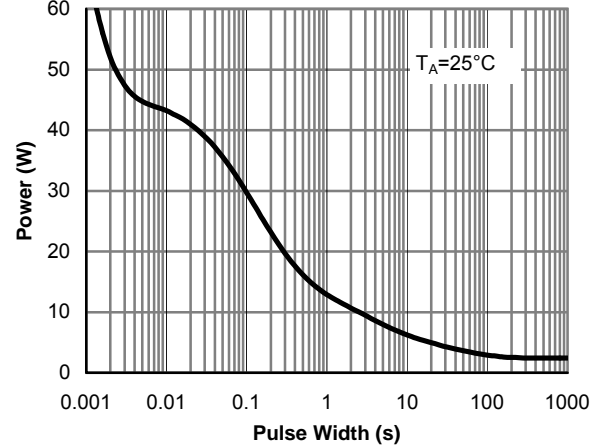


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

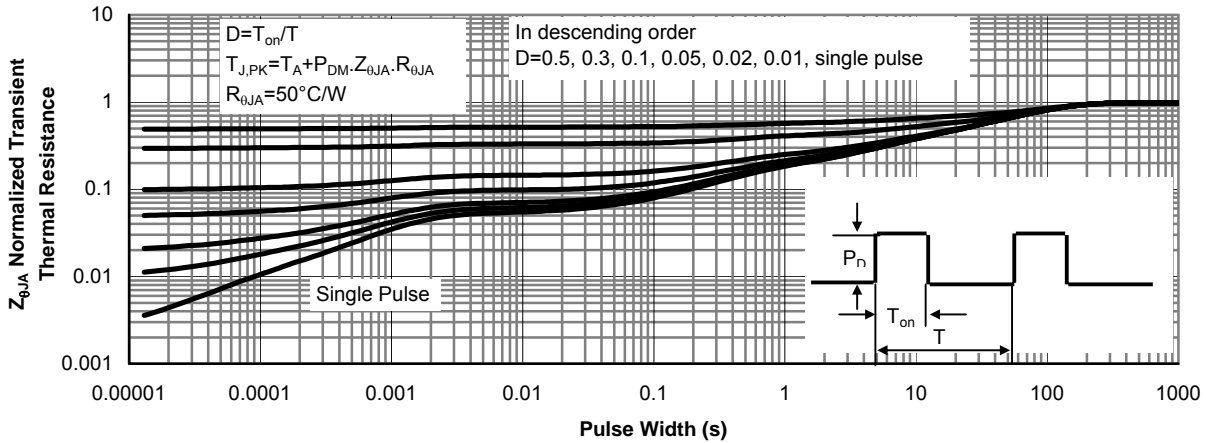
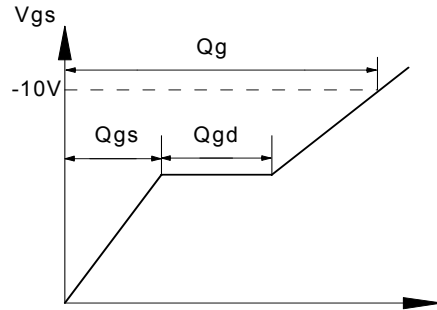
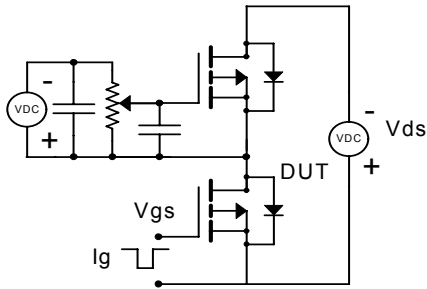
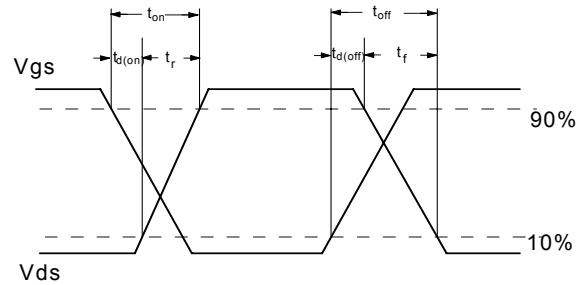
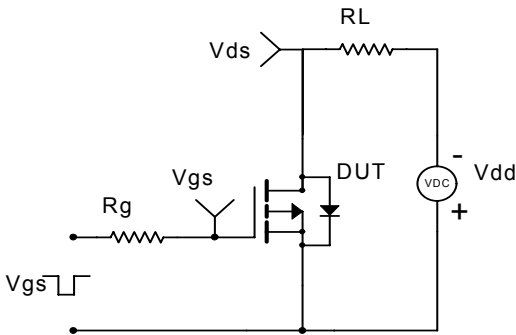


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

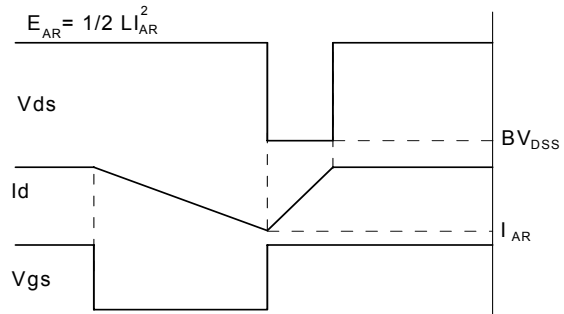
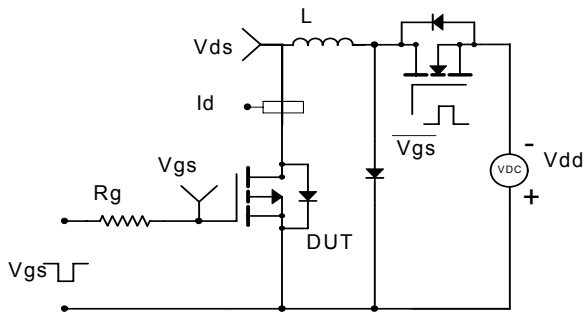
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

