

54AC11280, 74AC11280  
9-BIT PARITY GENERATORS/CHECKERST-45-17-00  
TI0117-D3201, APRIL 1989—REVISED MARCH 1990

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits Parity
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

**description**

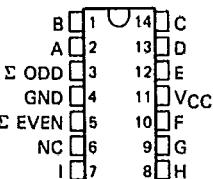
These universal nine-bit parity generators/checkers feature odd and even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading.

The 54AC11280 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11280 is characterized for operation from -40°C to 85°C.

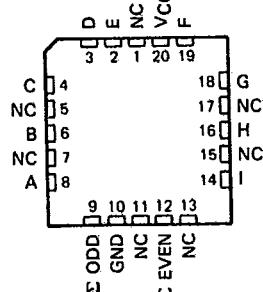
**FUNCTION TABLE**

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

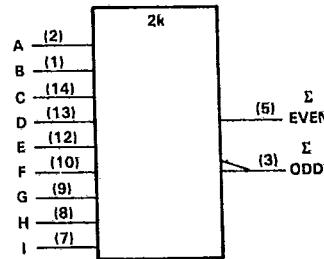
54AC11280 ... J PACKAGE  
74AC11280 ... D OR N PACKAGE  
(TOP VIEW)



54AC11280 ... FK PACKAGE  
(TOP VIEW)



NC—No internal connection

**logic symbol†**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, J, and N packages.

EPIC is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments Standard warranty. Production processing does not necessarily include testing of all parameters.

2-410

Copyright © 1990, Texas Instruments Incorporated



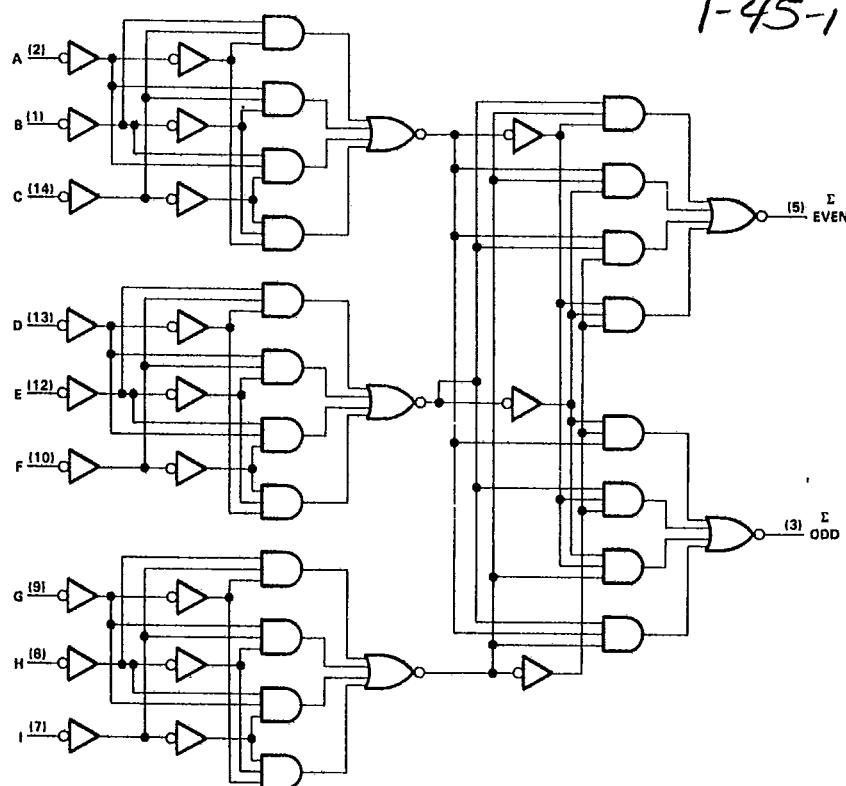
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC11280, 74AC11280  
9-BIT PARITY GENERATORS/CHECKERS

T10117—D3201, APRIL 1989—REVISED MARCH 1990

## logic diagram (positive logic)

T-45-17



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> .....	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1) .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Note 1).....	-0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> ) .....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ).....	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> ).....	±50 mA
Continuous current through V <sub>CC</sub> or GND pins .....	±100 mA
Storage temperature range .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

54AC11280, 74AC11280  
9-BIT PARITY GENERATORS/CHECKERS

T-45-17

D9201, APRIL 1989—REVISED MARCH 1990—TI0117

## recommended operating conditions

		54AC11280			74AC11280			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	3	5	5.5	3	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		2.1			V
		V <sub>CC</sub> = 4.5 V	3.15		3.15			
		V <sub>CC</sub> = 5.5 V	3.85		3.85			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V	0.9		0.9			V
		V <sub>CC</sub> = 4.5 V	1.35		1.35			
		V <sub>CC</sub> = 5.5 V	1.65		1.65			
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V	-4		-4			mA
		V <sub>CC</sub> = 4.5 V	-24		-24			
		V <sub>CC</sub> = 5.5 V	-24		-24			
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V	12		12			mA
		V <sub>CC</sub> = 4.5 V	24		24			
		V <sub>CC</sub> = 5.5 V	24		24			
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C		

PRODUCT PREVIEW Information concerns products in the formative stages of development. Characteristics data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

TEXAS  
INSTRUMENTS  
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC11280, 74AC11280

## 9-BIT PARITY GENERATORS/CHECKERS

T-45-17

TI0117—D3201, APRIL 1989—REVISED MARCH 1990

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54AC11280		74AC11280		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.4		2.48		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.7		3.8		
	I <sub>OH</sub> = -50 mA†	5.5 V	4.94			4.7		4.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	3 V				3.85				V
		4.5 V								
		5.5 V								
	I <sub>OL</sub> = 12 mA	3 V		0.36		0.5		0.44		
	I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5		0.44		
	I <sub>OL</sub> = 50 mA†	5.5 V		0.36		0.5		0.44		
I <sub>I</sub>	I <sub>OL</sub> = 75 mA†	5.5 V				1.65				µA
	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1		±1		
	I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8	160		80		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3.5						pF

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

PRODUCT PREVIEW information concerns products in the  
formative or design phase of development. Characteristics data  
and other specifications are design goals. Texas Instruments  
reserves the right to change or discontinue these products  
without notice.



POST OFFICE BOX 656303 • DALLAS, TEXAS 75265

54AC11280, 74AC11280  
9-BIT PARITY GENERATORS/CHECKERS

T-45-17

D3201, APRIL 1989—REVISED MARCH 1990—TQ1117

switching characteristics  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ , (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11280		74AC11280		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	Any input	EVEN	1.5	9.8	13.5	1.5	15.7	1.5	14.9	ns
			1.5	10.5	13.9	1.5	16.2	1.5	15.4	
$t_{PLH}$	Any input	ODD	1.5	9.9	13.8	1.5	16	1.5	15.1	ns
			1.5	10.6	14.4	1.5	16.7	1.5	15.6	

switching characteristics  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ , (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11280		74AC11280		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	Any input	EVEN	1.5	5.9	9.1	1.5	10.6	1.5	10.1	ns
			1.5	6.7	9.9	1.5	11.5	1.5	10.9	
$t_{PHL}$	Any input	ODD	1.5	6	9.3	1.5	10.8	1.5	10.3	ns
			1.5	6.8	10.3	1.5	11.7	1.5	11.1	

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS			TYP	UNIT
	$C_L = 50 \text{ pF}$	$f = 1 \text{ MHz}$			
$C_{pd}$ Power dissipation capacitance				68	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

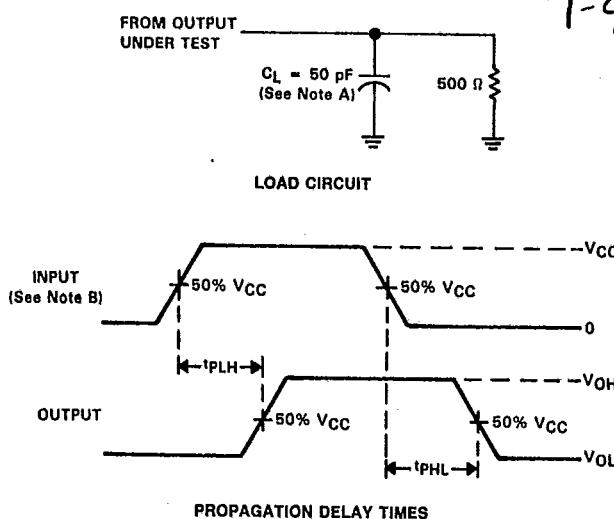
2-414

TEXAS  
INSTRUMENTS  
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

54AC11280, 74AC11280  
9-BIT PARITY GENERATORS/CHECKERS

T0117-D3201, APRIL 1989—REVISED MARCH 1990

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_0 = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS