CALMOS™

CA408/CA411

FM RECEIVER CHIP SET FOR DATA

T-75-90

- Wide supply voltage range 1.8 – 6.0 volts
- Single cell operation down to 0.9 volts using external inverter and on-chip regulator circuitry
- Strobed operation for prolonged battery life
- Low power consumption
  - 0.25 mW standby
  - 4.2 mW strobed ON
- Input frequency to 200MHz
- 0.5 μV typical sensitivity
- RF and mixer stage currents limited under high signal conditions
- Selectivity attained with active filters using on-chip amplifiers and external R-C components
- Bias currents derived from bandgap reference for supply rejection and temperature compensation
- Battery monitor comparator
- CMOS compatible control and logic interface

The CA408/CA411 chip set is a low power radio receiver for FM data transmission systems. Receiver simplicity and cost efficiency are achieved by using a direct conversion technique that converts VHF directly to audio.

The chip set operates over a supply voltage range of 1.8 – 6.0V. An inverter option allows the system to run off a single battery cell down to 0.9V. A battery economy pin powers down the circuits to extend battery life.

System input is FSK modulated RF to 200MHz. The incoming signal is divided into 2 channels where it is mixed in quadrature with the carrier frequency generated by a local oscillator. The mixer output signals are separated in phase by 90° and are at a frequency equal to the deviation of the incoming signal. They are then lowpass filtered to provide channel selectivity. A phase comparator/limiter detects the transmitted data and outputs it.

The CA408 contains an RF amplifier, local oscillator, and two mixers. The CA411 contains two operational amplifiers and two unity gain amplifiers for active filtering, two limiting IF amplifiers, detection logic and data output drive circuitry. The CA411 also contains a low battery flag, and a strobed, regulated 1V rail.

Applications include FM data transmission, radio pagers, security systems and radio link code-key systems.

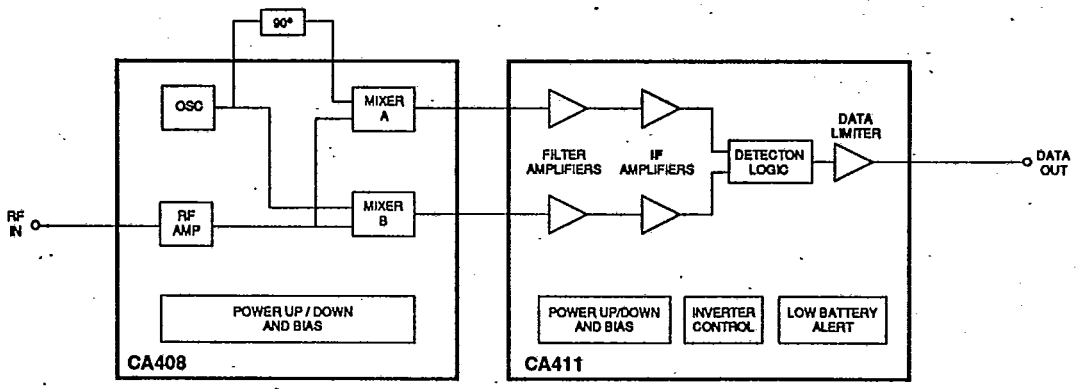

Figure 1 : CA408/CA411 CHIP SET BLOCK DIAGRAM

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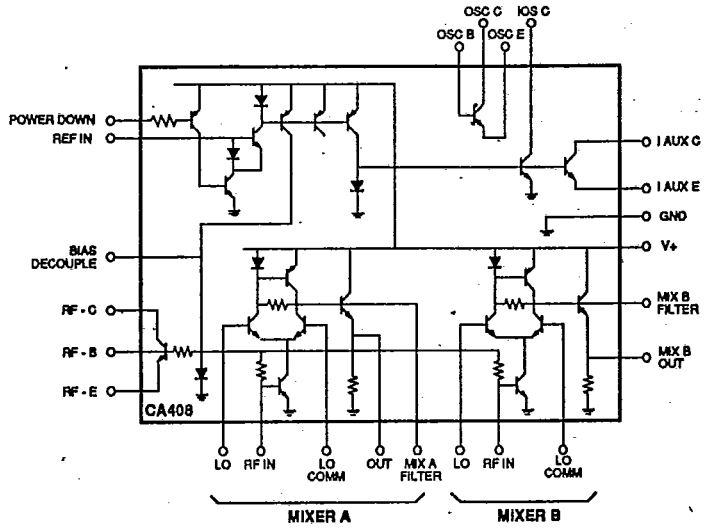

Figure 2 : CA408 BLOCK DIAGRAM

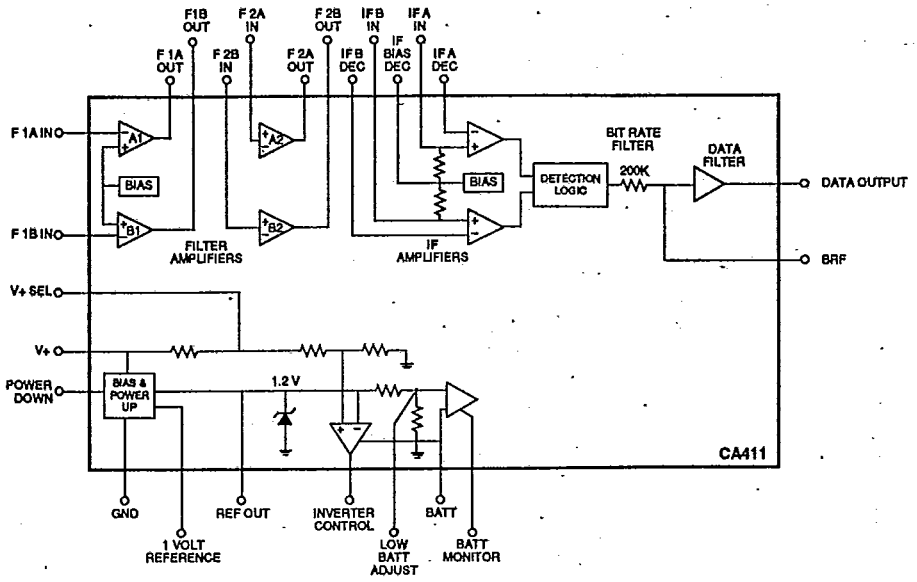

Figure 3 : CA411 BLOCK DIAGRAM

1	MIXER A COMMON	13	MIXER A IN-
2	MIXER A LO	14	GND
3	OSCILLATOR B	15	MIXER B IN
4	OSCILLATOR C	16	V+
5	OSCILLATOR E	17	POWER DOWN
6	I OSCILLATOR	18	REFERENCE IN
7	I AUX C	19	MIXER B FILTER
8	I AUX E	20	MIXER A FILTER
9	RF BASE	21	MIXER B OUT
10	RF EMITTER	22	MIXER A OUT
11	RF OUT	23	MIXER B LO
12	BIAS DECOUPLE	24	MIXER B COMMON

a) CA408 L–24

1	F1B OUT	13	F1A OUT
2	F2B IN	14	F1A IN
3	F2B OUT	15	V+
4	IF B IN	16	V+ SEL
5	IF B DECOUPLE	17	BATTERY MONITOR
6	DATA OUT	18	INV CTRL
7	BRF	19	REFERENCE OUT
8	BIAS DECOUPLE	20	BATTERY
9	IF A DECOUPLE	21	POWER DOWN
10	IF A IN	22	1 VOLT REFERENCE
11	F2A OUT	23	GND
12	F2A IN	24	F1B IN

b) CA411 L–24

1	I AUX E	15	MIXER A FILTER
2	N/C	16	MIXER B OUT
3	RF BASE	17	MIXER A OUT
4	N/C	18	N/C
5	RF EMITTER	19	MIXER B LO
6	RF OUT	20	MIXER B COMMON
7	BIAS DECOUPLE	21	MIXER A COMMON
8	MIXER A IN	22	MIXER A LO
9	GND	23	N/C
10	MIXER B IN	24	OSCILLATOR B
11	V+	25	OSCILLATOR C
12	POWER DOWN	26	OSCILLATOR E
13	REFERENCE IN	27	I OSCILLATOR
14	MIXER B FILTER	28	I AUX C

c) CA408 N–28

1	BRF	15	POWER DOWN
2	BIAS DECOUPLE	16	N/C
3	IF A DECOUPLE	17	N/C
4	IF A IN	18	N/C
5	F2A OUT	19	1 VOLT REFERENCE
6	F2A IN	20	N/C
7	F1A OUT	21	GND
8	F1A IN	22	F1B IN
9	V+	23	F1B OUT
10	V+ SEL	24	F2B IN
11	BATTERY MONITOR	25	F2B OUT
12	INV CTRL	26	IF B IN
13	REFERENCE OUT	27	IF B DECOUPLE
14	BATTERY	28	DATA OUT

d) CA411 N–28

1	I AUX E	16	MIXER A FILTER
2	N/C	17	MIXER B OUT
3	N/C	18	MIXER A OUT
4	RF BASE	19	N/C
5	RF EMITTER	20	MIXER B LO
6	RF OUT	21	MIXER B COMMON
7	BIAS DECOUPLE	22	MIXER A COMMON
8	MIXER A IN	23	MIXER A LO
9	GND	24	N/C
10	MIXER B IN	25	OSCILLATOR B
11	V+	26	OSCILLATOR C
12	N/C	27	OSCILLATOR E
13	POWER DOWN	28	N/C
14	REFERENCE IN	29	I OSCILLATOR
15	MIXER B FILTER	30	I AUX C

e) CA408 30–LEAD VINSON QUILL

1	BIAS DECOUPLE	16	N/C
2	IF A DECOUPLE	17	N/C
3	IF A IN	18	N/C
4	F2A OUT	19	1 VOLT REFERENCE
5	F2A IN	20	N/C
6	F1A OUT	21	N/C
7	F1A IN	22	GND
8	V+	23	F1B IN
9	V+ SEL	24	F1B OUT
10	BATTERY MONITOR	25	F2B IN
11	INV CTRL	26	F2B OUT
12	REFERENCE OUT	27	IF B IN
13	BATTERY	28	IF B DECOUPLE
14	POWER DOWN	29	DATA OUT
15	N/C	30	BRF

f) CA411 30–LEAD VINSON QUILL

Figure 4 : CA408 and CA411 PINOUT DIAGRAMS for DIFFERENT PACKAGE CONFIGURATIONS

Table 1 : CA408 ELECTRICAL CHARACTERISTICS
(V+ = Full range, 47K from 1.22V to REFERENCE IN to give I_R = 10μA nominal. T_A = 20°C unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range V+		1.8		6	V
Supply Current OFF	I (V+)		0	2	μA
(POWER DOWN *high*)	I (RF OUT) @ 1 volt		0	2	μA
	I (OSCILLATOR) @ 1 volt		0	2	μA
	I (AUX C) @ 1 volt, AUX E @ GND		0	2	μA
Supply Current ON	I (V+)		1030	1200	μA
(POWER DOWN *low*)	I (RF OUT) @ 1 volt		500	600	μA
	I (OSCILLATOR) @ 1 volt		250	285	μA
	I (AUX C) @ 1 volt, AUX E @ GND		250	285	μA
RF Stage	Bias Current[1] : RF EMITTER @ 0V, RF OUT @ 1V	42.5	50	57.5	x I_R
	Bias Resistor: RF BASE to BIAS DECOUPLE	1.4	2	2.6	KΩ
	HFE	50		300	
Mixers	Bias Current (Note 1)	21	25	29	x I_R
	Bias Resistor: RF IN to BIAS DECOUPLE	2.8	4	5.2	KΩ
	LO Input Bias Current @ 1.5V			4	μA
	LO Input Common Mode Range	0.9		V+-0.7	V
	Source Resistance for MIXER A/B FILTERS	5.6	7.5	9.3	KΩ
	Mixer Out - DC Level		V+-1.4		V
	Signal swing	0.6			Vp-p
	Follower bias (Note 1)	2	2.5	3	x I_R
	Conversion Gain with V(LO) = 30mV RMS @ 150 MHz V(RF) = 1mV @ 150.005 MHz		24		dB
Local Oscillator	Bias[1] : I OSC @ 1V	22.5	25	27.5	x I_R
	NPN HFE	50		300	
	Schottky Clamp VCB @ IC-B = 100μA			0.5	V
Power Down	V_{IH}	V+-0.3			V
	V_{IL}			0.3	V
	I_{IH} @ V_I = V+-0.2V	-1		+1	μA
	I_{IL} @ V_I = 0.2V	-4		-7.5	μA
Auxilliary Current Source	I (AUX C) at 1 volt with AUX E at GND (Note 1)	22.5	25	27.5	x I_R

Notes:

1. Bias currents are proportional to reference current I_R set by external resistor R7 (Figure 8). I_R is derived from V (bandgap) – V_{BE} and hence is proportional to absolute temperature.
2. Operating temperature range is: -20° to +60°C

Table 2 : CA411 ELECTRICAL CHARACTERISTICS
(V+ and BATTERY = Full range, POWER DOWN @ GND, T_A = 20°C unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range	BATTERY	0.9		6	V
	V+	1.8		6	V
Supply Current	OFF (POWER DOWN *high*)				
	I Battery @ 1.3V		35	50	µA
(V+ SEL s/c to V+,	I (V+) @ 2.4V		90	125	µA
Inverter not connected)	ON (POWER DOWN *low*)				
	I (BATTERY) @ 1.3V		35	50	µA
	I (V+) @ 2.4V		380	550	µA
Filter Amplifiers A1, B1	Input Bias Current		0.3	0.5	µA
	Output DC Level (unity DC gain)		V+–1.3		V
	Output swing RL = 20KΩ	0.6	0.8		Vp-p
	Output current sink capability	30	50		µA
	DC Open Loop Gain: RL = 20KΩ	60			dB
	Gain bandwidth	1			MHz
	Equivalent input noise @ pts C & D				
	in Figure 8		6		µVrms
Filter Amplifiers A2, B2	Voltage Gain (RL = 50KΩ)		1		
	Input Voltage Range	0.2		V+–0.8	V
	Input Bias Current		0.1	0.5	µA
	Input to Output Offset	–0.1		+0.1	V
	Output Resistance, I/P @ V+ = –1.3V		1.0	1.5	KΩ
	Output Current Sink Capability	15	25		µA
Limiting Amplifiers	Input Impedance (with respect to				
IF-A, IF-B	BIAS DECOUPLE)	35	50	65	KΩ
	Input DC Level at BIAS DECOUPLE		V+–0.74		V
	Input Limiting Threshold			10	µVrms
Bit Rate Filter	Source Resistor	140	200	280	KΩ
	Data Swing at BRF Pin into O/C				
	High		1.2		V
	Low		0.1	0.15	V
Data Out Buffer	Input Switching Threshold			0.6	V
	Output Levels				
	Low: V (BRF) = 0.8V, I_{OL} = 5µA			0.3	V
	High: V (BRF) = 0.4V, I_{OH} = 2µA	V+–0.3			V
	OFF state output level				
	POWER DOWN @ V+, I_{OH} = 2µA	V+–0.3			V
Reference	VREF with external 10µA load	1.17	1.22	1.27	V

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Table 2 : CA411 ELECTRICAL CHARACTERISTICS (con't)

Parameter	Condition	Min	Typ	Max	Units
POWER DOWN	V_{IH}	1.5			V
	V_{IL}		0.3	V	
	I_{IH} @ V_I = 1.8V	–8		–3	µA
	I_{IL} @ V_I = 0.2V	–8		–3	µA
BATTERY MONITOR	Switching Threshold: V Battery		1.05		V
	Output Levels				
	Low: V (BATTERY) < 1.0V, I_{OL} = –10µA		0.3	V	
	High: V (BATTERY) > 1.1V, I_{OH} = 2 µA	V+–0.3			V
Low Battery Threshold Adjust	Threshold Voltage		1.05		V
	Source Resistance	22	32	44	KΩ
Inverter Control Regulator	INV CTRL: Output swing	0		0.6	V
	Pull down resistor	11	15	20	KΩ
Transconductance	V+ = 2.2V, V+ SEL, S/C to V+, INV CTRL at 0V: d (I (INV CTRL) /d (V+))	–0.4	–3		mmhos
INV CTRL Output Levels	V+ SEL S/C to V+				
	V (INV CTRL) with V+ = 2.4V		0	0.1	V
	V (INV CTRL) with V+ = 2.0 V	0.5	0.7		V
	V+ SEL O/C				
	V (INV CTRL) with V+ = 3.3V		0	0.1	V
	V (INV CTRL) with V+ = 2.7V	0.5	0.7		V

Note: Operating temperature range is: –20° to +60°C

Table 3 : ABSOLUTE MAXIMUM RATINGS (CA408 and CA411)

Input Voltage	6 V
Storage Temperature Range	–65° to +150°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The direct conversion system operates by routing the FSK input into two signal processing channels with the channel inputs separated in phase by 90°. Each channel is made up of a mixer, a lowpass filter and a limiting IF amplifier.The input signals are mixed with the output of a local oscillator that runs at the carrier frequency, so that the IF is DC. The lowpass filters provide channel selectivity. The low frequency signals out of the lowpass filters are fully limited in the IF amplifiers such that their outputs can be regarded as digital waveforms. These are digitally demodulated by a phase detector to give output data in NRZ format.

The direct conversion approach minimizes image and IF-related spurious responses. Also, most of the gain required is at low frequencies resulting in low power consumption and non-demanding stability considerations. Thus, the external components required includes no crystal or ceramic filters and a minimum number of coils. In addition, no IF tuning is needed.

Signal Path

The incoming RF signal (see Figure 8) is coupled to the base of the RF amplifier transistor through C1. L1 and C2 make up the load tuned to 150 MHz. R2/C4/C5 provide a decoupled supply for the RF amplifier. C3 couples the signal out of the RF amplifier directly to the mixers.

The local oscillator is a grounded base seventh overtone configuration tuned to the RF carrier frequency. Base bias and decoupling are provided by R3 and C6. Capacitive tap C7/C8 in the tank circuit is for impedance transformation and to provide a phase lead to compensate for phase lag through the transistor. L3 is chosen to be anti-resonant with the capacitance of the crystal at 150 MHz. L2 is to compensate for rolloff of output impedance of the constant current source transistors.

A LO transistor is provided on the CA408, although it is not connected in Figure 8, because of possible signal interference problems. For lower frequency or lower performance applications the on-chip LO transistor can be used .

The signal out of the LO is coupled to the quadrature network through transformer T1. A phase lead of 45° at 150 MHz is provided by C9/R4 while a phase lag of 45° is provided by R5/C10, thereby phase separating by 90° the input signals to the two double balanced mixers. R6/C11 provide balanced input terminations for the mixers.

The lowpass filter configuration (and response) for one signal channel is shown in Figure 5, (the second channel is identical). The lowpass filter must pass the maximum FSK frequency deviation of 5 kHz while attenuating adjacent (25 kHz) channel signals by about 70 dB. Signals from adjacent channels must be attenuated sufficiently such that they cannot limit the IF amplifiers.

The detection logic is a digital phase comparator. DATA OUT is a 1 if channel B leads channel A, and a 0 if A leads B. The cutoff frequency in Hz of bit rate filter (BRF) R30/C36 should be approximately 0.6 times the data rate in bps, for example 300 Hz for 512 bps.

Stage gains are controllable through external components up to the inputs of the IF amplifiers. The voltage gains for the application in Figure 8 are: RF amplifiers 10 dB, Mixers 24dB and Active filters 6 dB. This gain distribution is considered to be close to optimum.

The input sensitivity of the receiver of Figure 8 is 0.5 µV typical for a data error rate of 1 in 1000.

Other Features

Both the CA408 and CA411 have POWER DOWN pins. A *one* on the POWER DOWN pin places the chip in the low power mode. The 1 VOLT REFERENCE bias rail is powered up and down under the control of the POWER DOWN input pin.

The BATTERY MONITOR pin on the CA411 is a low battery flag that goes low if the battery voltage falls below 1.05 V.

Power Supply and Bias

The CA408 has one V+ pin and one ground pin. The CA411 has multiple V+, battery and ground pins that are explained below. Each chip has a POWER DOWN pin.

Bias currents on the CA408 are derived from an external reference current applied to REFERENCE IN. This current can conveniently be provided by connecting an external resistor from the silicon bandgap reference voltage REFERENCE OUT of the CA411 to the REFERENCE IN of the CA408. The bias currents will then have a positive temperature coefficient to temperature compensate the RF and mixer stage gains. The external resistor allows tight control of RF, mixer and oscillator bias currents.

In the Power Down mode, the CA408 is completely switched off. The following circuitry on the CA411, however, remains powered:

- Limiting amplifiers IFA and IFB
- DATA OUT pull-up current source
- Bandgap reference (REFERENCE OUT)
- BATTERY MONITOR
- Alert driver input circuitry
- Power up circuitry

The CA411 has the following power supply and ground connections:

BATTERY	General battery
POWER BATTERY	Battery to ALERT outputs
V+	General V+
GND	General ground

Inverter

The inverter is a simple blocking oscillator made up of Q1, Q2, D1, T2, R15, R16, C25, C26 and L3. A feedback loop that includes circuitry on the CA411 and transistor Q2 regulates V+ at a multiple of the bandgap reference voltage. V+ is regulated to 3.0 volts if the V+ SEL pin is left open, and to 2.2 volts if V+ SEL pin is shorted to V+.

Inverter waveforms are shown in Figure 6. Assume that Q1 has just turned ON. It remains in saturation as its collector current increases linearly with time. Base current drive to Q1 is present because the end of R15 connected to the 1:1 inverting pulse transformer (node B) is *high*. A portion of potential base current drive to Q1 is diverted to ground through regulating transistor Q2. The amount of current conducted by Q2 depends strongly on voltage such that Q2 can be thought of as a voltage clamp on the Vbe of Q1.

At some time the collector current of Q1 increases to the point where the available base current can no longer hold Q1 in saturation. Collector current stops increasing, collector voltage moves positive as Q1 comes out of saturation, and point B pulses negative. Q1 is quickly turned OFF by regenerative action.

To maintain the current flowing in the transformer and node common to the transformer, Q1 collector and D1 anode (node A) pulses *high* so that diode D1 conducts. Current that decreases linearly with time flows through the transformer and through D1 onto charge storage capacitor C26. The voltage ripple on C26 is removed with lowpass filter L3/C25. When the transformer current falls to zero and momentarily stabilizes, point B rings positive to the battery voltage so that Q1 is again turned on.

Figure 7 shows a simplified schematic of the CA411 inverter control circuit. The regulator amplifier compares an attenuated sample of V+ with REFERENCE OUT and drives the Inverter Control pin (INV CTRL) through a PNP output stage. A start oscillator is enabled for V+ < BATTERY to guarantee that a blocking oscillator such as the one shown in Figure 8 will start under all conditions.

Single Supply Operation

If supply voltage greater than 1.8 volts is available, the chip set can be operated from that single supply connected to V+. The inverter pins are left open. The CA411 BATTERY pin is left open and a 510 KΩ resistor is connected between V+ and REFERENCE OUT. These conditions assure full operation at specified supply currents.

Table 4 : CA411 FUNCTION TABLE

POWER DOWN Input (also applies to CA408)	0	Active Mode
	1	Power Down Mode
BATTERY MONITOR Output	0	Battery Low
	1	Battery Okay

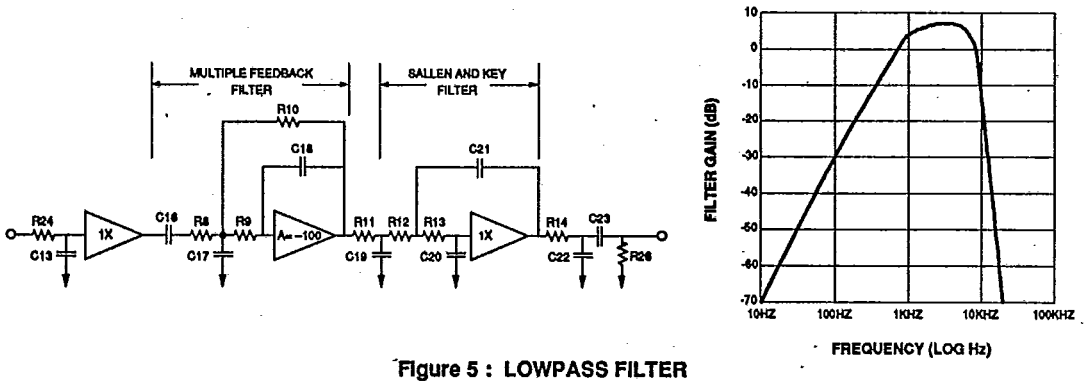


Figure 5 : LOWPASS FILTER (SCHEMATIC AND FREQUENCY CHARACTERISTICS)

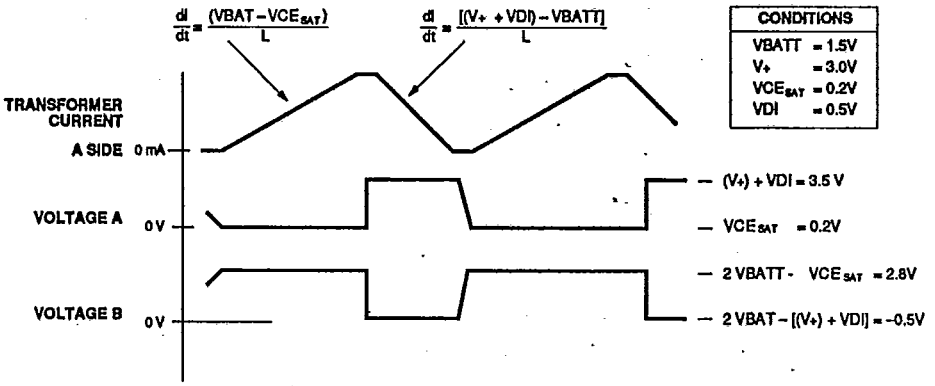


Figure 6 : INVERTER WAVEFORMS

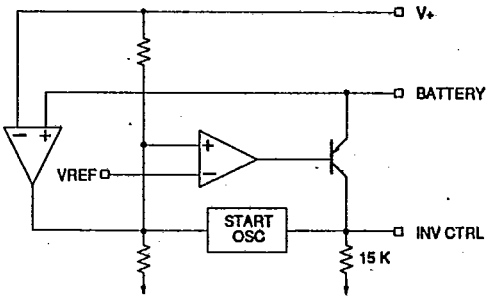
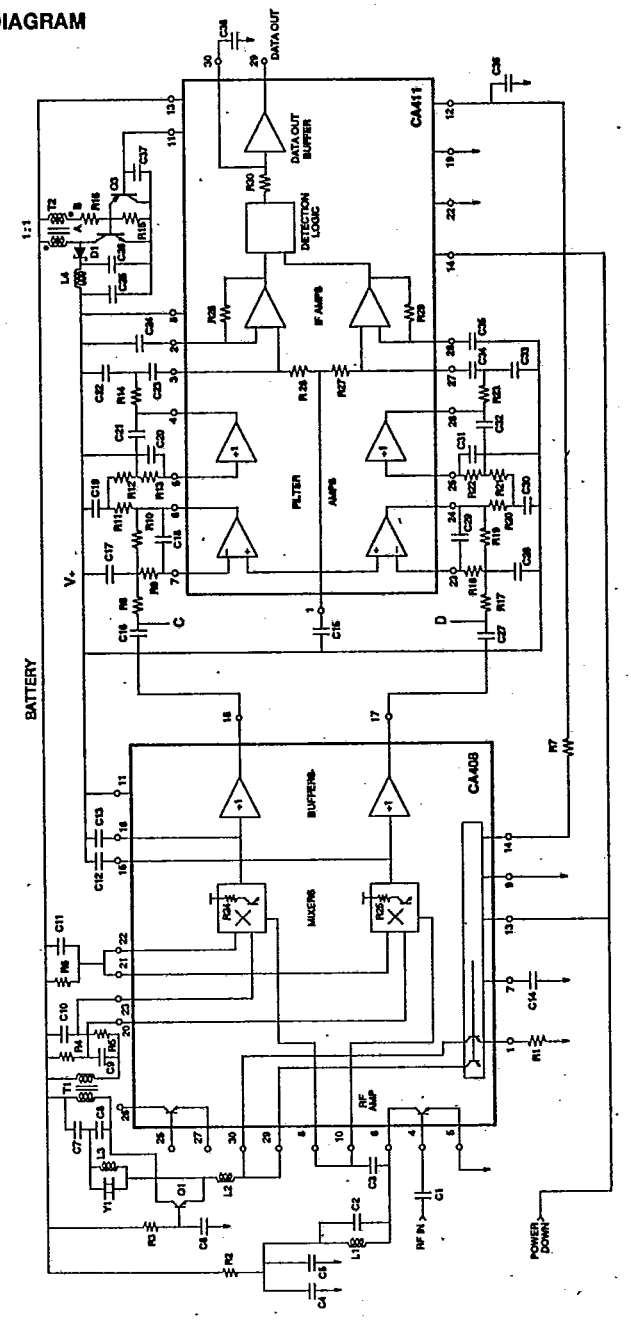


Figure 7 : INVERTER CONTROL CIRCUIT

APPLICATION DIAGRAM



Note: Pin numbers correspond to 30 – lead Vinson Quill package

RFCarrier Frequency :	150 MHz	Frequency Deviation :	±5 KHz
Channel Spacing :	25 KHz	Data Rate :	512 BPS

Figure 8 : CA408/CA411 DATA RECEIVER and TEST CIRCUIT

Table 5: COMPONENT VALUES for APPLICATION SCHEMATIC (Figure 8)

#	Value	#	Value	#	Value	#	Value	#	Value
R1	To trim I OSC	R21	24K	C10	5.6 pF	C29	180 pF	Q1	NPN 2N6429
R2	100 Ω	R22	47K	C11	10 pF	C30	4.7 nF	Q2	PNP 2N5087
R3	750 Ω	R23	10K	C12	1.8 nF	C31	390 pF	Q3	NPN 2N918
R4	180 Ω	R24	7.5K (on-chip)	C13	1.8 nF	C32	1.0 nF		
R5	180 Ω	R25	7.5K (on-chip)	C14	10 nF	C33	2.7 nF		
R6	100 Ω	R26	50K (on-chip)	C15	10 µF	C34	2.7 nF		
R7	47K	R27	50K (on-chip)	C16	27 nF	C35	10 µF		
R8	5.6K	R28	200K (on-chip)	C17	10 nF	C36	2.2 nF		
R9	13K	R29	200K (on-chip)	C18	180 pF	C37	0.1 µF		
R10	20K	R30	200K (on-chip)	C19	4.7 nF	C38	10 µF		
R11	5.6K	C1	0.001 µF	C20	390 pF	L1	50 nH ± 10 nH	(TOKO 5K Series	
R12	24K	C2	22 pF	C21	1.0 nF			294SN-A057HM)	
R13	47K	C3	100 pF	C22	2.7 nF	L2	1 µH	(Coilcraft ss163-25)	
R14	10K	C4	10 nF	C23	2.7 nF	L3	0.30 µH	(Coilcraft ss163-12)	
R15	12K	C5	10 µF	C24	10 µF	L4	100 µH	(Coilcraft ss165-24)	
R16	27K	C6	470 pF	C25	10 µF	T1	Transformer	(TOKO 2945N-0199AQ)	
R17	5.6K	C7	18 pF	C26	10 µF	T2	Inverter Toroid	(INDIANA GEN F867-1-06)	
R18	13K	C8	10 pF	C27	27 nF	D1	Schottky Diode	(IN5817)	
R19	20K	C9	5.6 pF	C28	10 nF	Y1	Crystal	(TOYOCOM UM5 or UM1)	
R20	5.6K								

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