PRELIMINARY

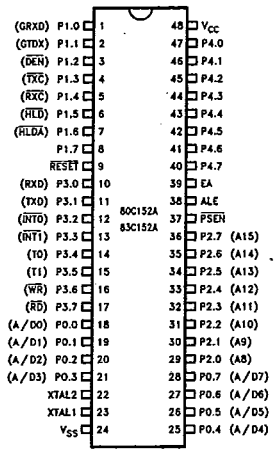
T-52-33-05

83C152A
UNIVERSAL COMMUNICATION CONTROLLER
8-BIT MICROCOMPUTER WITH FACTORY MASK PROGRAMMABLE ROM
80C152A
UNIVERSAL COMMUNICATION CONTROLLER
8-BIT MICROCOMPUTER

- **Superset of 80C51BH Architecture**
- **Multi-Protocol Serial Communication I/O Port (1.5 Mbps/2.4 Mbps Max)**
  - **SDLC**
  - **HDLC**
  - **CSMA/CD**
  - **User Definable Protocols**
- **Full Duplex/Half Duplex**
- **MCS®-51 Compatible UART**
- **12 MHz Maximum Clock Frequency**
- **Multiple Power Conservation Modes**
- **64KB Program Memory Addressing**
- **64KB Data Memory Addressing**
- **256 Bytes On-Chip RAM**
- **Dual On-Chip DMA Channels**
- **Hold/Hold Acknowledge**
- **Two General Purpose Timer/Counters**
- **56 Special Function Registers**
- **11 Interrupt Sources**
- **Available in 48 Pin Dual-in-Line Package and 68 Pin Surface Mount PLCC Package**
  (See Packaging Spec. Order #231369)

The 80C152, which is based on the MCS®-51 CPU, is a highly integrated single-chip 8-bit microcontroller designed for cost-sensitive, high-speed, serial communications. It is well suited for implementing Integrated Services Digital Networks (ISDN), emerging Local Area Networks, and user defined serial backplane applications. In addition to the multi-protocol communication capability, the 80C152 offers traditional microcontroller features for peripheral I/O interface and control.

Silicon implementations are much more cost effective than multiwire cables found in board level parallel-to-serial and serial-to-parallel converters. The 83C152 contains, in silicon, all the features needed for the serial-to-parallel conversion. Other 83C152 benefits include: 1) better noise immunity through differential signaling or fiber optic connections, 2) data integrity utilizing the standard, designed in CRC checks, and 3) better modularity of hardware and software designs. All of these—cost, network parameter and real estate improvements apply to 83C152 serial links between boards or systems and 83C152 serial links on a single board.



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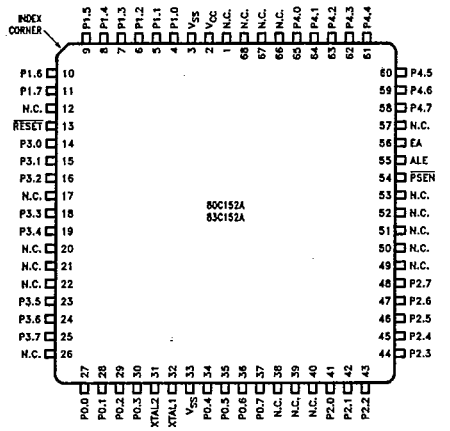

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Figure 1. Connection Diagrams

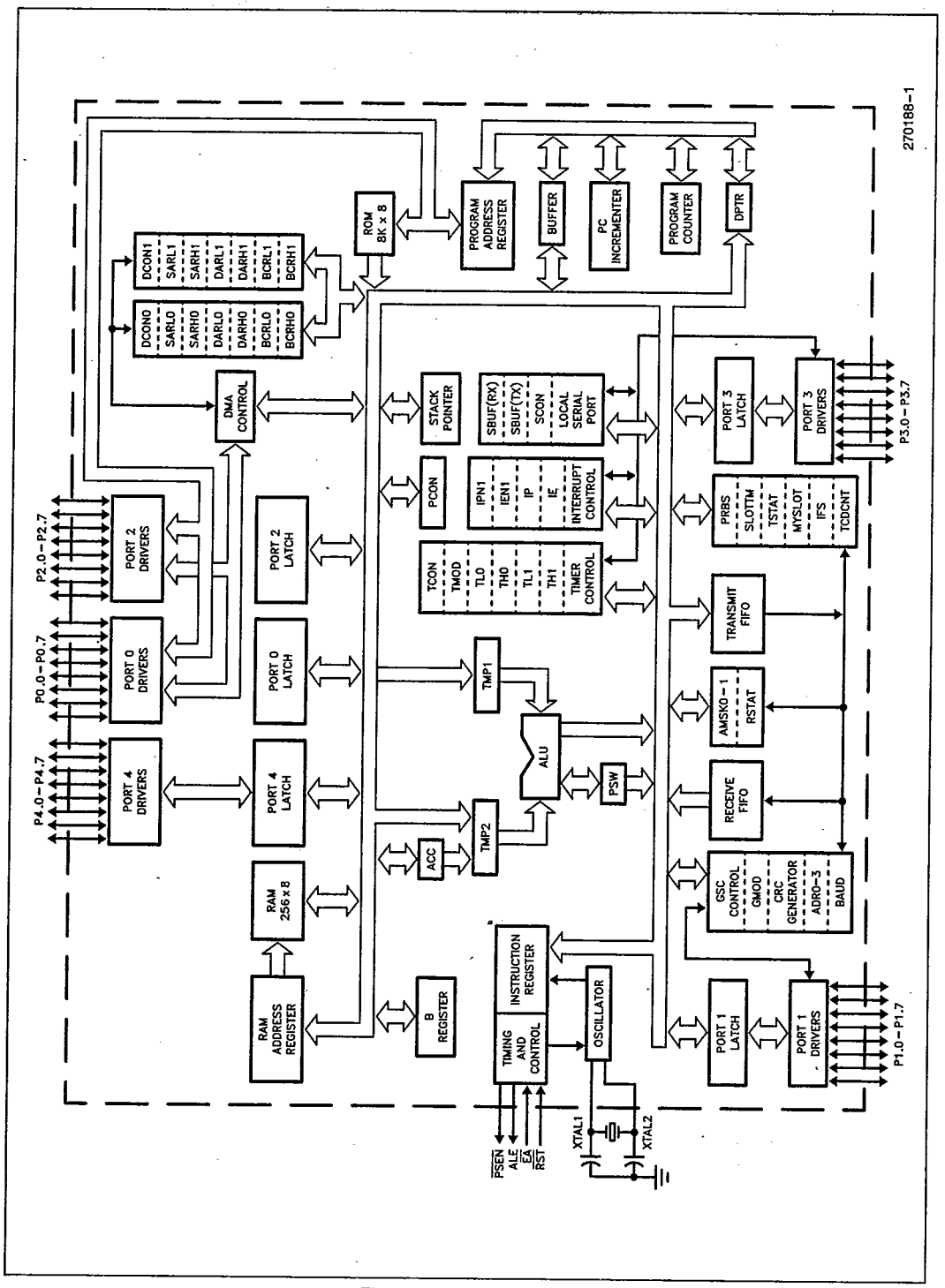

Figure 2. Block Diagram

Pin #		Pin Description
DIP	PLCC(1)	
48	2	V_{CC}—Supply voltage.
24	3,33(2)	V_{SS}—Circuit ground.
18-21, 25-28	27-30, 34-37	**Port 0**—Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification. External pullups are required during program verification.
1-8	4-11	**Port 1**—Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 1 also serves the functions of various special features of the 8XC152, as listed below:

Pin	Name	Alternate Function
P1.0	GRXD	GSC data input pin
P1.1	GTXD	GSC data output pin
P1.2	$\overline{DEN}$	GSC enable signal for an external driver
P1.3	$\overline{TXC}$	GSC input pin for external transmit clock
P1.4	$\overline{RXC}$	GSC input pin for external receive clock
P1.5	$\overline{HLD}$	DMA hold input/output
P1.6	$\overline{HLDA}$	DMA hold acknowledge input/output

29-36	41-48	**Port 2**—Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR and DMA operations). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits during program verification.
10-17	14-16, 18, 19, 23-25	**Port 3**—Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups. Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial input line
P3.1	$\overline{TXD}$	Serial output line
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 external input
P3.5	T1	Timer 1 external input
P3.6	$\overline{WR}$	External Data Memory Write strobe
P3.7	$\overline{RD}$	External Data Memory Read strobe

NOTES:
1. N.C. pins on PLCC package may be connected to internal die and should not be used in customer applications.
2. It is recommended that both Pin 3 and Pin 33 be grounded for PLCC devices.

Pin Description (Continued)

Pin #		Pin Description
47-40	65-58	**Port 4**—Port 4 is an 8-bit bidirectional I/O port with internal pullups. Port 4 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. In addition, Port 4 also receives the low-order address bytes during program verification.
9	13	**$\overline{RST}$**—Reset input. A logic low on this pin for three machine cycles while the oscillator is running resets the device. An internal pullup resistor permits a power-on reset to be generated using only an external capacitor to V_{SS}. Although the GSC recognizes the reset after three machine cycles, data may continue to be transmitted for up to 4 machine cycles after Reset is first applied.
38	55	**ALE**—Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. While in Reset, ALE remains at a constant high level.
37	54	**$\overline{PSEN}$**—Program Store Enable is the Read strobe to External Program Memory. When the 8XC152 is executing from external program memory, $\overline{PSEN}$ is active (low). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory. While in Reset, $\overline{PSEN}$ remains at a constant high level.
39	56	**$\overline{EA}$**—External Access enable. $\overline{EA}$ must be externally pulled low in order to enable the 8XC152 to fetch code from External Program Memory locations 0000H to 0FFFH. $\overline{EA}$ must be connected to V_{CC} for internal program execution.
23	32	**XTAL1**—Input to the inverting oscillator amplifier and input to the internal clock generating circuits.
22	31	**XTAL2**—Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

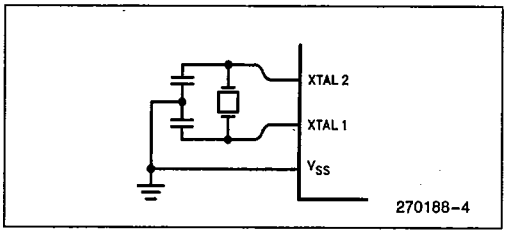

Figure 3. Using the On-Chip Oscillator

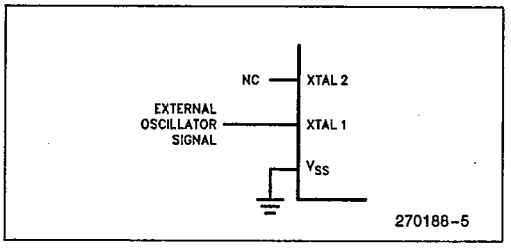

Figure 4. External Clock Drive

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while most of the on-chip peripherals remain active. The major peripherals that do not remain active during Idle, are the DMA channels. The Idle Mode is invoked by software. The content of the on-chip RAM and all the Special Function Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

POWER DOWN MODE

In Power Down Mode, the oscillator is stopped and all on-chip functions cease except that the on-chip RAM contents are maintained. The mode Power Down is invoked by software. The Power Down Mode can be terminated only by a hardware reset.

Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	Port 0	Port 1	Port 2	Port 3	Port 4
Idle	Internal	1	1	Data	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data	Data
Power Down	Internal	0	0	Data	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to the Embedded Controller Handbook, and Application Note AP-252, "Designing with the 80C51BH."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any pin to V_{SS} ..−0.5V to (V_{CC} + 0.5V)
Voltage on V_{CC} to VSS.....−0.5V to +6.5V
Power Dissipation .....1.0 W(7)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V)

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (All Except $\overline{EA}$)	−0.5		$0.2V_{CC}-0.1$	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$)	−0.5		$0.2V_{CC}-0.3$	V	
V_{IH}	Input High Voltage (Except XTAL1, $\overline{RST}$)	$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, $\overline{RST}$)	$0.7V_{CC}$		$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3, 4)			0.45	V	I_{OL} = 1.6 mA (Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)			0.45	V	I_{OL} = 3.2 mA (Note 2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, 4, ALE, $\overline{PSEN}$)	2.4			V	I_{OH} = −60 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −10 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −400 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −40 μA (Note 3)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, 4)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3, 4)			−650	μA	V_{IN} = 2V
I_{LI}	Input Leakage (Port 0, $\overline{EA}$)			±10	μA	$0.45<V_{IN}<V_{CC}$
RRST	Reset Pullup Resistor	40			kΩ	

NOTES:
1. "Typicals" are based on samples taken from early manufacturing lots and are not guaranteed. The measurements were made with V_{CC} = 5V at room temperature.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} − 0.5V; XTAL2 N.C.; Port 0 pins connected to V_{CC}. "Operating" current is measured with $\overline{EA}$ connected to V_{CC} and $\overline{RST}$ connected to V_{SS}. "Idle" current is measured with $\overline{EA}$ connected to V_{SS}, $\overline{RST}$ connected to V_{CC} and GSC inactive.
5. The specifications relating to external data memory characteristics are also applicable to DMA operations.
6. TQVWX should not be confused with TQVWX as specified for 80C51BH. On 80C152, TQVWX is measured from data valid to rising edge of $\overline{WR}$. On 80C51BH, TQVWX is measured from data valid to falling edge of $\overline{WR}$. See timing diagrams.
7. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

MAX I_{CC} (ACTIVE) = (2.24 × FREQ) + 4.16 (Note 4)
MAX I_{CC} (IDLE) = (0.8 × FREQ) + 2.2 (Note 4)
where FREQ is the external oscillator Frequency in Megahertz and I_{CC} is in Milliamps

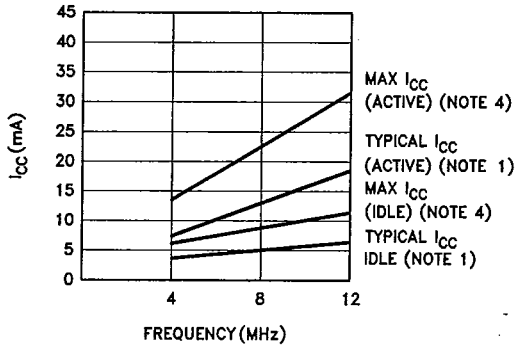

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Figure 5. I_{CC} vs Frequency

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address.
C: Clock
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: $\overline{PSEN}$.
Q: Output data.
R: $\overline{READ}$ signal.
T: Time.
V: Valid.
W: $\overline{WRITE}$ signal.
X: No longer a valid logic level.
Z: Float.

For example,

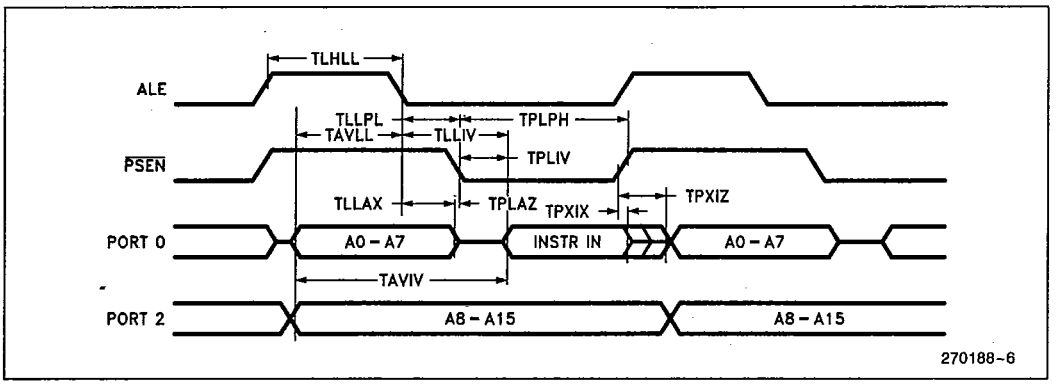
TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{PSEN}$ Low.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

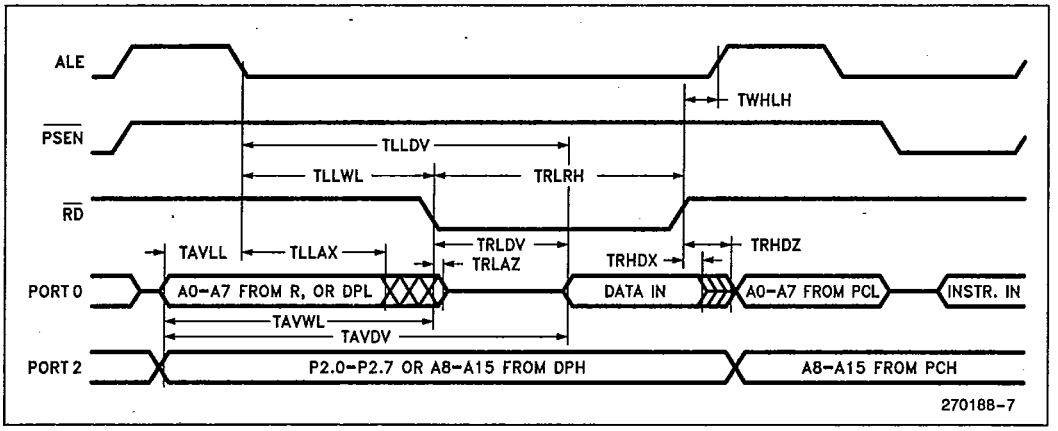
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS (Note 5)

Symbol	Parameter	12 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12	MHz
TLHLL	ALE Pulse Width	126		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	28		TCLCL-55		ns
TLLAX	Address Hold After ALE Low	48		TCLCL-35		ns
TLLIV	ALE Low to Valid Instruction In		233		4TCLCL-100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	43		TCLCL-40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL-45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		3TCLCL-105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		58		TCLCL-25	ns
TAVIV	Address to Valid Instruction In		311		5TCLCL-105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL-100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		251		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		96		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		516		8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL-130		ns
TQVWX (Note 6)	Data Valid to $\overline{WR}$ Transition	333		6TCLCL-167		ns
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL-40	TCLCL+40	ns

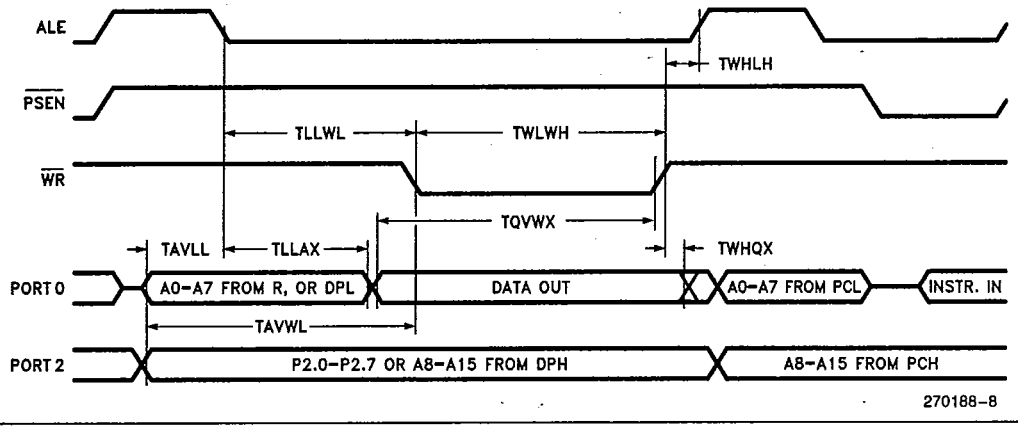
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



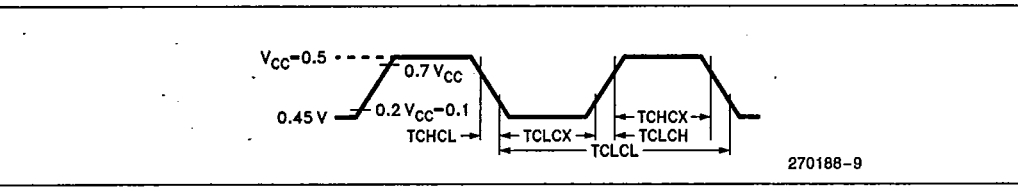
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

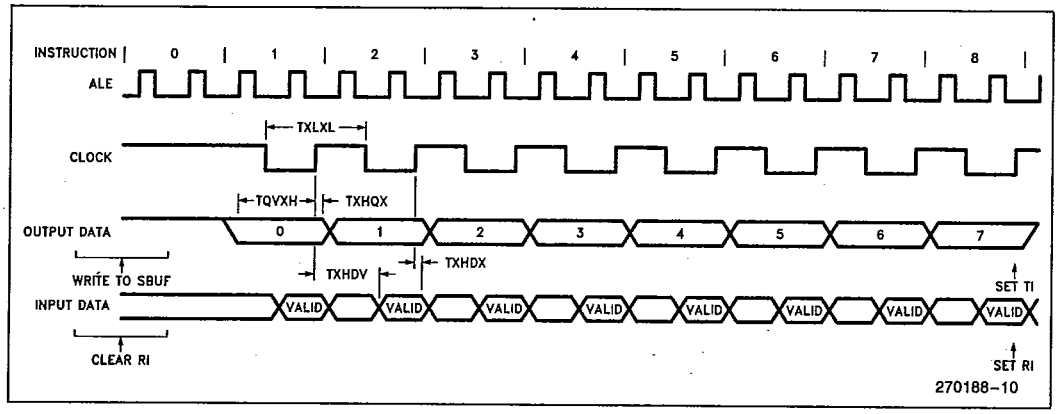
EXTERNAL CLOCK DRIVE WAVEFORM



LOCAL SERIAL CHANNEL TIMING—SHIFT REGISTER MODE

Symbol	Parameter	12 MHz		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1000		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL-133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



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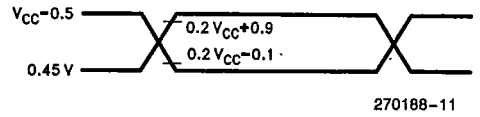
A.C. TESTING:

INPUT, OUTPUT WAVEFORMS



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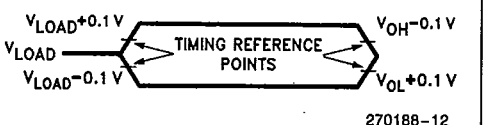
AC Inputs During Testing are Driven at $V_{CC}-0.5$ for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at V_{IH} Min for a Logic "1" and V_{IL} Max for a Logic "0".

FLOAT WAVEFORM



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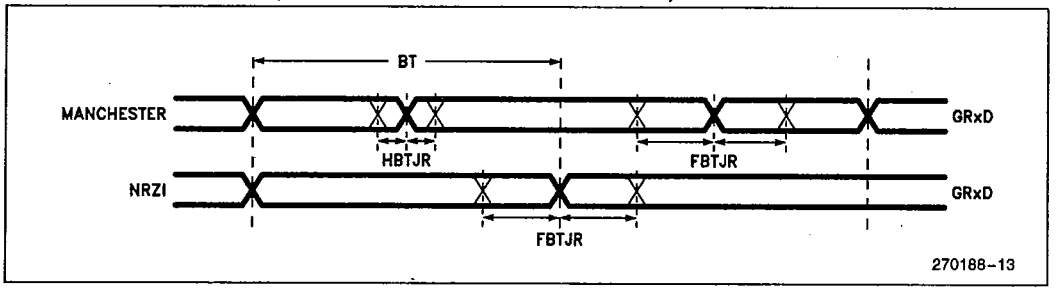
For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs, and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 20$ mA

GLOBAL SERIAL PORT TIMINGS—Internal Baud Rate Generator

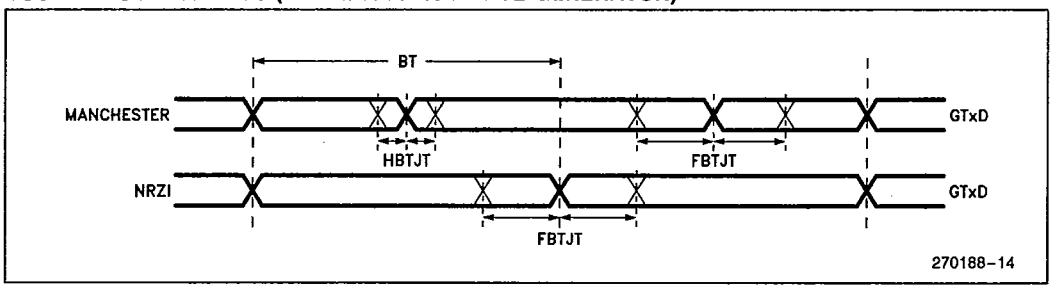
Symbol	Parameter	12 MHz (BAUD = 0)		Variable Oscillator		Unit
		Min	Max	Min	Max	
HBTJR	Allowable jitter on the Receiver for ½ bit time (Manchester encoding only)		0.058		(0.125 × (BAUD+1)× 8TCLCL) −25 ns	µs
FBTJR	Allowable jitter on the Receiver for one full bit time (NRZI and Manchester)		0.142		(0.25 × (BAUD+1)× 8TCLCL) −25 ns	µs
HBTJT	Jitter of data from Transmitter for ½ bit time (Manchester encoding only)		±35		±35	ns
FBTJT	Jitter of data from Transmitter for one full bit time (NRZI and Manchester)		±70		±70	ns
DRTR	Data rise time for Receiver (Note 8)		20		20	ns
DFTR	Data fall time for Receiver (Note 9)		20		20	ns

NOTES:
8. Same as TCLCH, use External Clock Drive Waveform.
9. Same as TCHCL, use External Clock Drive Waveform.

GSC RECEIVER TIMINGS (INTERNAL BAUD RATE GENERATOR)



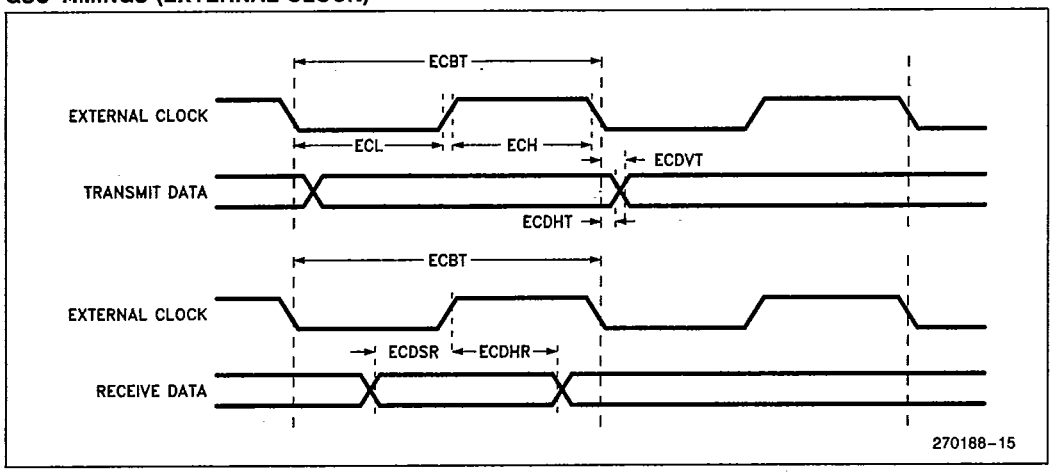
GSC TRANSMIT TIMINGS (INTERNAL BAUD RATE GENERATOR)



GLOBAL SERIAL PORT TIMINGS—External Clock

Symbol	Parameter	12 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/ECBT	GSC Frequency with an External Clock	0.009	2.4	0.009	1/5TCLCL	MHz
ECH	External Clock High	197		2TCLCL + 30 ns		ns
ECL	External Clock Low	197		2TCLCL + 30 ns		ns
ECRT	External Clock Rise Time (Note 8)		20		20	ns
ECFT	External Clock Fall Time (Note 9)		20		20	ns
ECDVT	External Clock to Data Valid Out - Transmit (to External Clock Negative Edge)		150		150	ns
ECDHT	External Clock Data Hold - Transmit (to External Clock Negative Edge)	0		0		ns
ECDSR	External Clock Data Set-up - Receiver (to External Clock Positive Edge)	45		45		ns
ECDHR	External Clock to Data Hold - Receiver (to External Clock Positive Edge)	50		50		ns

GSC TIMINGS (EXTERNAL CLOCK)



NOTES ON THE OPERATION OF THE 80C152A

1. Current in Power Down Mode

   Typically, I_{CC} in Power Down Mode is about 10 μA. However, you may note under certain conditions an abnormally high I_{CC}, about 600 μA, in Power Down. This is caused by an interaction between internal signals local to the interrupt control system. The problem disappears once an interrupt, any interrupt, is requested and serviced. Therefore, if I_{CC} in Power Down is critical to the application, it is suggested that an interrupt be generated and exercised before Power Down is invoked.

2. SDLC Flags While Idling

   In SDLC Mode, the GSC can be programmed to transmit SDLC flags between transmission frames. This is done by setting the GFIEN bit in PCON. When the GSC is so programmed, the $\overline{DEN}$ signal is asserted only during the actual transmission frame, not during the idle fill flags. In this case the $\overline{DEN}$ signal will normally not be used to enable the line driver, but is available for use as a positive indication that a transmission frame is in progress.

3. Immediate Deactivation of $\overline{DEN}$ in CSMA/CD Mode

   CSMA/CD protocols typically require two bittimes of inactivity in the line to indicate an idle condition. Note, however, that the 80C152A deactivates $\overline{DEN}$ immediately at the end of the transmission frame.