

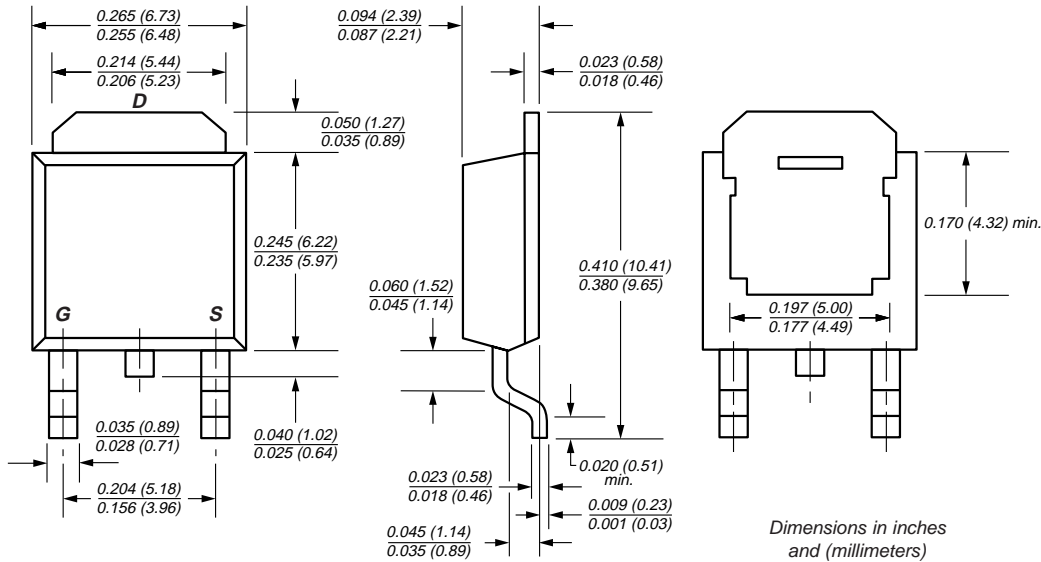
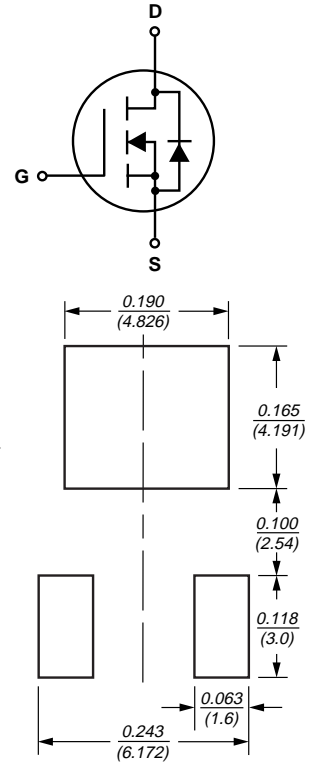
N-Channel Enhancement-Mode MOSFET

V_{DS} 30V R_{DS(ON)} 16.5mΩ I_D 38A



TRENCH GENFET®
New Product

TO-252 (DPAK)



Dimensions in inches and (millimeters)

Mounting Pad Layout

Mechanical Data

Case: JEDEC TO-252 molded plastic body
Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
High temperature soldering guaranteed: 250°C/10 seconds at terminals
Weight: 0.011oz., 0.4g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Specially Designed for Low Voltage DC/DC Converters
- Fast Switching for High Efficiency
- Low Gate Charge

Maximum Ratings and Thermal Characteristics (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current T _J = 150°C	I _D	T _C = 25°C 38	A
		T _C = 70°C 30	
Pulsed Drain Current ⁽¹⁾	I _{DM}	80	
Power Dissipation T _J = 150°C	P _D	T _C = 25°C 38	W
		T _C = 70°C 24	
		T _A = 25°C ⁽²⁾ 2.5	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Junction-to-Case Thermal Resistance	R _{θJC}	3.3	°C/W
Junction-to-Ambient Thermal Resistance ⁽²⁾	R _{θJA}	50	°C/W

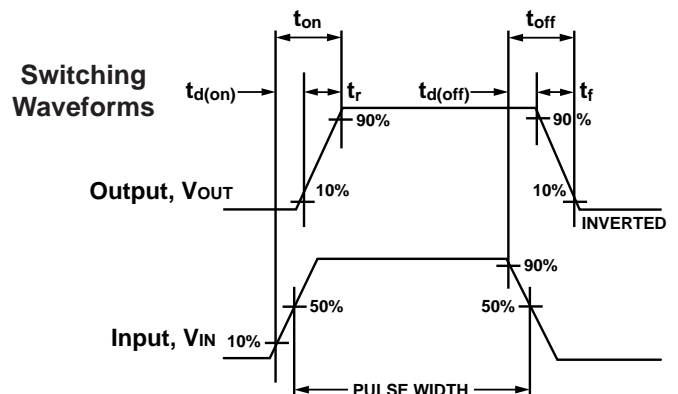
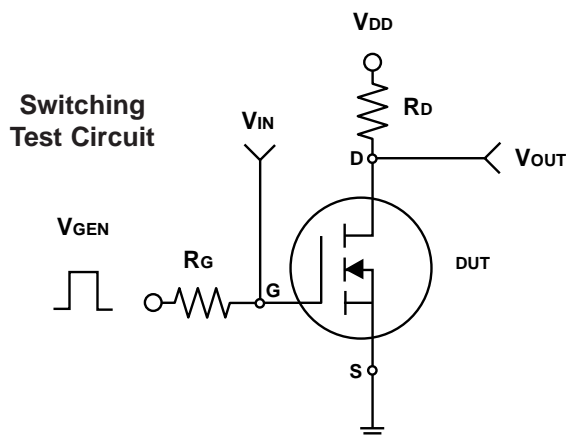
Notes: (1) Pulse width limited by maximum junction temperature
 (2) Surface mounted on a 1in² 2 oz.. Cu PCB (FR-4 material)

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Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	30	–	–	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.8	–	2.5	V
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	–	–	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V	–	–	1	μA
		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C	–	–	10	
On-State Drain Current ⁽¹⁾	I _{D(on)}	V _{DS} ≥ 5V, V _{GS} = 10V	80	–	–	A
Drain-Source On-State Resistance ⁽¹⁾	R _{DS(on)}	V _{GS} = 10V, I _D = 19A	–	12.5	16.5	mΩ
		V _{GS} = 4.5V, I _D = 15A	–	19	25	
Forward Transconductance ⁽¹⁾	g _{fs}	V _{DS} = 5V, I _D = 19A	–	25	–	S
Dynamic						
Total Gate Charge	Q _g	V _{DS} = 15V, V _{GS} = 5V, I _D = 19A	–	11	14	nC
		V _{DS} = 15V, I _D = 19A V _{GS} = 10V	–	22	28	
Gate-Source Charge	Q _{gs}	V _{DS} = 15V, I _D = 19A V _{GS} = 10V	–	3.4	–	nC
Gate-Drain Charge	Q _{gd}	V _{DS} = 15V, I _D = 19A V _{GS} = 10V	–	3.4	–	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15V, I _D = 1A V _{GEN} = 10V, R _G = 6Ω	–	10	18	ns
Turn-On Rise Time	t _r		–	14	25	
Turn-Off Delay Time	t _{d(off)}		–	38	60	
Turn-Off Fall Time	t _f		–	6	10	
Input Capacitance	C _{iss}	V _{DS} = 15V, V _{GS} = 0V f = 1.0MHz	–	1173	–	pF
Output Capacitance	C _{oss}		–	199	–	
Reverse Transfer Capacitance	C _{rss}		–	112	–	
Source-Drain Diode						
Diode Forward Voltage ⁽¹⁾	V _{SD}	I _S = 19A, V _{GS} = 0V	–	0.9	1.2	V
Continuous Source Current (Diode Conduction)	I _S	–	–	–	30	A

Notes: (1) Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%



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Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 1 – Output Characteristics

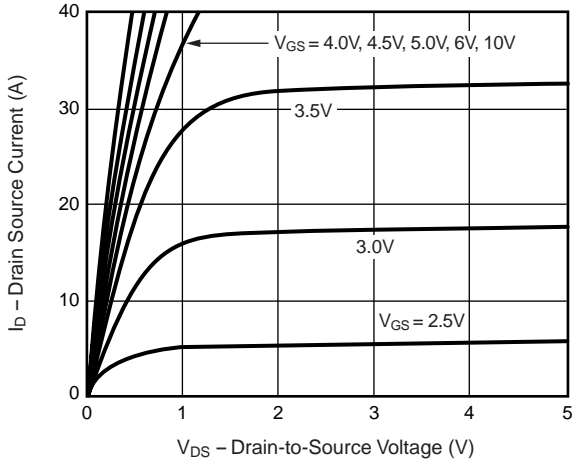


Fig. 2 – Transfer Characteristics

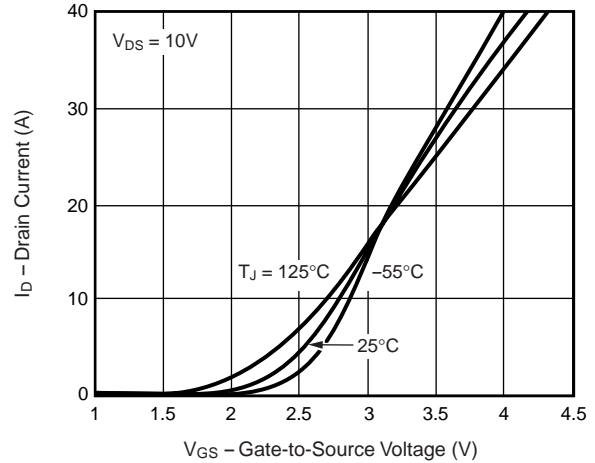


Fig. 3 – Threshold Voltage vs. Temperature

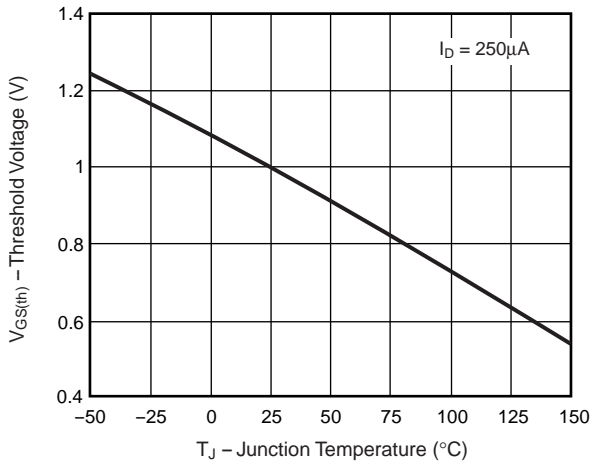


Fig. 4 – On-Resistance vs. Drain Current

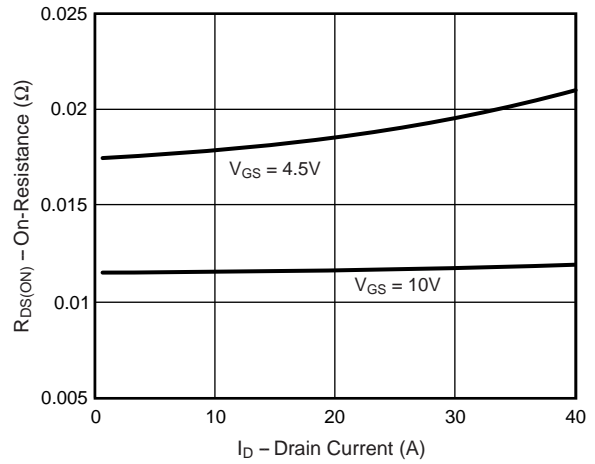
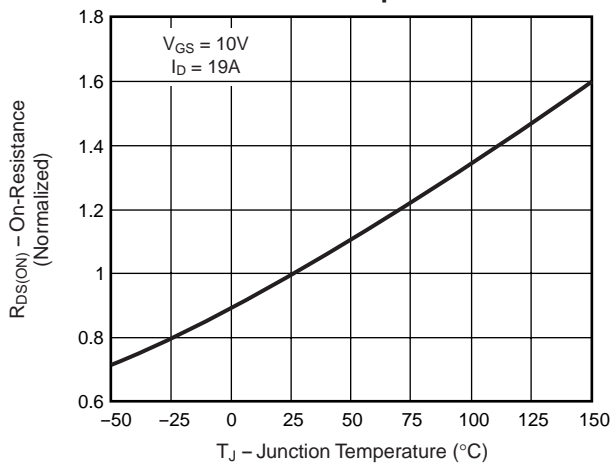


Fig. 5 – On-Resistance vs. Junction Temperature



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Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

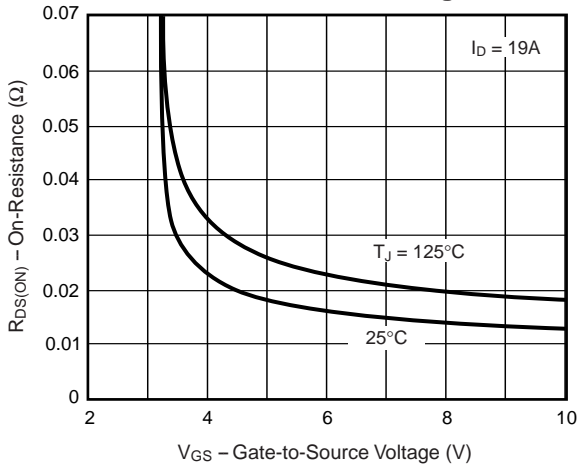


Fig. 7 – Gate Charge

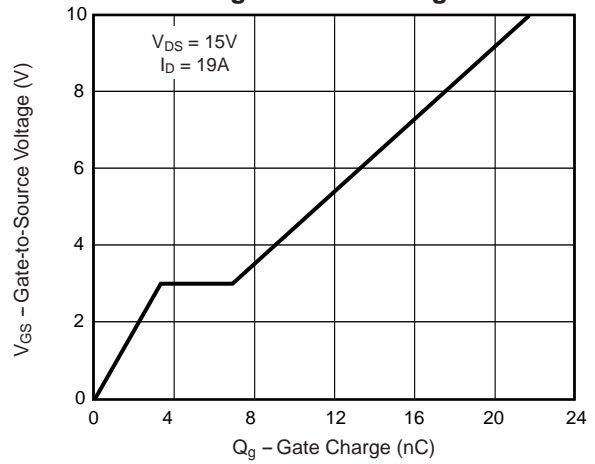


Fig. 8 – Capacitance

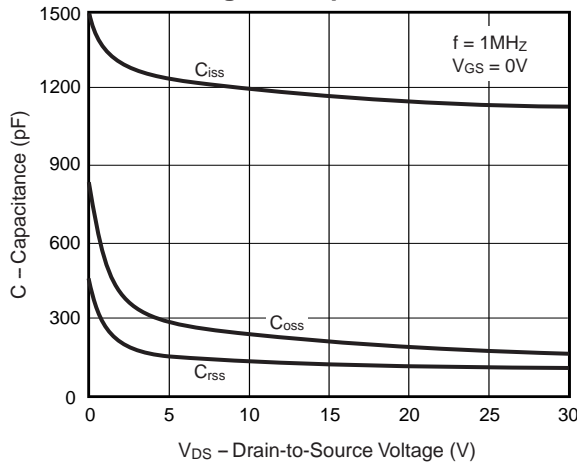


Fig. 9 – Source-Drain Diode Forward Voltage

