FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27707-2E

ASSP for Power Supply Applications (For Secondary Battery)

Li-Ion Battery Protection IC

MB3836

■ DESCRIPTION

The MB3836 is a lithium-ion battery protection IC for three cells series lithium-ion battery pack in a notebook PC's. This IC supports charging at 12.6 V and detects an over-charge, over-discharge, and over-current to control charging and discharging.

The IC has a built-in function that makes the battery rechargeable even when the battery voltage has decreased to 0 V.

Upon detection of an over-discharge from the lithium-ion battery, the IC outputs a preliminary signal to stop discharging. This feature allows the notebook PC to save its memory data to hard disk. In addition, the IC allows the battery to be used up to the over-discharge level of each cell, increasing the operating time.

After detecting an over-discharge, the IC disconnects all of its biases so that its current consumption becomes 0 μA. The IC can therefore make the battery pack rechargeable even when it has been left for an extended period of time with the output disconnected due to over-discharging.

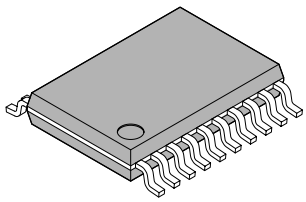
The battery can also be set into a quasi-over-discharged state even when the cell voltage is equal to or greater than the over-discharge detection voltage. When the notebook PC is shipped, the IC can prevent the battery pack from being discharged and turn off its bias sources, allowing the battery pack to be stored for a long time.

The IC's remote on/off function can turn off the output from the detached battery pack without the need for an external logic circuit or any mechanism on the notebook PC. This prevents the output from being short-circuited by a malfunction and facilitates the handling of the battery pack itself.

The MB3836 is the best IC for protecting the lithium-ion battery pack used for a notebook PC.

■ PACKAGE

20-pin plastic SSOP



(FPT-20P-M03)

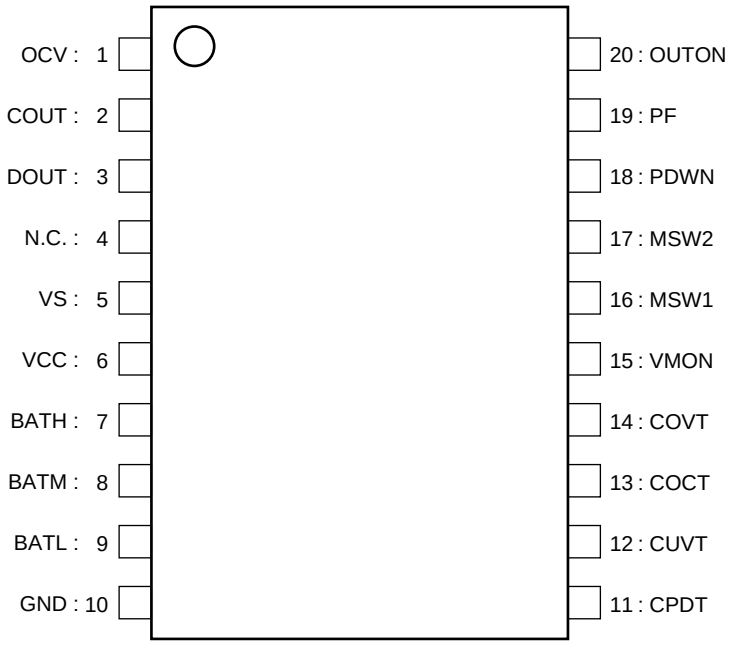
FUJITSU

■ FEATURES

- Power supply voltage range : 6 V to 13.5 V
- High-precision over-charge detection voltage : 4.325 V ± 0.025 V
- Circuit power consumption after detecting over-discharge : 0 μA (Typ)
- Built-in quasi-over-discharge function
- Built-in pre-alarm function before shutting down of over-discharge
- Built-in remoting ON/OFF function
- Built-in over-discharge current detecting function with 2-step delay time : Vth = 300 mV→7 ms (Typ)
  : Vth = 600 mV→500 μs (Typ)
- Built-in charge recovery function for 0 V cell

■ PIN ASSIGNMENT

(TOP VIEW)

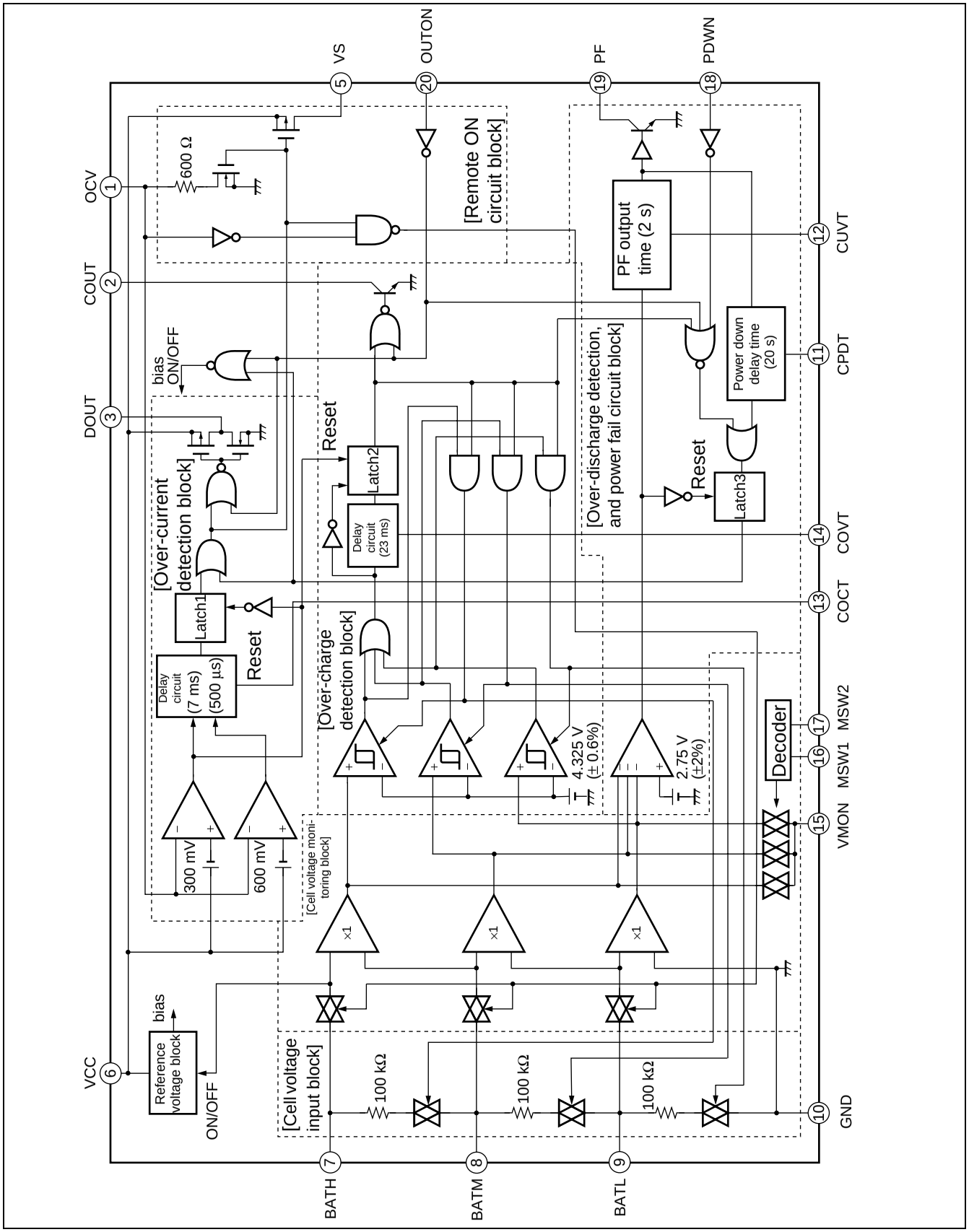


(FPT-20P-M03)

■ PIN DESCRIPTIONS

<table>
<tr><th>Pin no.</th><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td>1</td><td>OCV</td><td>I</td><td>Over-current state and discharging/charging state detection terminal</td></tr>
<tr><td>2</td><td>COUT</td><td>O</td><td>Pch MOS control output terminal for charging control switch</td></tr>
<tr><td>3</td><td>DOUT</td><td>O</td><td>Pch MOS control output terminal for discharging control switch</td></tr>
<tr><td>4</td><td>N.C.</td><td>—</td><td>No connection</td></tr>
<tr><td>5</td><td>VS</td><td>O</td><td>“H” level output terminal for remoting ON function</td></tr>
<tr><td>6</td><td>VCC</td><td>—</td><td>Power supply terminal</td></tr>
<tr><td>7</td><td>BATH</td><td>I</td><td>Battery connection terminal</td></tr>
<tr><td>8</td><td>BATM</td><td>I</td><td>Battery connection terminal</td></tr>
<tr><td>9</td><td>BATL</td><td>I</td><td>Battery connection terminal</td></tr>
<tr><td>10</td><td>GND</td><td>—</td><td>GND terminal</td></tr>
<tr><td>11</td><td>CPDT</td><td>—</td><td>Capacitor connection terminal for setting power-down delay time</td></tr>
<tr><td>12</td><td>CUVT</td><td>—</td><td>Capacitor connection terminal for setting PF output delay time</td></tr>
<tr><td>13</td><td>COCT</td><td>—</td><td>Capacitor connection terminal for setting over-current detection time</td></tr>
<tr><td>14</td><td>COVT</td><td>—</td><td>Capacitor connection terminal for setting over-charge detection time</td></tr>
<tr><td>15</td><td>VMON</td><td>O</td><td>Output terminal of monitoring cell voltage</td></tr>
<tr><td>16</td><td>MSW1</td><td>I</td><td rowspan="2">Switching signal of monitoring cell voltage input terminal
<table>
<tr><th>MSW1</th><th>MSW2</th><th>VMON output</th><th>Cell voltage input block SW</th></tr>
<tr><td>L</td><td>L</td><td>—</td><td>Depend on over-charge detection block</td></tr>
<tr><td>L</td><td>H</td><td>H cell voltage</td><td>Off</td></tr>
<tr><td>H</td><td>L</td><td>M cell voltage</td><td>Off</td></tr>
<tr><td>H</td><td>H</td><td>L cell voltage</td><td>Off</td></tr>
</table></td></tr>
<tr><td>17</td><td>MSW2</td><td>I</td></tr>
<tr><td>18</td><td>PDWN</td><td>I</td><td>Power down signal input terminal
After input “H” level, Latch 3 will be set, DOUT=”H” level, and OCV=”L” level. At this time, all battery connecting terminal will be released, and all bias will be set OFF.</td></tr>
<tr><td>19</td><td>PF</td><td>O</td><td>PF signal output terminal</td></tr>
<tr><td>20</td><td>OUTON</td><td>I</td><td>Remoting ON signal input terminal
After input “L” level, the bias of over-charge detection block will be set OFF. At this time, DOUT and COUT value will be equal to “H” level.</td></tr>
</table>

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	—	—	20	V
Input voltage	V_I	BATH, OCV, PDWN, OUTON, PF, MSW1, MSW2 terminals	—	20	V
Collector output voltage	V_O	COUT terminal	—	25	V
Output current	I_O	DOUT, COUT terminals (DC)	—	2	mA
Peak output current	I_O	DOUT, COUT terminals Duty = t_{ON} / t	—	2 / Duty	mA
Power dissipation	P_D	Ta ≤ + 25 °C	—	540 *	mW
Operating temperature	Ta	—	–30	+ 85	°C
Storage temperature	Tstg	—	–55	+ 125	°C

* : When mounted on a 10 cm square double-sided epoxy board.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	—	6.0	12.6	13.5	V
Input voltage	V_I	OCV, PDWN, OUTON, MSW1, MSW2 terminals	0	—	18	V
Output current	I_O	VS terminal	–10	—	0	mA
External OCV terminal resistor	R_{OCV}	—	—	—	10	Ω
Capacitor for setting delay time	C_{OVT}	—	220	10000	—	pF
	C_{UVT}	—	0.001	0.15	—	µF
	C_{PDT}	—	0.001	1.5	—	µF
	C_{OCT}	—	220	560	—	pF

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 12.6 V, Ta = + 25 °C)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Over-charge detection block	Detection voltage	V_{TH}	2, 7, 8, 9	Ta = + 25 °C, Each cell voltage	4.300	4.325	4.350	V
				Ta = 0 °C to + 70 °C, Each cell voltage	4.280	4.325	4.370	V
	Hysteresis width	V_H	2, 7, 8, 9	—	0.14	0.20	0.26	V
	Input current	I_{IN}	7, 8, 9	Each cell voltage = 4.2 V	—	0.1	0.5	µA
	Delay time	t_D	2	COVT = 0.01 µF	11.5	23	34.5	ms
	Output voltage	V_{OL}	2	COUT = 1 mA	—	0.75	1.0	V
	Output leakage current	I_{LEAK}	2	COUT = 13.5 V	—	0	0.5	µA
Over-discharge detection, power-fail circuit block	Detection voltage	V_{TH}	7, 8, 9, 19	—	2.695	2.75	2.805	V
	PF output delay time	t_{D1}	19	CUVT = 0.15 µF, VCC = 8.5 V	1	2	3	s
	PF Min pulse width	t_P	19	CUVT = 0.15 µF, VCC = 8.5 V	—	7 *	—	ms
	Output voltage	V_{OL}	19	PF = 1 mA	—	0.75	1.0	V
	Output leakage current	I_{LEAK}	19	PF = 13.5 V	—	0	0.5	µA
	Input threshold voltage	V_{TH}	3, 18	Each cell voltage = 2 V	2.0	3.5	5.0	V
	Input current	I_{IN}	18	PDWN = 5 V	—	50	100	µA
	Power-down delay time	t_{D2}	3	CPDT = 1.5 µF, VCC = 8.5 V	10	20	30	s
Over-current detection block	Detection voltage	V_{TH1}	1, 3, 13	Voltage between VCC terminal and OCV terminal	0.22	0.30	0.38	V
		V_{TH2}	1, 3, 13	Voltage between VCC terminal and OCV terminal	0.45	0.60	0.75	V
	Delay time	t_{D1}	3	COCT = 560 pF V_{TH2} > VCC–OCV > V_{TH1}	4	7	10	ms
		t_{D2}	3	COCT = 560 pF VCC–OCV > V_{TH2}	250	500	750	µs
	Output voltage	V_{OL}	3	DOUT = 1 mA	—	—	1.0	V
		V_{OH}	3	DOUT = –0.4 mA	V_{CC}– 0.4	—	—	V
Cell voltage input block	Input current at over-charge	I_{IN}	7, 8, 9	Each cell voltage = 4.5 V	22.5	45	67.5	µA
	Short cell detection voltage	V_{TH}	7, 8, 9	Cell voltage without measuring cell = 3.6 V at COUT = “L”→“H”	—	0.6 *	—	V

*: Standard design value

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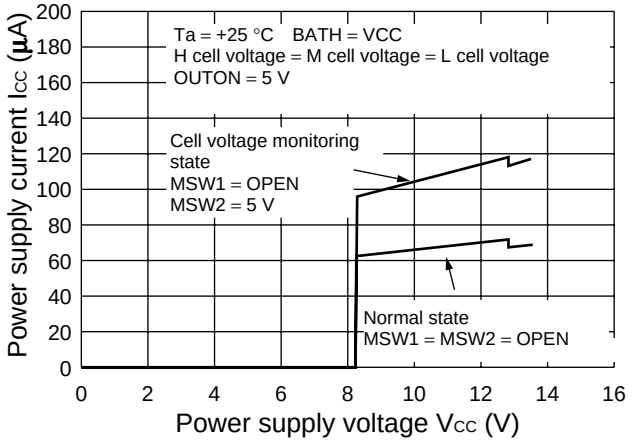
(VCC = 12.6 V, Ta = + 25 °C)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Remoting ON circuit block	Input thereshold voltage	V_{TLH}	1, 2	—	0.8	1.4	2.0	V
	Input current	I_{IN}	1	OCV = 13.5 V	—	10	20	µA
	Input resistance at power-down	R_I	1	—	480	600	720	Ω
	Input thereshold voltage	V_{TH}	20	—	0.8	1.4	2.0	V
	Input current	I_{IN}	20	OUTON = 13.5 V	—	13	17	µA
	Output voltage	V_{OH}	5	VS = –4 mA	V_{CC}–0.5	V_{CC}–0.2	—	V
	Output current	I_O	5	VS = 0 V	–30	—	–11	mA
	Output leakage current	I_{LEAK}	5	VS = 0 V, Each cell voltage = 2 V	–0.5	0	—	µA
Cell voltage monitoring block	Voltage gain	A_V	15	Cell voltage = 2.9 V to 4.2 V	0.98	1.0	1.02	V/V
	Input thereshold voltage	V_{TH}	16, 17	—	0.8	1.4	2.0	V
	Input current	I_{IN}	16, 17	MSW1 = MSW2 = 5 V	—	50	100	µA
	Output source current	I_{OH}	15	Each cell voltage = 2.9 V, MON = 1.9 V	—	–350	–180	µA
	Output sink current	I_{OL}	15	Each cell voltage = 2.9 V, MON = 3.9 V	40	80	—	µA
All device	Power supply current	I_{CC1}	6	VCC = 12.6 V, normal state, OUTON = 5 V	—	75	110	µA
		I_{CC2}	6	VCC = 8.7 V, normal state, OUTON = 5 V	—	65	95	µA
		I_{CC3}	6	VCC = 12.6 V, Cell voltage monitoring state	—	130	200	µA
		I_{CC4}	6	VCC = 6 V, Shutting over-discharge state	—	0 *	—	µA

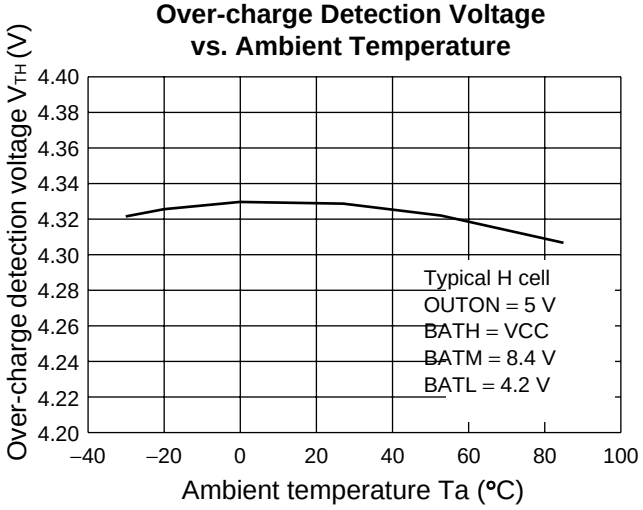
* : Standard design value.

■ TYPICAL CHARACTERISTICS

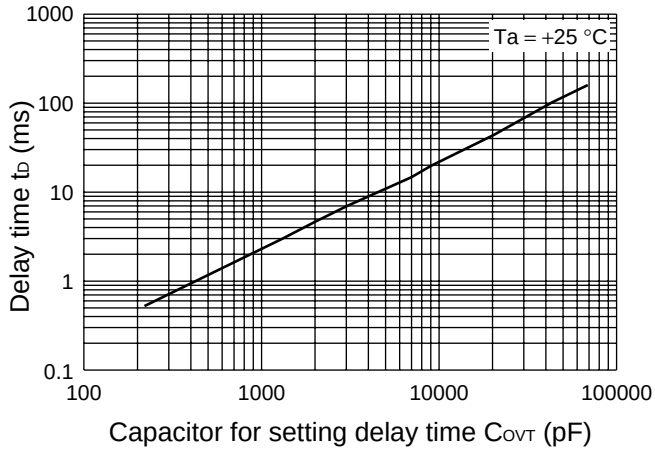
Power Supply Current vs.Power Supply Voltage



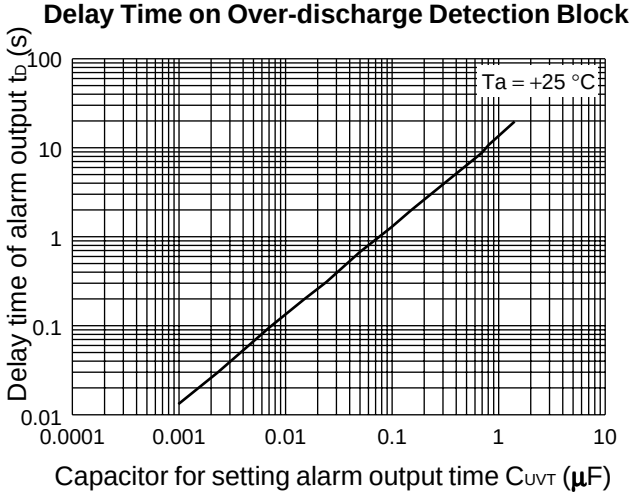
Over-charge Detection Voltage vs. Ambient Temperature



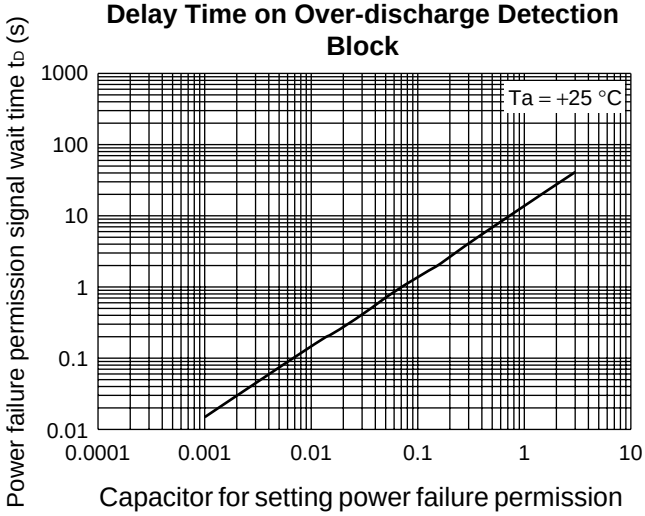
Delay Time on Over-charge Detection Block



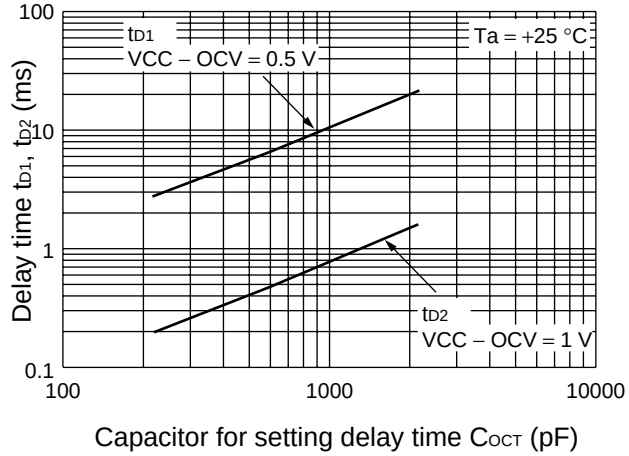
Delay Time on Over-discharge Detection Block



Delay Time on Over-discharge Detection Block



Delay Time of Over-current Detection



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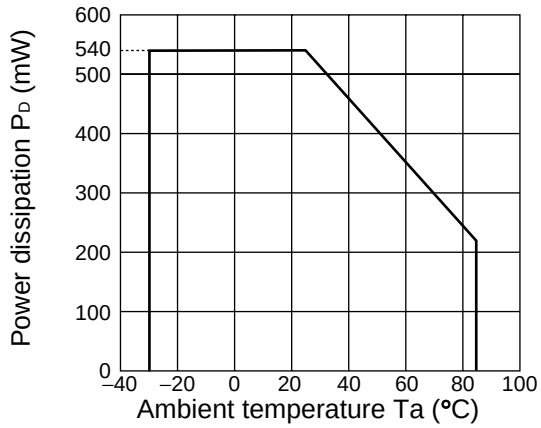
Power Dissipation vs. Ambient Temperature Characteristics



■ FUNCTIONAL DESCRIPTION

(1) Over-charge Detection Block

When the battery is being charged, the over-charge detection block monitors each cell voltage. If any cell voltage reaches or exceeds the over-charge detection voltage (4.325 V Typ) as in Figure 1 (see "1. Over-charge detection block and cell voltage input block " in "■OPERATION TIMING CHART"), the COUT terminal (pin 2) goes “H” level, after a delay time (23 ms Typ) managed by the capacitor (C_{OVT}) connected between the COVT terminal (pin 14) and GND, to turn off the Pch MOS FET for external charge control, thereby stopping charging the battery.

When all the cell voltages in the over-charge detected state become the over-charge release voltage (4.125 V Typ) or less, the COUT terminal (pin 2) goes “L” level to turn on the Pch MOS FET for external charge control.

Even when a cell voltage reaches or exceeds the over-charge detection voltage as in Figure 2, the cell voltage does not enter the over-charge detected state if it falls below the over-charge detection voltage within the delay time (23 ms Typ).

(2) Cell Voltage Input Block

If any cell voltage reaches or exceeds the over-charge detection voltage (4.325 V Typ) as in Figures 1 and 2 (see "1. Over-charge detection block and cell voltage input block" in "■OPERATION TIMING CHART"), the COUT terminal (pin 2) goes high to turn off the Pch MOS FET for external charge control after a delay time (23 ms Typ) managed by the capacitor (C_{OVT}) connected between the COVT terminal (pin 14) and GND. At the same time, the cell voltage input block switch for the cell exceeding the over-charge detection value is turned on to supply the cell voltage input current to that cell so that high-voltage cells are lowered in voltage.

When the cell voltage in the over-charge detected state becomes the over-charge release voltage (4.125 V Typ) or less, the cell voltage input block switch is turned off.

(3) Over-discharge Detection/Power Fail Circuit Block

When the battery is being discharged, the over-discharge detection/power fail circuit block monitors each cell voltage. If any cell voltage becomes the over-discharge detection voltage (2.75 V Typ) as in Figure 5 (see "3. Over-discharge detection/power fail circuit" in "■OPERATION TIMING CHART"), the PF terminal (pin 19) outputs a “L” level PF signal to the notebook PC after a PF output delay time (2 s Typ) managed by the capacitor (C_{UVT}) connected between the CUVT terminal (pin 12) and GND. At the same time, after a power-down delay time (20 s Typ) managed by the capacitor (C_{PDT}) connected between the CPDT terminal (pin 11) and GND, the DOUT terminal (pin 3) goes “H” level to turn off the Pch MOS FET for external discharge control, thereby stopping discharging the battery.

(4) Over-current Detection Block

The over-current detection block monitors the discharge current from the battery. It detects an over-current if the potential difference between the VCC and OCV terminals by RON of Pch MOS FET for external charge control becomes 300 mV or more as in Figure 6 (see "4. Over-current detection block 1" in "■OPERATION TIMING CHART"). After a delay time (7 ms Typ) managed by the capacitor (C_{OCT}) connected between the COCT terminal (pin 13) and GND, the DOUT terminal (pin 3) goes “H” level to turn off the Pch MOS FET for external discharge control, thereby stopping discharging the battery.

When the discharge current is large, if the potential difference between the VCC and OCV terminals becomes 600 mV or more as in Figure 7 (see "5. Over-current detection block 2" in "■OPERATION TIMING CHART"), the DOUT terminal (pin 3) goes “H” level to turn off the Pch MOS FET for external discharge control, thereby stopping discharging the battery, after a power-down delay time (500 µs Typ) managed by the capacitor (C_{OCT}) connected between the COCT terminal (pin 13) and GND.

Note that, if an over-current is detected, the VS terminal (pin 5) goes “L” level in the same way as when the over-discharge detection function works. As discharging is stopped, the OCV terminal (pin 1) goes “L” level to

completely turn off the bias source of this IC, so that the battery pack enters the power-down state. To return from that state, perform recharging operation, or set the OCV terminal (pin 1) to “H” level.

(5) Remote ON Circuit Block

When the battery pack is detached from the notebook PC, the OUTON terminal (pin 20) pulled up to the VS terminal (pin 5) on the notebook PC side goes “L” level to turn off the bias of the over-current detection block. At the same time, the COUT terminal (pin 2) and DOUT terminal (pin 3) go “H” level to turn off the Pch MOS FET for external charge/discharge control.

Even when the OUTON terminal (pin 20) is “L” level with charging/discharging off, the IC is operating and the over-discharge detection function is working to protect the battery. If the VS terminal (pin 5) is “H” level, connecting the battery pack to the main unit makes it readily available.

(6) Cell Voltage Monitor Block

The cell to be monitored can be selected depending on the voltage levels at the MSW1 terminal (pin 16) and MSW2 terminal (pin 17). When the monitor function is operating, the cell voltage input block switch does not work even when an over-charge is detected.

Condition of monitoring cell voltage

Voltage level at MSW1 terminal	Voltage level at MSW2 terminal	VMON output	SW at cell voltage input block
L	L	—	Depend on over-charge detection block
L	H	H cell voltage	Off
H	L	M cell voltage	Off
H	H	L cell voltage	Off

■ SETTING DELAY TIME for OVER-CHARGE DETECTION BLOCK

For over-charge detection, you can set the delay time from when charging the capacitor (C_{OVT}) connected to the COVT terminal (pin 14) is started and the COVT terminal voltage increases until the COUT terminal (pin 2) voltage goes “H” level (with the open-collector output off) with the COVT terminal at the threshold voltage.

Over-charge detection block delay time : t_D (s) ≒ 2.3 × C_{OVT} (μF)

■ SETTING PF OUTPUT DELAY TIME

For over-discharge detection, you can set the delay time from charging the capacitor (C_{UVT}) connected to the CUVT terminal (pin 12) is started and the CUVT terminal voltage increases until the PF terminal (pin 19) voltage goes “L” level with the CUVT terminal at the threshold voltage.

PF output delay time : t_{D1} (s) ≒ 13.3 × C_{UVT} (μF)

■ SETTING POWER-DOWN DELAY TIME

You can set the delay time from charging the capacitor (C_{PDT}) connected to the CPDT terminal (pin 11) is started after “L” level output to the PF terminal (pin 19) at over-discharge detection and the CPDT terminal voltage increases until the DOUT terminal (pin 3) voltage goes high with the CPDT terminal at the threshold voltage.

Power-down delay time : t_{D2} (s) ≒ 13.3 × C_{PDT} (μF)

After the DOUT terminal goes “H” level to stop overdischarging, the OCV terminal (pin 1) goes “L” level to turn off the entire internal circuitry of the IC so that the circuit current becomes 0 μA. Considering the time constant based on the notebook PC’s capacitor connected to the OCV terminal, the discharge time constant of CPDT terminal is used to prevent recovery (return) and shutdown (power-down) from being repeated in response to variations in battery voltage. The capacitor connected to the OCV terminal on the notebook PC side requires the restriction expressed below based on the value of the capacitor (C_{PDT}) connected to the CPDT terminal.

OCV terminal external capacitor : C_{OCV} (μF) < 1790 × C_{PDT} (μF)

■ SETTING DELAY TIME for OVER-CURRENT DETECTION BLOCK

For over-current detection when 0.6 V (Typ) > VCC - OCV > 0.3 V (Typ), you can set the delay time from when charging the capacitor (C_{OCT}) connected to the COCT terminal (pin 13) is started and the COCT terminal voltage increases until the DOUT terminal (pin 3) voltage goes “H” level with the COUT terminal at the threshold voltage.

Over-current detection block delay time : t_{D1} (s) ≒ 12.5 × C_{OCT} (μF)

For over-current detection when VCC - OCV > 0.6 V (Typ), you can set the delay time from when charging the capacitor (C_{OCT}) connected to the COCT terminal (pin 13) is started and the COCT terminal voltage increases until the DOUT terminal (pin 3) voltage goes “H” level with the COCT terminal at the threshold voltage.

Over-current detection block delay time : t_{D2} (s) ≒ 0.9 × C_{OCT} (μF)

■ OPERATION at LOW VOLTAGE

If cell voltages cause extreme imbalance or one or more cells enter the short-circuited state (0.6 V Typ) or less, the short-circuit cell detection function sets the COUT terminal (pin 2) to “H” level (with the open-collector output off). If the VCC terminal (pin 6) voltage becomes 4.2 V (Typ) or less, however, the short-circuit cell detection function is disabled, the COUT terminal (pin 2) goes “L” level, enabling 0 V cell charging, with the OCV terminal (pin 1) at a voltage of 1.4 V (Typ) or higher.

When VCC is less than 4.2 V, the DOUT terminal (pin 3) is fixed at “H” level.

■ OPERATION TIMING CHART

1. Over-charge Detection Block and Cell Voltage Input Block

(1) When cell 3 does not exceed V_{TH} and cells 1 and 2 are lowered in voltage by cell voltage input current and self-discharging

If any cell voltage reaches or exceeds the over-charge detection voltage (4.325 V Typ), the COUT terminal (pin 2) goes “H” level to turn off the Pch MOS FET for external charge control, after a delay time (23 ms Typ) managed by the capacitor (C_{OVT}) connected between the COVT terminal (pin 14) and GND, thereby stopping charging the battery. At this time, the cell voltage input block switch is turned on to supply the cell voltage input current to that cell so that high-voltage cells are lowered in voltage.

When all the cell voltages in the over-charge detected state become the over-charge release voltage (4.125 V Typ) or less, the COVT terminal (pin 14) and COUT terminal (pin 2) go “L” level to turn on the Pch MOS FET for external charge control.

When any cell voltage in the over-charge detected state becomes the over-charge release voltage (4.125 V Typ) or less, the cell voltage input block switch is turned off.

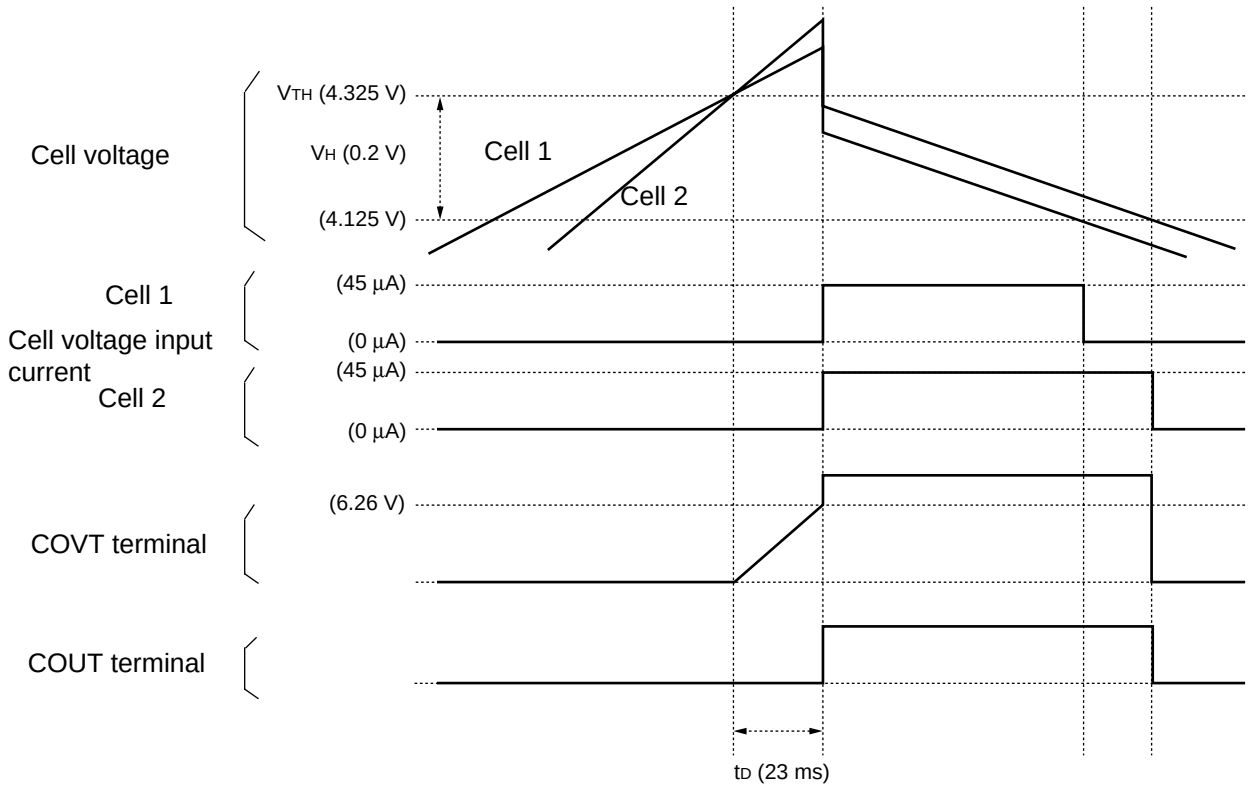


Figure 1

(2) When the voltage is lowered by cell voltage input current and self-discharge after pulsed charge

Even when a cell voltage reaches or exceeds the over-charge detection voltage (4.325 V Typ), the cell voltage does not enter the over-charge detected state if it falls below the over-charge detection voltage (4.325 V Typ) within the delay time (23 ms Typ) managed by the capacitor (C_{OVT}) connected between the COVT terminal (pin 14) and GND.

If a cell voltage reaches or exceeds the over-charge detection voltage (4.325 V Typ), the COUT terminal (pin 2) goes “H” level to turn off the Pch MOS FET for external charge control, stopping charging the battery, after a delay time (23 ms Typ) managed by the capacitor (COVT) connected between the COVT terminal (pin 14) and GND. At this time, the cell voltage input block switch is turned on to supply the cell voltage input current to that cell so that high-voltage cells are lowered in voltage.

When all the cell voltages in the over-charge detected state become the over-charge release voltage (4.125 V Typ) or less, the COVT terminal (pin 14) and COUT terminal (pin 2) go “L” level to turn on the Pch MOS FET for external charge control.

When any cell voltage in the over-charge detected state becomes the over-charge release voltage (4.125 V Typ) or less, the cell voltage input block switch is turned off.

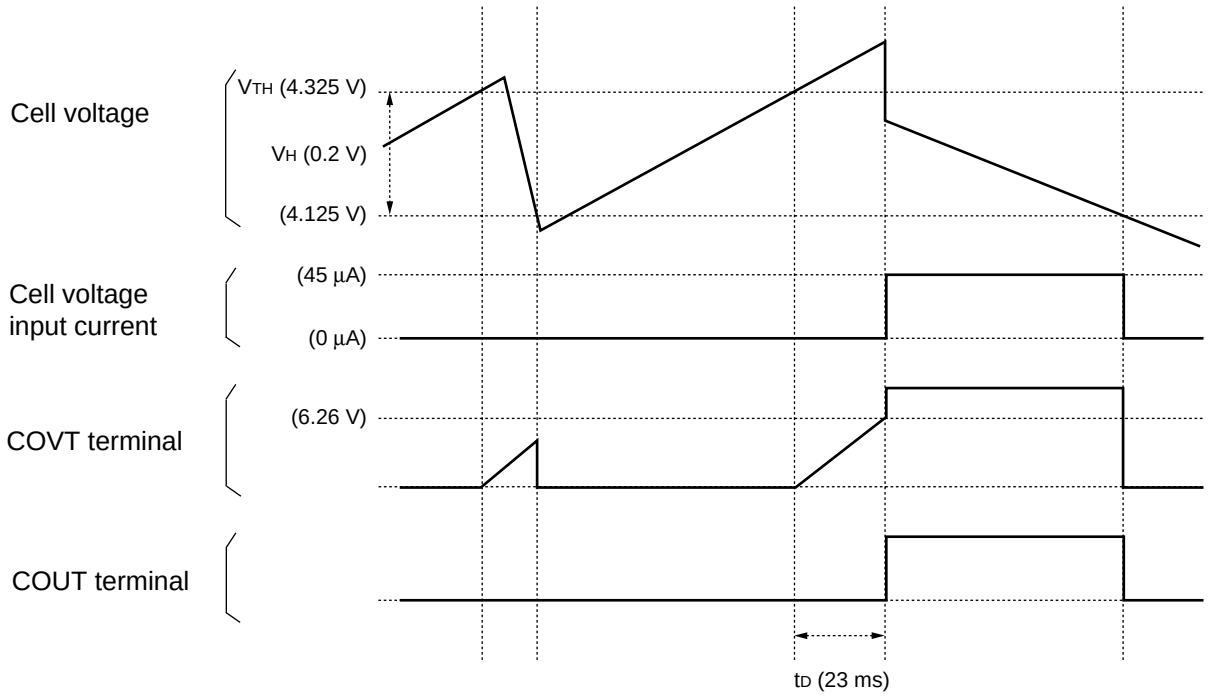


Figure 2

(3) When the OUTON terminal changes "H"→"L"→"H" after detection of an over-charge

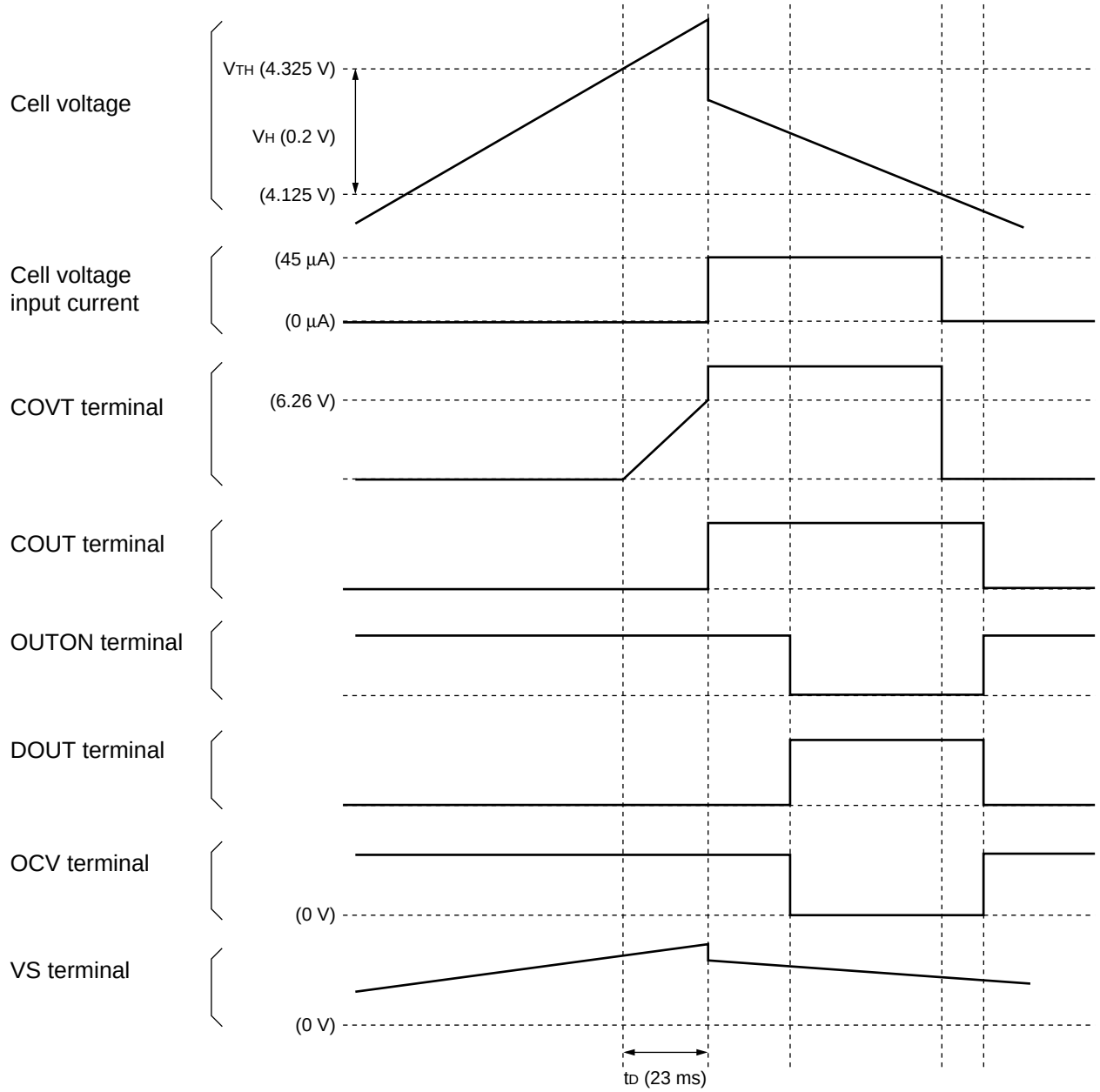


Figure 3

When the OUTON terminal (pin 20) changes from “H” level to “L” level after detection of an over-charge, the DOUT terminal (pin 3) goes “H” level to turn off the Pch MOS FET for external discharge control, thereby setting the OCV terminal (pin 1) to “L” level.

When the OUTON terminal (pin 20) changes from “H” level to “L” level after all the cell voltages in the over-charge detected state become the over-charge release voltage (4.125 V Typ) or less, the COUT terminal (pin 2) goes “L” level to turn on the Pch MOS FET for external charge control. When the OCV terminal (pin 1) changes from “L” level to “H” level at this time, the DOUT terminal (pin 3) goes “L” level to turn on the Pch MOS FET for external discharge control.

2. Over-charge Detection Block, Discharge Detection Block, and Cell Voltage Input Block

- When battery is discharged after detection of an over-charge or re-discharged after detection of an over-charge by recharging

  If a cell voltage reaches or exceeds the over-charge detection voltage (4.325 V Typ), the COUT terminal (pin 2) goes “H” level to turn off the Pch MOS FET for external charge control after a delay time (23 ms Typ) managed by the capacitor (C_{OVT}) connected between the COVT terminal (pin 14) and GND. This stops charging the battery and puts it into the over-charge detected state.

  When a discharge is started in the over-charge detected state, the OCV terminal voltage is lowered by the body diode voltage of the Pch MOS FET for external charge control. When the potential difference between the VCC terminal and OCV terminal (pin 1) becomes 300 mV or more, the COUT terminal (pin 2) goes “L” level to turn on the Pch MOS FET for external charge control and the cell voltage input block switch is turned off at the same time.

  An over-charge caused by recharging can be detected even with cell voltages remaining above the over-charge release voltage (4.125 V Typ).

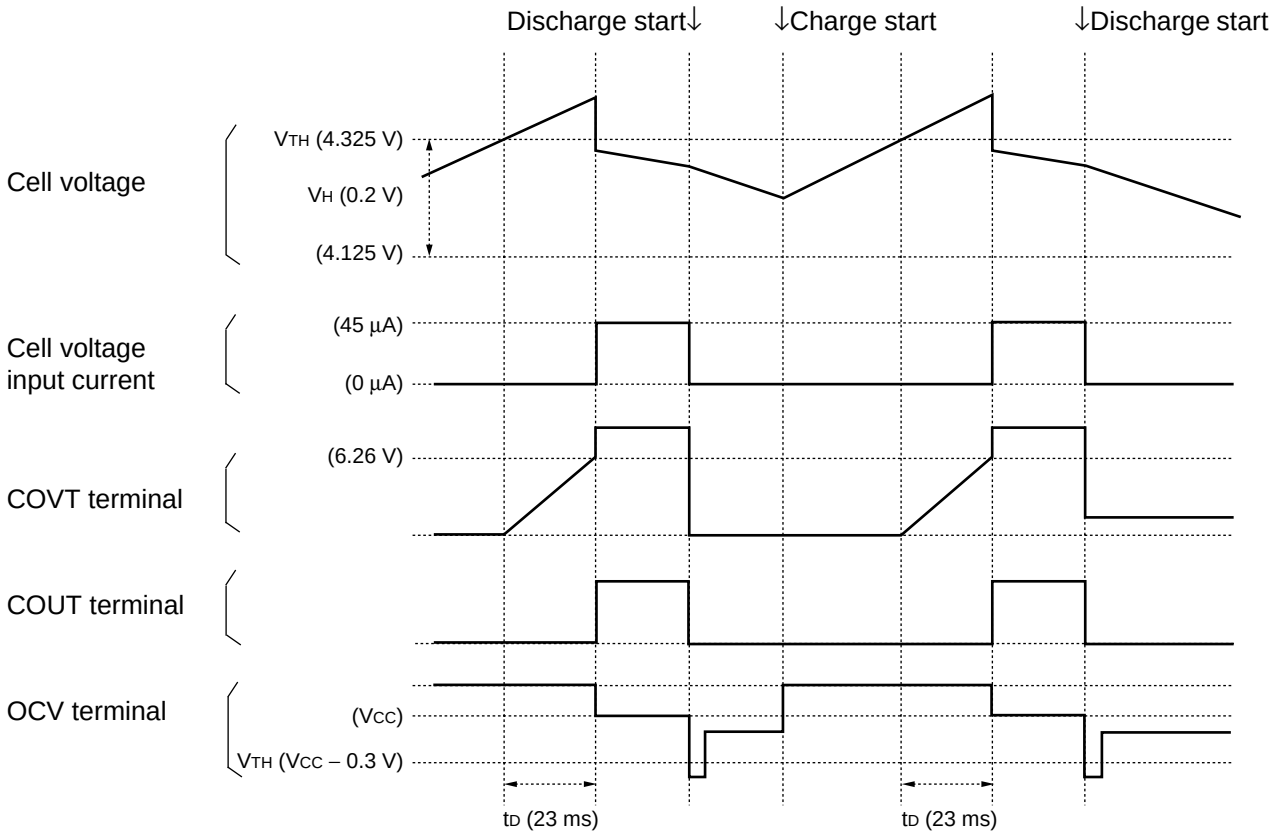


Figure 4

3. Over-discharge Detection/Power Fail Circuit

- When no “H” level signal is input to the PDWN terminal after over-discharge detection

If any cell voltage becomes the over-discharge detection voltage (2.75 V Typ), the PF terminal (pin 19) outputs a “L” level PF signal to the notebook PC after a PF output delay time (2 s Typ) managed by the capacitor (C_{UVT}) connected between the CUVT terminal (pin 12) and GND. At the same time, after a power-down delay time (20 s Typ) managed by the capacitor (C_{PDT}) connected between the CPDT terminal (pin 11) and GND, the DOUT terminal (pin 3) goes “H” level to turn off the Pch MOS FET for external discharge control, thereby stopping discharging the battery. The VS terminal (pin 5) goes “L” level at this time. As discharging is stopped, the OCV terminal (pin 1) goes “L” level to completely turn off the bias source in the IC.

That is, an over-discharge state is detected when a cell voltage does not return to the over-discharge detection voltage (2.75 V Typ) or more within the power-down delay time (20 s Typ), an over-discharge state is detected.

When the OCV terminal (pin 1) goes “H” level, the DOUT terminal (pin 3) goes “L” level to turn on the Pch MOS FET for external discharge control and the VS terminal (pin 5) goes “H” level. If the cell voltage remains not exceeding the over-discharge detection voltage (2.75 V Typ) at this time, the PF terminal (pin 19) outputs a “L” level PF signal to the notebook PC again after a PF output delay time (2 s Typ) managed by the capacitor (C_{UVT}) connected between the CUVT terminal (pin 12) and GND. If the cell voltage reaches or exceeds the over-discharge detection voltage (2.75 V Typ) within the power-down delay time (20 s Typ), however, the PF terminal goes “H” level and an over-discharge state is not detected.

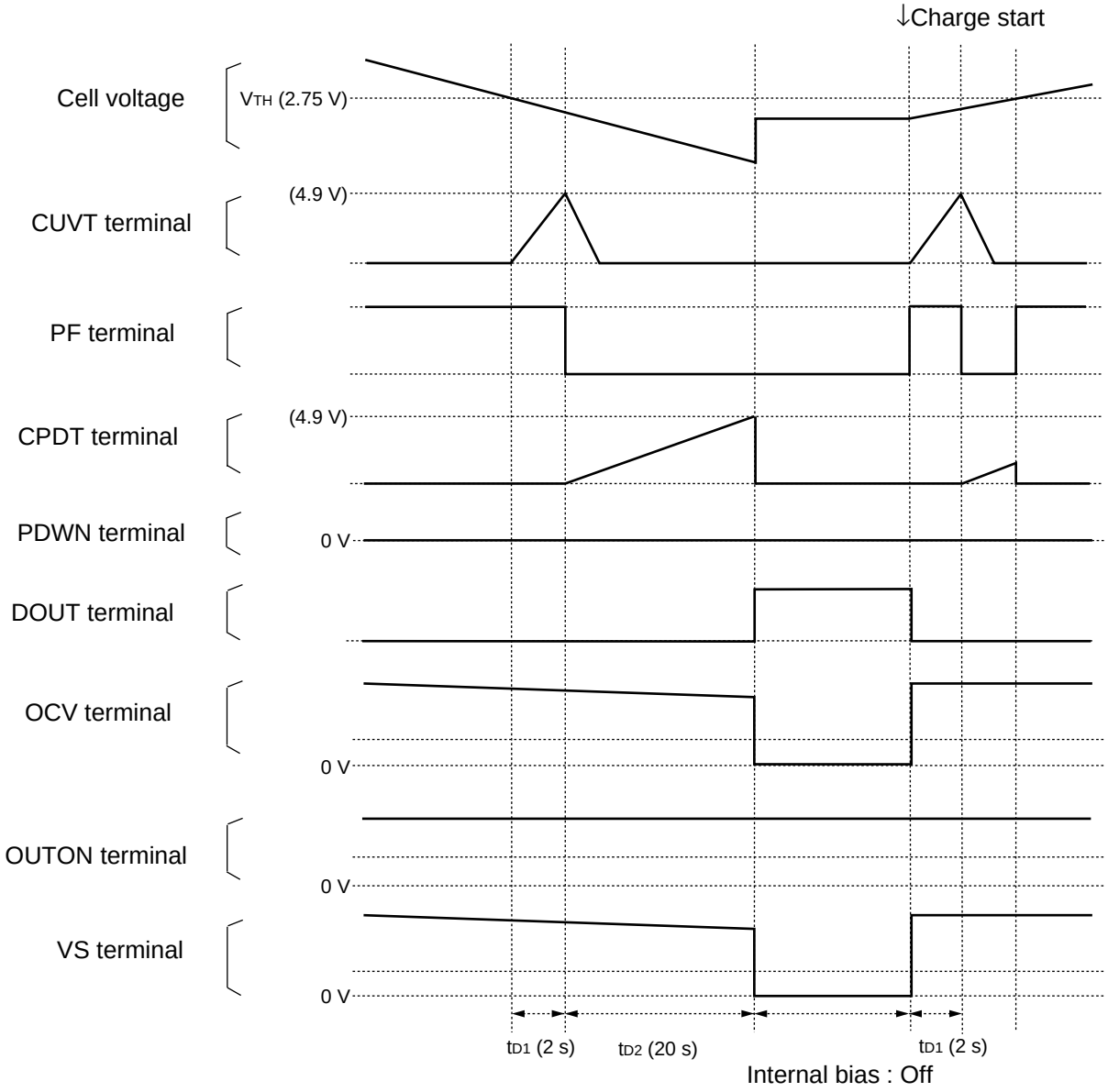

↓Charge start
Cell voltage
VTH (2.75 V)
CUVT terminal
(4.9 V)
PF terminal
CPDT terminal
(4.9 V)
PDWN terminal
0 V
DOUT terminal
OCV terminal
0 V
OUTON terminal
0 V
VS terminal
0 V
tD1 (2 s)
tD2 (20 s)
tD1 (2 s)
Internal bias : Off

Figure 5

4. Over-current Detection Block 1

When a discharge current is relatively small as an over-current, if the potential difference between the VCC terminal and OCV terminal (pin 1) by RON of the Pch MOS FET for external charge control becomes 300 mV or more, the capacitor (C_{OCT}) connected between the COCT terminal (pin 13) and GND is charged. No over-current is detected if the OCV terminal voltage returns to the battery voltage level within the delay time (7 ms Typ). If the potential difference between the VCC terminal and OCV terminal (pin 1) by RON of the Pch MOS FET for external charge control becomes 300 mV or more again, an over-current is detected after a delay time (7 ms Typ) managed by the capacitor (C_{OCT}) connected between the COCT terminal (pin 13) and GND. At this time, the DOUT terminal (pin 3) goes “H” level to turn off the Pch MOS FET for external discharge control and the bias source in the IC is completely turned off as well.

Recharging can be restarted by setting the OCV terminal (pin 1) to “H” level to set the DOUT terminal (pin 3) to “L” level and VS terminal (pin 5) to “H” level, respectively.

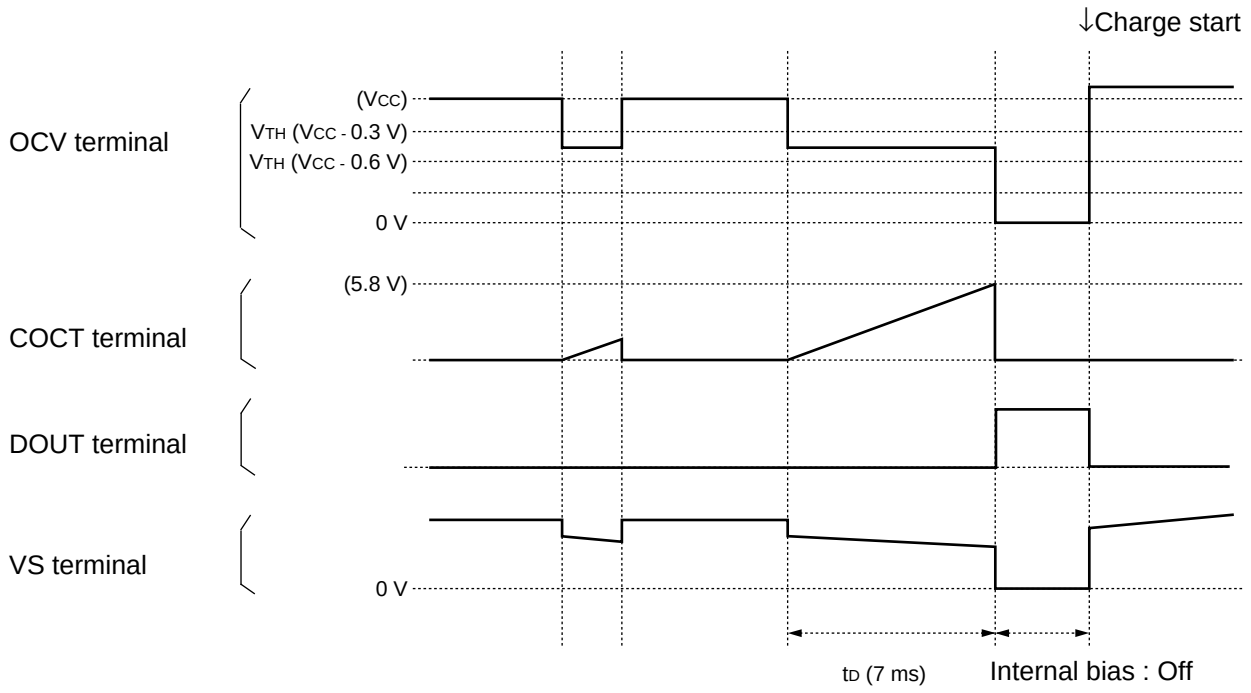


Figure 6

5. Over-current Detection Block 2

When a discharge current is relatively large as an over-current, if the potential difference between the VCC terminal and OCV terminal (pin 1) by RON of the Pch MOS FET for external charge control becomes 300 mV or more, the capacitor (C_{OCT}) connected between the COCT terminal (pin 13) and GND is charged. No over-current is detected if the OCV terminal voltage returns to the battery voltage level within the delay time (7 ms Typ). If the potential difference between the VCC terminal and OCV terminal (pin 1) of the Pch MOS FET for external charge control becomes 600 mV or more, an over-current is detected after a delay time (500 ms Typ) managed by the capacitor (C_{OCT}) connected between the COCT terminal (pin 13) and GND. At this time, the DOUT terminal (pin 3) goes “H” level to turn off the Pch MOS FET for external discharge control, both of the VS terminal (pin 5) and OCV terminal (pin 1) go “L” level, and the bias source in the IC is completely turned off as well.

Recharging can be restarted by setting the OCV terminal (pin 1) to “H” level to set the DOUT terminal (pin 3) to “L” level and VS terminal (pin 5) to “H” level, respectively.

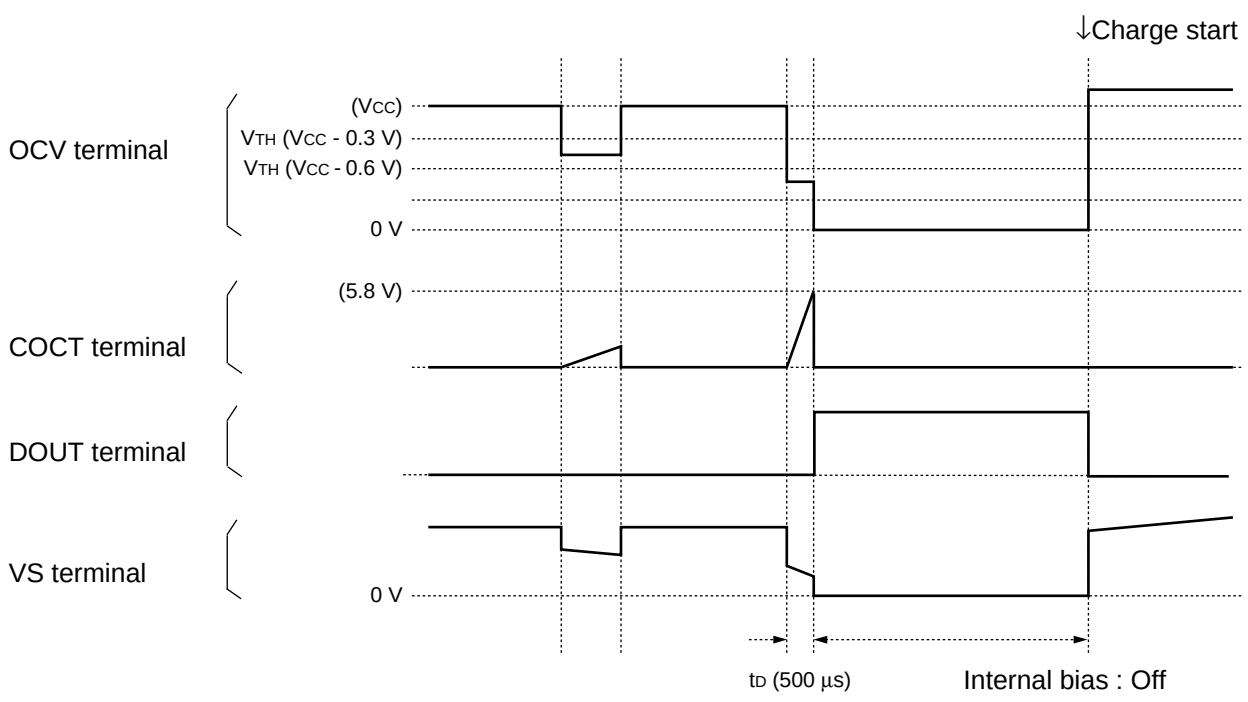
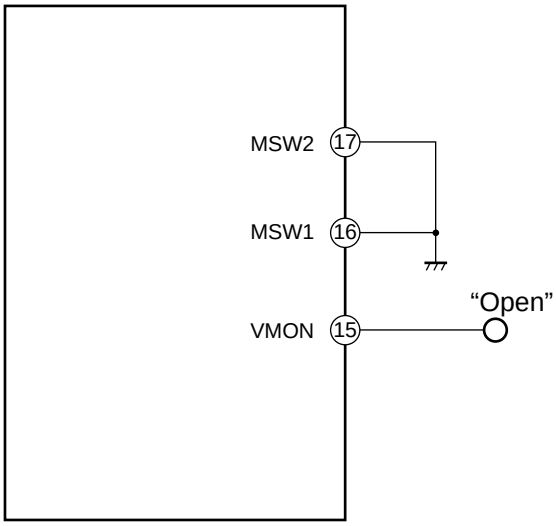


Figure 7

■ TREATMENT WHEN VOLTAGE MONITOR FUNCTION IS NOT USED

When the voltage monitor function is not used, connect the MSW1 terminal (pin 16) and MSW2 terminal (pin 17) to GND by taking their shortest ways and leave the VMON terminal (pin 15) open.



When voltage monitor function is not used

■ NOTE ON VS TERMINAL

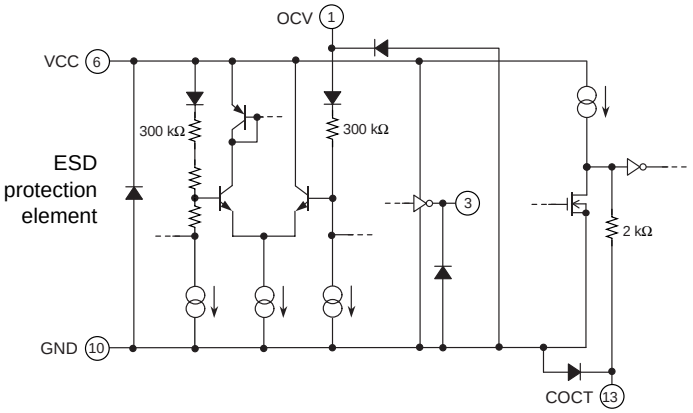
If the battery is charged through the body diode of the internal Pch MOS FET connected to the VS terminal (pin 5), the over-charge protection function cannot be disabled. Be careful not to apply a voltage equal to or higher than the VCC terminal voltage to the VS terminal.

■ NOTE ON ELECTROSTATIC APPLICATION

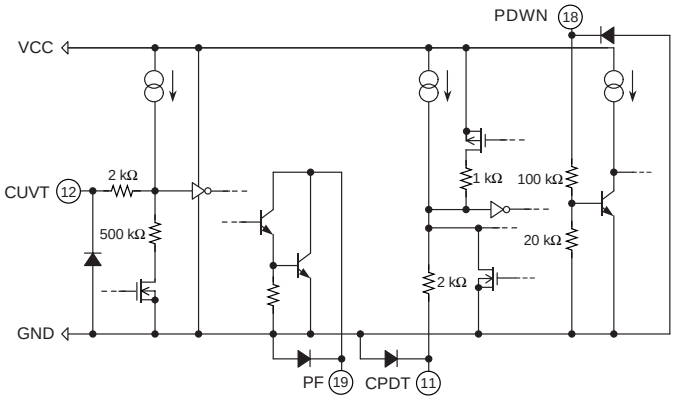
This IC has a built-in function to set ICC to 0 μA in power-down mode to extend the battery life. As a charger is required to return the IC from power-down mode, use meticulous care not to let it malfunction, for example, with applied static electricity. To prevent electrostatic noise from coming into each input pin of the IC, it is advisable to lower impedance, for example, by adding a capacitor. The capacitor used for this purpose should be placed as close to the IC as possible.

■ I/O TERMINAL EQUIVALE CIRCUIT

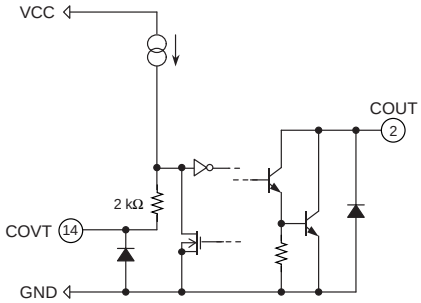
[Over-current detection block]



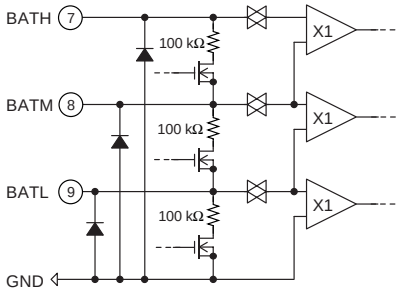
[Over-discharge detection/power fail circuit block]



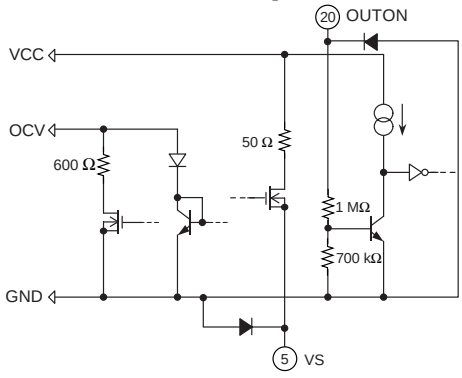
[Over-charge detection block]



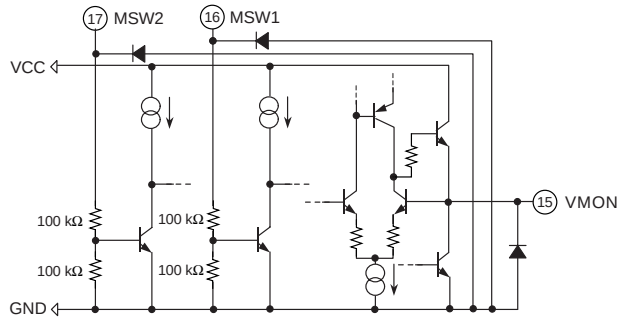
[Cell voltage input block]



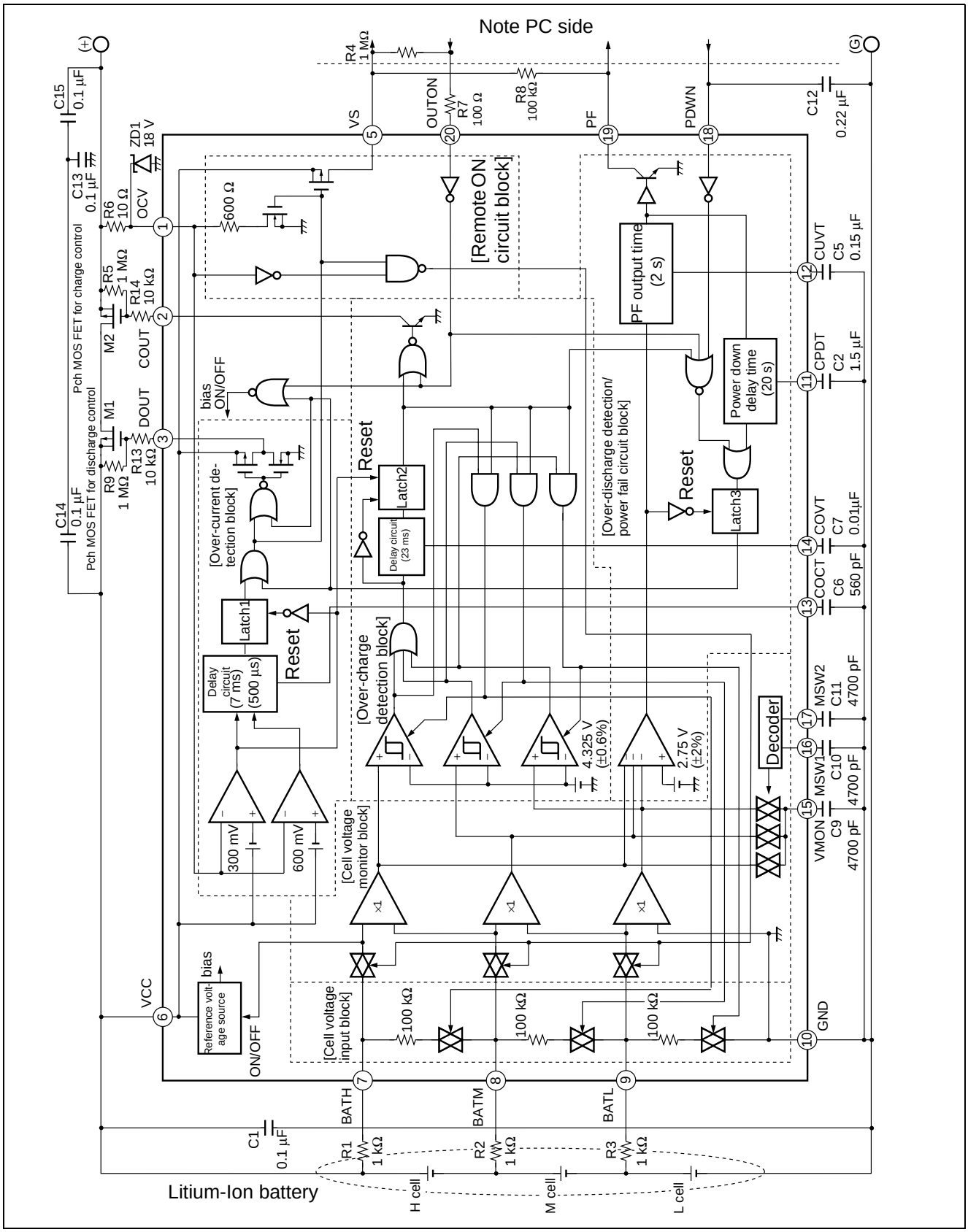
[Remote ON circuit block]



[Cell voltage monitor block]



■ APPLICATION EXAMPLE



■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
M1, M2	FET	VDS = –30 V		VISHAY SILICONIX	Si4425DY
ZD1	Diode	200 mW, 18 V ± 7%		TOSHIBA	02CZ18-Y
C1	Ceramics Condenser	0.1 µF	25 V (10%)	—	—
C2	Ceramics Condenser	1.5 µF	16 V (10%)		
C5	Ceramics Condenser	0.15 µF	16 V (10%)		
C6	Ceramics Condenser	560 pF	50 V (5%)		
C7	Ceramics Condenser	0.01 µF	25 V (10%)		
C9, C10, C11	Ceramics Condenser	4700 pF	25 V (10%)		
C12	Ceramics Condenser	0.22 µF	25 V (10%)		
C13, C14, C15	Ceramics Condenser	0.1 µF	25 V (10%)		
R1, R2, R3	Resistor	1 kΩ	1/16 W, 5%	—	—
R4, R5, R9	Resistor	1 MΩ	1/16 W, 5%		
R6	Resistor	10 Ω	1/16 W, 5%		
R7	Resistor	100 Ω	1/16 W, 5%		
R8	Resistor	100 kΩ	1/16 W, 5%		
R13, R14	Resistor	10 kΩ	1/16 W, 5%		

Note: VISHAY SILICONIX : VISHAY Intertechnology, Inc.
TOSHIBA : TOSHIBA CORPORATION

■ USAGE PRECAUTION

- Printed circuit board ground lines should be set up with consideration for common impedance.
- Take appropriate static electricity measures.
  - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
  - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
  - Work platforms, tools, and instruments should be properly grounded.
  - Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

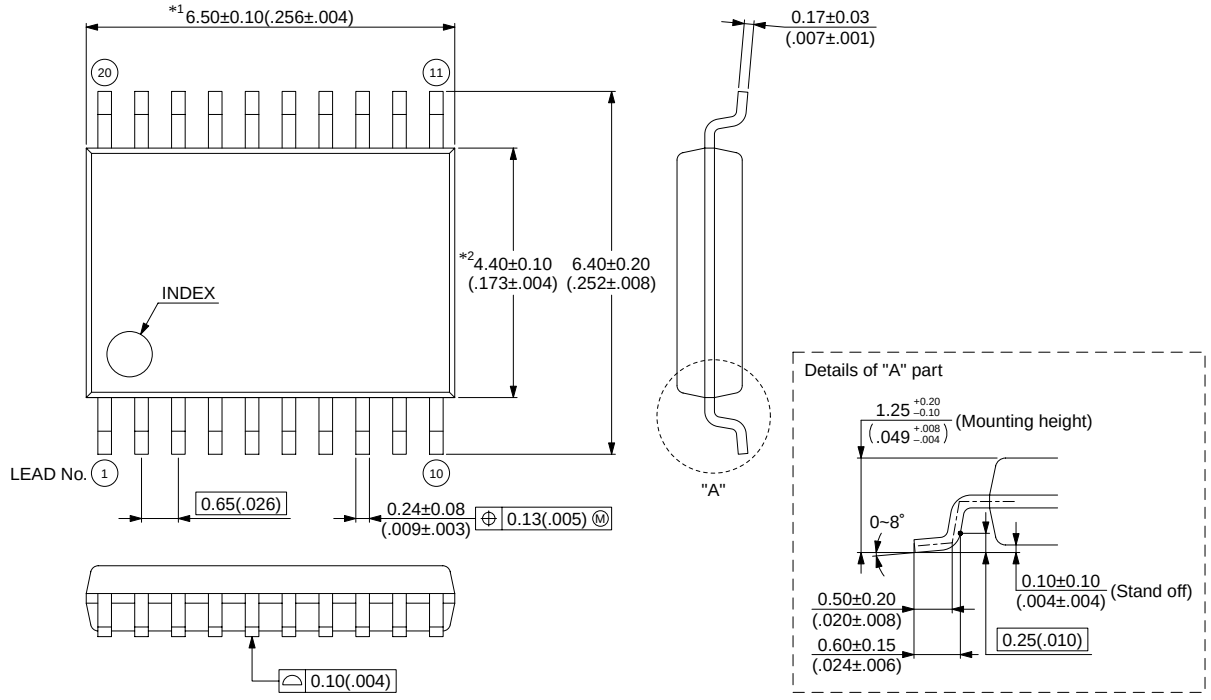
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3836PFV	20-pin plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSION

20-pin plastic SSOP
(FPT-20P-M03)

Note 1) *1: Resin protrusion. (Each side: +0.15 (.006) Max).
Note 2) *2: These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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