NXP 30 MHz 32-bit Cortex-M0+ MCU LPC800

A 32-bit microcontroller designed for the 8-bit world

The LPC800 combines the simplicity and ease of use of 8-bit micros, the versatility of 32-bit micros and a set of peripherals that will change the way designers look at flexibility and scalability. Every peripheral on this chip was redesigned from the ground up with the low-cost 8-bit market in mind.

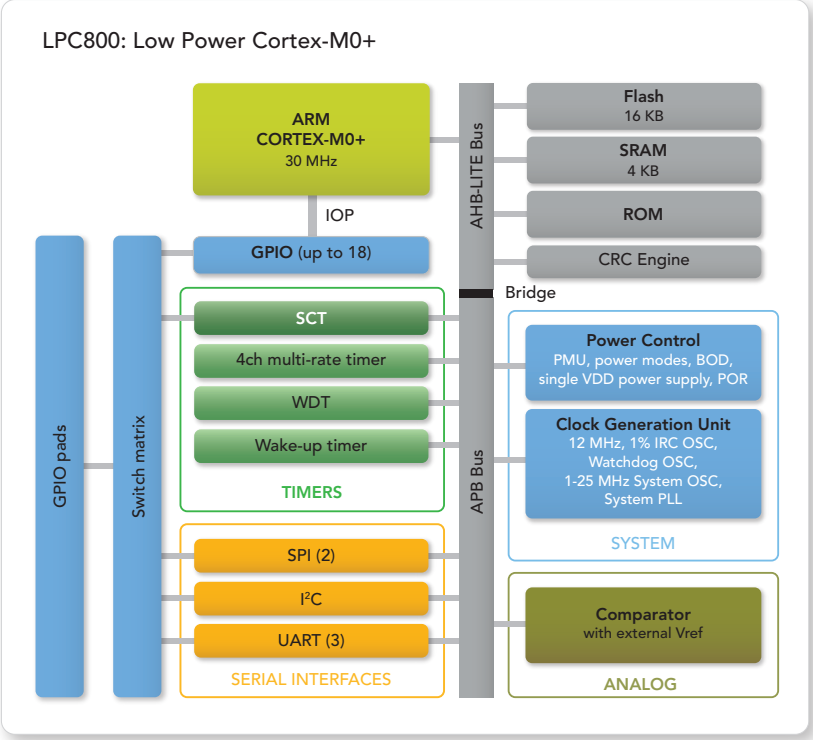
Key features

- ARM Cortex-M0+™ processor
  - Up to 30 MHz
  - Backward compatibility to the Cortex-M0™
  - Upwards compatibility with Cortex-M3™ and Cortex-M4™
  - Nested Vectored Interrupt Controller (NVIC)
  - Serial Wire Debug (SWD) and JTAG boundary scan modes
  - Micro Trace Buffer (MTB)
  - Single Cycle Access to all port pins
- Memories:
  - Up to 16 kB Flash (with 64 Byte page size)
  - 4 kB SRAM
- Serial Peripherals
  - Three USART interfaces
  - Two SPI controllers
  - One I²C-bus interface
- Timers
  - Multiple-channel multi-rate timer (MRT)
  - State Configurable Timer (SCT)
  - Self Wake-up Timer (WKT) clocked from either the IRC or a low-power clock source
  - Windowed Watchdog timer (WWDT)
  - System tick timer
- Analog peripherals
  - Comparator with external voltage reference
- I/O
  - Switch matrix for flexible configuration of each I/O pin function
  - Up to 18 General-Purpose I/O (GPIO) pins
  - GPIO interrupt generation capability with boolean pattern-matching capability
  - Digital glitch filter with programmable time constant
- Clock Generation Unit
  - 12 MHz internal RC oscillator trimmed to 1% accuracy
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz
  - Programmable watchdog oscillator
  - 10 kHz low-power oscillator for the WKT.
  - PLL allows max CPU rate without a high-frequency crystal.
- Other
  - ROM drivers for I²C, USART, power profiles, ISP, and IAP
  - Easy to use low pin-count TSSOP and DIP packages
  - CRC engine
  - Single VDD power supply (1.8 V to 3.6 V)

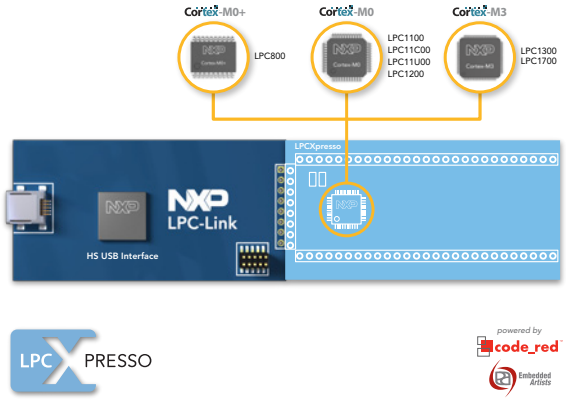
The LPC800 family is extremely power-efficient and straightforward to use. Based on an ultra-low-power 30-MHz ARM® Cortex-M0+ processor, the LPC800 is fully compatible with the Cortex-M architecture and instruction set. The Cortex-M0+ handles 32-bit data more efficiently than 8-bit processor by requiring less code, memory and 30% less dynamic power from the Cortex-M0+ processor. At the same time, it easily outperforms 8-bit and 16-bit MCUs.

The LPC800 includes two innovative features controlled via GUI-based configuration tools. A new flexible switch matrix enables designers to assign on-chip peripherals to any pin, giving the LPC800 enormous flexibility without adding complexity. The State Configurable Timer (SCT) combines a powerful 32-bit timer — or two 16-bit timers — with a configurable state machine. In the LPC800, the SCT implements virtually any timing or PWM function found on popular 8-bit MCUs.

The LPC800 is available in a range of low-pin-count packages, including SO20, TSSOP20, TSSOP16, and DIP8.



LPC800 block diagram



LPCXpresso development tool

Development tools

LPCXpresso, the full-featured, easy-to-use Eclipse-based software development tool, supports the complete product design cycle for the LPC800. The LPC800 is also fully supported by the Keil-MDK by ARM, the Embedded Workbench from IAR Systems, as well as other third party development tools. Additional support, free tools, and sample code are available on the web at www.lpcware.com. For further information on LPCXpresso, visit www.nxp.com/lpcxpresso.

Ordering information

Final Part Number	SRAM	Flash	Package	I²C	SPI	UART	SCT	MRT	Comp	Comp. Vref	GPIO
LPC810 M021FN8	1	4	DIP8	1	1	2	1	1, 4ch	1		6
LPC811 M001FDH16	2	8	TSSOP16	1	1	2	1	1, 4ch	1	•	14
LPC812 M101FDH16	4	16	TSSOP16	1	2	3	1	1, 4ch	1	•	14
LPC812 M101FD20	4	16	SO20	1	1	2	1	1, 4ch	1	•	18
LPC812 M101FDH20	4	16	TSSOP20	1	2	3	1	1, 4ch	1	•	18

LPCware NXP MCU COMMUNITY www.lpcware.com

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