19-6400; Rev 0; 7/12

MAX71020

Single-Chip Electricity Meter AFE

General Description

The MAX71020 is a single-chip, analog front-end to be used in high-performance revenue meters. It contains the compute engine found in Maxim's fourth-generation meter SOC and an improved ADC, and interfaces to the host microcontroller of choice over a SPI interface.

The MAX71020 comes in a 28-pin TSSOP package.

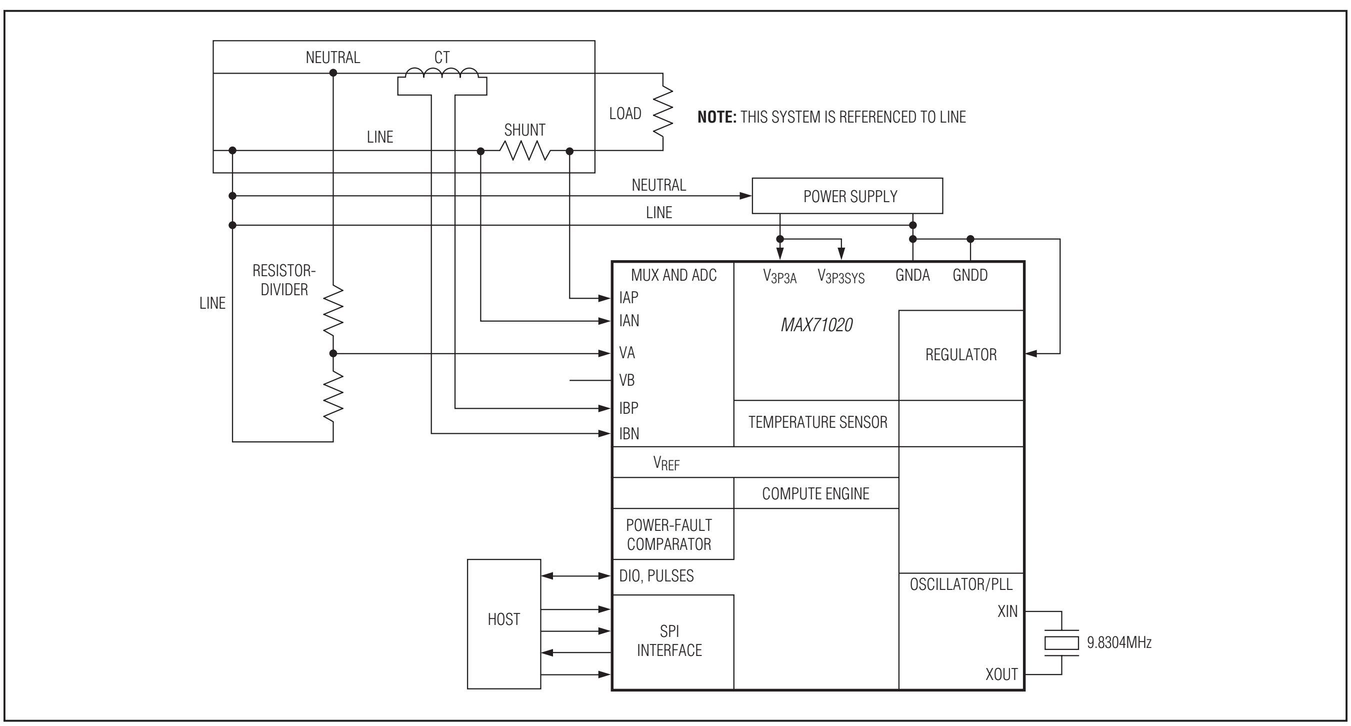
***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to ***www.maxim-ic.com/MAX71020.related****.*

Features

- ♦ **0.1% Accuracy Over 2000:1 Current Range**
- ♦ **Exceeds IEC 62053/ANSI C12.20 Standards**
- ♦ **Two Differential Current Sensor Inputs**
- ♦ **Two Voltage Sensor Inputs**
- ♦ **Selectable Gain of 1 or 9 for One Current Input to Support a Shunt**
- ♦ **High-Speed Wh/VARh Pulse Outputs with Programmable Width**
- ♦ **Up to Four Pulse Outputs with Pulse Count**
- ♦ **Four-Quadrant Metering**
- ♦ **Digital Temperature Compensation**
- ♦ **Independent 32-Bit Compute Engine**
- ♦ **45Hz to 65Hz Line Frequency Range with Same Calibration**
- ♦ **Phase Compensation (±10°)**
- ♦ **Four Multifunction DIO Pins**
- ♦ **SPI Interface**
- ♦ **-40°C to +85°C Industrial Temperature Range**
- ♦ **28-Pin TSSOP Lead(Pb)-Free Package**

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

(All voltages with respect to GNDA.)

Voltage and Current Supplies and Ground Pins

V_{3P3SYS}, V_{3P3A} .... -0.5V to +4.6V
GNDD .... -0.1V to +0.1V

Analog Input Pins

IAP, IAN, IBP, IBN, VA, VB .... (-10mA to +10mA), (-0.5V to (V_{3P3A} + 0.5V))
XIN, XOUT .... (-10mA to +10mA), (-0.5V to +3.0V)

Digital Pins

Inputs .... (-10mA to +10mA), (-0.5V to +6V)
Outputs .... (-10mA to +10mA), (-0.5V to (V_{3P3SYS} + 0.5V))

Temperature and ESD Stress

Operating Junction Temperature (peak, 100ms) .... 140°C
Operating Junction Temperature (continuous) .... 125°C
Storage Temperature Range .... -45°C to +165°C
ESD Stress on All Pins .... ±4kV, HBM
Lead Temperature (soldering, 10s) .... 300°C
Soldering Temperature (reflow) .... +250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 78°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 13°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS					
V_{3P3SYS} and V_{3P3A} Supply Voltage	Precision metering operation	3.0		3.6	V
	Digital operation	2.8		3.6	
Operating Temperature		-40		+85	°C
INPUT LOGIC LEVELS					
Digital High-Level Input Voltage (V_{IH})		2			V
Digital Low-Level Input Voltage (V_{IL})				0.8	V
Input Pullup Current (I_{IL}) RESETZ	$V_{V3P3SYS}$ = 3.6V, V_{IN} = 0V	41	78	115	µA
Input Pullup Current (I_{IL}) Other Digital Inputs	$V_{V3P3SYS}$ = 3.6V, V_{IN} = 0V	-1	0	+1	µA
Input Pulldown Current (I_{IH}) All Pins	VIN = V3P3SYS	-1	0	+1	µA
OUTPUT LOGIC LEVELS					
Digital High-Level Output Voltage (V_{OH})	I_{LOAD} = 1mA	V_{3P3SYS} - 0.4			V
	I_{LOAD} = 15mA (Note 2)	V_{3P3SYS} - 1.1			
Digital Low-Level Output Voltage (V_{OL})	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 15mA (Note 2)	0		0.96	
TEMPERATURE MONITOR					
TNOM (Nominal Value at 22°C)	V_{V3P3A} = 3.3V		956		LSB

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Measurement Equation		Temp = 0.33 x STEMP + 21.77			°C
Temperature Error (Note 2)	T_A = -40°C to +85°C	-6		+6	°C
	T_A = -20°C to +60°C	-4.8		+4.8	
Duration of Temperature Measurement After Setting TEMP_START	TEMP_PER = 0		15	60	ms
SUPPLY CURRENT PERFORMANCE SPECIFICATIONS					
V_{3P3A} + V_{3P3SYS} Current (Note 2)	V_{V3P3A} = $V_{V3P3SYS}$ = 3.3V, CE_E = 1, ADC_E = 1			4.3	mA
INTERNAL POWER-FAULT COMPARATOR SPECIFICATIONS					
Overall Response Time	100mV overdrive, falling	20		200	µs
	100mV overdrive, rising	8		200	
Falling Threshold	3.0V comparator	2.83	2.93	3.03	V
	2.8V comparator	2.75	2.81	2.89	V
	Difference 3.0V and 2.8V comparators	50	136	220	mV
Hysteresis (Rising Threshold - Falling Threshold)	3.0V comparator, T_A = +22°C	17	45	74	mV
	2.8V comparator, T_A = +22°C	15	42	70	
PLL PERFORMANCE SPECIFICATIONS					
PLL Power-Up Settling Time	V_{V3P3A} = 0 to 3.3V step, measured from first edge of MCK		75		µs
PLL_FAST Settling Time	V_{V3P3A} = 3.3V, PLL_FAST rise		10		µs
	V_{V3P3A} = 3.3V, PLL_FAST fall		10		
PLL Lock Frequency at XOUT	V_{V3P3A} = 3.3V, MCK frequency error < 1%	7	9.8	13	MHz
VREF PERFORMANCE SPECIFICATIONS					
VREF Output Voltage, VREF (22)	T_A = +22°C	1.200	1.205	1.210	V
VREF Power-Supply Sensitivity ($\Delta V_{REF}/\Delta V_{3P3A}$)	V_{3P3A} = 3.0V to 3.6V	-1.5		+1.5	mV/V
VNOM Definition		VNOM(T) = VREF(22) + TC1(T - 22) + TC2(T - 22)^2			V
VNOM Temperature Coefficient TC1		29.32 - 1.05 x TRIMT			µV/°C
VNOM Temperature Coefficient TC2		-0.56 - 0.004 x TRIMT			µV/°C^2
VREF(T) Deviation from VNOM(T): $\frac{VREF(T) - VNOM(T)}{VNOM(T)} \frac{10^6}{62}$	(Note 2)	-40		+40	ppm/°C
ADC CONVERTER PERFORMANCE SPECIFICATIONS					
Recommended Input Range (With Respect to GNDA)	VA, VB, IBP, IBN	-250		+250	mV peak

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Recommended Input Range (With Respect to GNDA)	IAP, IAN (preamplifier enabled)		-27.78		+27.78	mV peak
Input Impedance, No Preamplifier	f_{IN} = 65Hz		50		100	kΩ
ADC Gain Error vs Percentage Power-Supply Variation $\frac{10^6 \Delta Nout_{PK} 357nV / V_{IN}}{100 \Delta V3P3A / 3.3}$	V_{IN} = 200mV peak, 65Hz V_{V3P3A} = 3.0V, 3.6V				81	ppm/%
Input Offset	IAP = IAN = GNDA		-10		+10	mV
Total Harmonic Distortion at 250mVpk	V_{IN} = 55Hz, 250mVpk, 64kpts FFT, Blackman Harris Window			-85		dB
Total Harmonic Distortion at 20mVpk	V_{IN} = 55Hz, 20mVpk, 64kpts FFT, Blackman Harris Window			-85		dB
LSB Size (LSB Values Do Not Include the 9-Bit Left Shift at the CE Input)	V_{IN} = 55Hz, 20mVpk, 64kpts FFT, Blackman-Harris window, 10MHz CKADC	FIRLEN = 15		120.46		nV
		FIRLEN = 14		146.20		
		FIRLEN = 13		179.82		
		FIRLEN = 12		224.59		
		FIRLEN = 11		285.54		
		FIRLEN = 10		370.71		
Digital Full Scale	V_{IN} = 55Hz, 400mVpk, 10MHz CKADC	FIRLEN = 15		±2621440		LSB
		FIRLEN = 14		±2160000		
		FIRLEN = 13		±1756160		
		FIRLEN = 12		±1406080		
		FIRLEN = 11		±1105920		
		FIRLEN = 10		±851840		
PREAMPLIFIER PERFORMANCE SPECIFICATIONS						
Differential Gain, (V_{IN} = 28mV Differential)	T_A = +25°C, V_{V3P3A} = 3.3V, PRE_E = 1, DIFF0_E = 1			8.9		V/V
Differential Gain (V_{IN} = 15mV Differential)						
Gain Variation vs. V_{3P3} (V_{IN} = 28mV Differential)	V_{V3P3A} = 3.0V, 3.6V			-72		ppm/%
Gain Variation vs. Temperature (V_{IN} = 28mV Differential) (Note 4)	T_A = -40°C to +85°C			-45		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

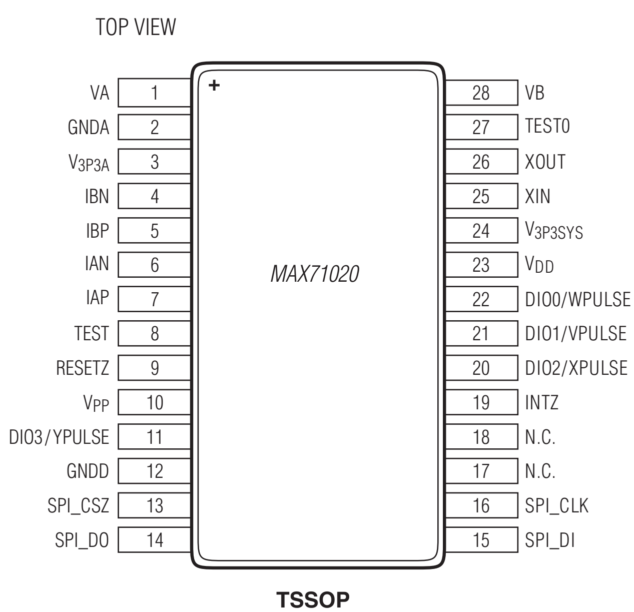
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Phase Shift (V_{IN} = 28mV Differential) (Note 2)	T_A = +25°C, V_{V3P3A} = 3.3V	0		8	m°
Preamplifier Input Current (I_{ADC0}) Preamplifier Input Current (I_{ADC1})	PRE_E = 1, DIFF0_E = 1, IADC0 = IADC1 = V_{3P3A}	9	15	20	µA
Preamplifier and ADC Total Harmonic (V_{IN} = 28mV Differential)	T_A = +25°C; V_{V3P3A} = 3.3V, PRE_E = 1, DIFF0_E = 1		-80		dB
Preamplifier and ADC Total Harmonic Distortion (V_{IN} = 15mV Differential)	T_A = +25°C; V_{V3P3A} = 3.3V, PRE_E = 1, DIFF0_E = 1		-85		dB
SPI SLAVE TIMING SPECIFICATIONS					
SPI Setup Time	SPI_DI to SPI_CK rise	10			ns
SPI Hold Time	SPI_CLK rise to SPI_DI	10			ns
SPI Output Delay	SPI_CLK fall to SPI_D0			40	ns
SPI Recovery Time	SPI_CSZ fall to SPI_CLK	10			ns
SPI Removal Time	SPI_CLK to SPI_CSZ rise	15			ns
SPI Clock High		40			ns
SPI Clock Low		40			ns
SPI Clock Frequency				10	MHz
SPI Transaction Space (SPI_CSZ Rise to SPI_CSZ Fall)		1			µs
RESETZ TIMING					
Reset Pulse Width	Following power-on	1			ms
	At all other times	5			µs
Reset Pulse Rise Time (Note 2)				1	µs
VOLTAGE MONITOR					
Nominal value at +22°C (VNOM)	V_{V3P3A} = 3.3V		130		LSB
Voltage Measurement Equation			V_{V3P3}(CALC) = 3.29V + (BSENSE – 130) x 0.025V + STEMP x 242µV		
Voltage Error $100 \times \left(\frac{V_{V3P3}(CALC)}{V_{V3P3}} - 1 \right)$		-4		+4	%

Note 2: Guaranteed by design, not production tested.
Note 3: V_{3P3SYS} and V_{3P3A} must be connected together.
Note 4: AGND and DGND must be connected together.

RECOMMENDED EXTERNAL COMPONENTS

NAME	FROM	TO	FUNCTION	VALUE	UNITS
C1	V_{3P3A}	GNDA	Bypass capacitor for 3.3V supply	≥ 0.1 ±20%	µF
CSYS	V_{3P3SYS}	GNDD	Bypass capacitor for V_{3P3SYS}	≥ 1.0 ±30%	µF
C1P8	V_{DD}	GNDD	Bypass capacitor for V1P8 regulator	0.1 ±20%	µF
XTAL	XIN	XOUT	At cut crystal specified for 18pF load	9.8304	MHz
CXS	XIN	GNDA	Load capacitor values for crystal depend on crystal specifications and board parasitics. Nominal values are based on 4pF board capacitance and include an allowance for chip capacitance.	32 ±10%	pF
CXL	XOUT	GNDA		32 ±10%	pF

Pin Configuration



Pin Description

(Pin types: P = Power, O = Output, I = Input, I/O = Input/Output. The circuit number denotes the equivalent circuit, as specified under Figure 1).

PIN	NAME	TYPE	CIRCUIT	DESCRIPTION
POWER AND GROUND PINS				
2	GNDA	P	—	Analog Ground. GNDA should be connected directly to the ground plane.
3	V_{3P3A}	P	—	Analog Power Supply. A 3.3V power supply should be connected to V_{3P3A}. V_{3P3A} must be the same voltage as V_{3P3SYS}.
12	GNDD	P	—	Digital Ground. GNDD should be connected directly to the ground plane.
23	V_{DD}	O	—	Output of the 1.8V Regulator. A 0.1µF bypass capacitor to ground should be connected to this pin.
24	V_{3P3SYS}	P	—	System 3.3V Supply. V_{3P3SYS} should be connected to a 3.3V power supply.
ANALOG PINS				
7, 6	IAP, IAN	I	6	Differential or Single-Ended Line Current-Sense Inputs. These pins are voltage inputs to the internal ADC. Typically, these pins are connected to the outputs of current sensors. **Unused pins must be tied to GNDA**.
5, 4	IBP, IBN			
1, 28	VA, VB	I	6	Line Voltage Sense Inputs. VA/VB are voltage inputs to the internal ADC. Typically, the pins are connected to the outputs of resistor-dividers. **Unused pins must be tied to GNDA**.
25	XIN	I	8	Crystal Inputs. A 9.8304MHz crystal should be connected to XIN and XOUT.
26	XOUT	O		
DIGITAL PINS				
22	DIO0/WPULSE	I/O	3, 4	Multiple-Use Pins. Configurable as DIO. Alternative functions with proper selection of associated registers are: DIO0 = WPULSE DIO1 = VPULSE
21	DIO1/VPULSE			
20	DIO2/XPULSE			
11	DIO3/YPULSE			
8, 27	TEST, TEST0	I	3	Connect to GNDD
9	RESETZ	I	3	Active-Low Reset
13	SPI_CSZ	I	3	SPI Interface
14	SPI_DO	O	4	
15	SPI_DI	I	3	
16	SPI_CLK	I	3	
19	INTZ	O	4	Active-Low Interrupt Request
OTHER PIN				
10	V_{PP}	I	—	Connect to GNDD

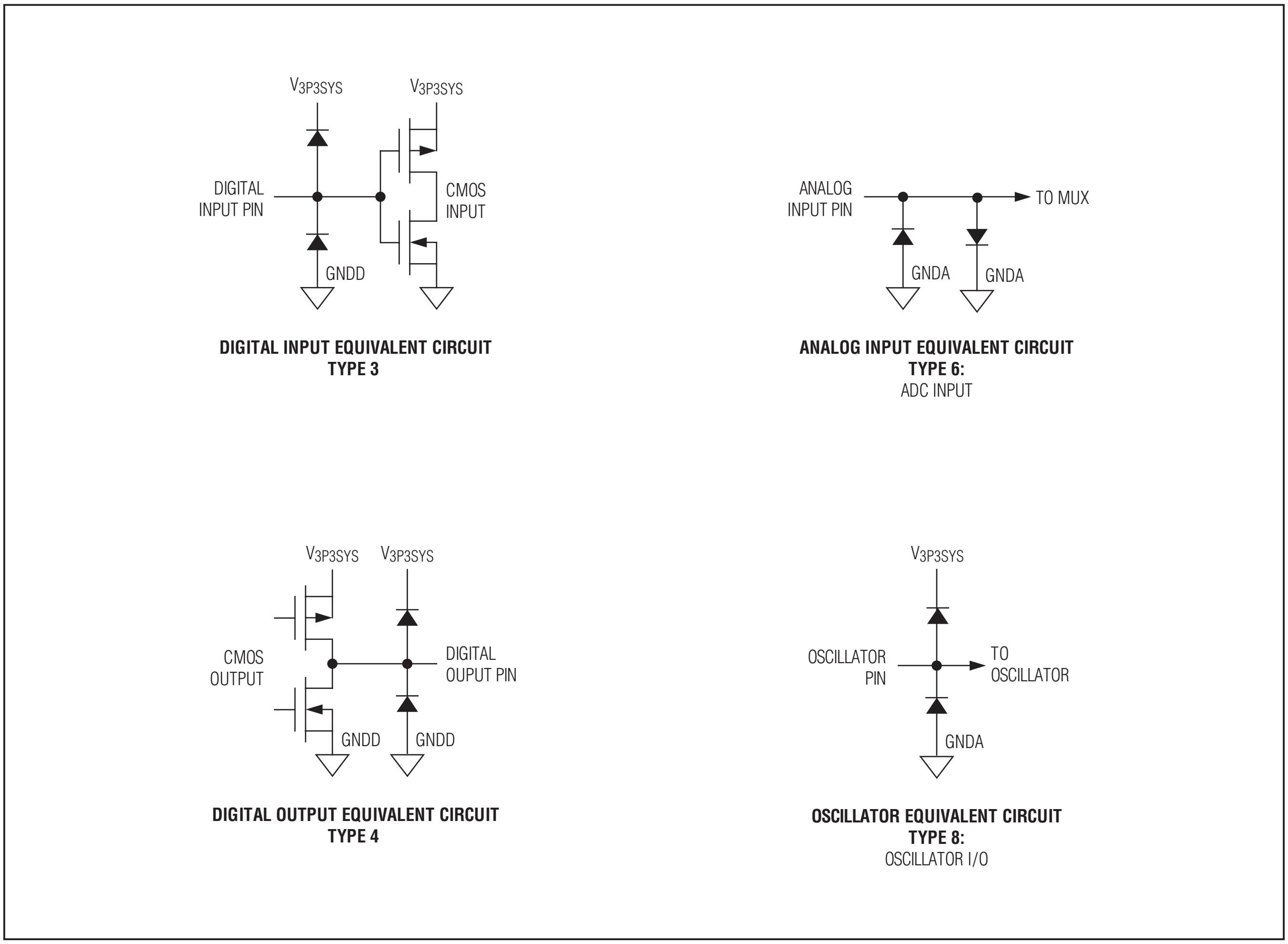
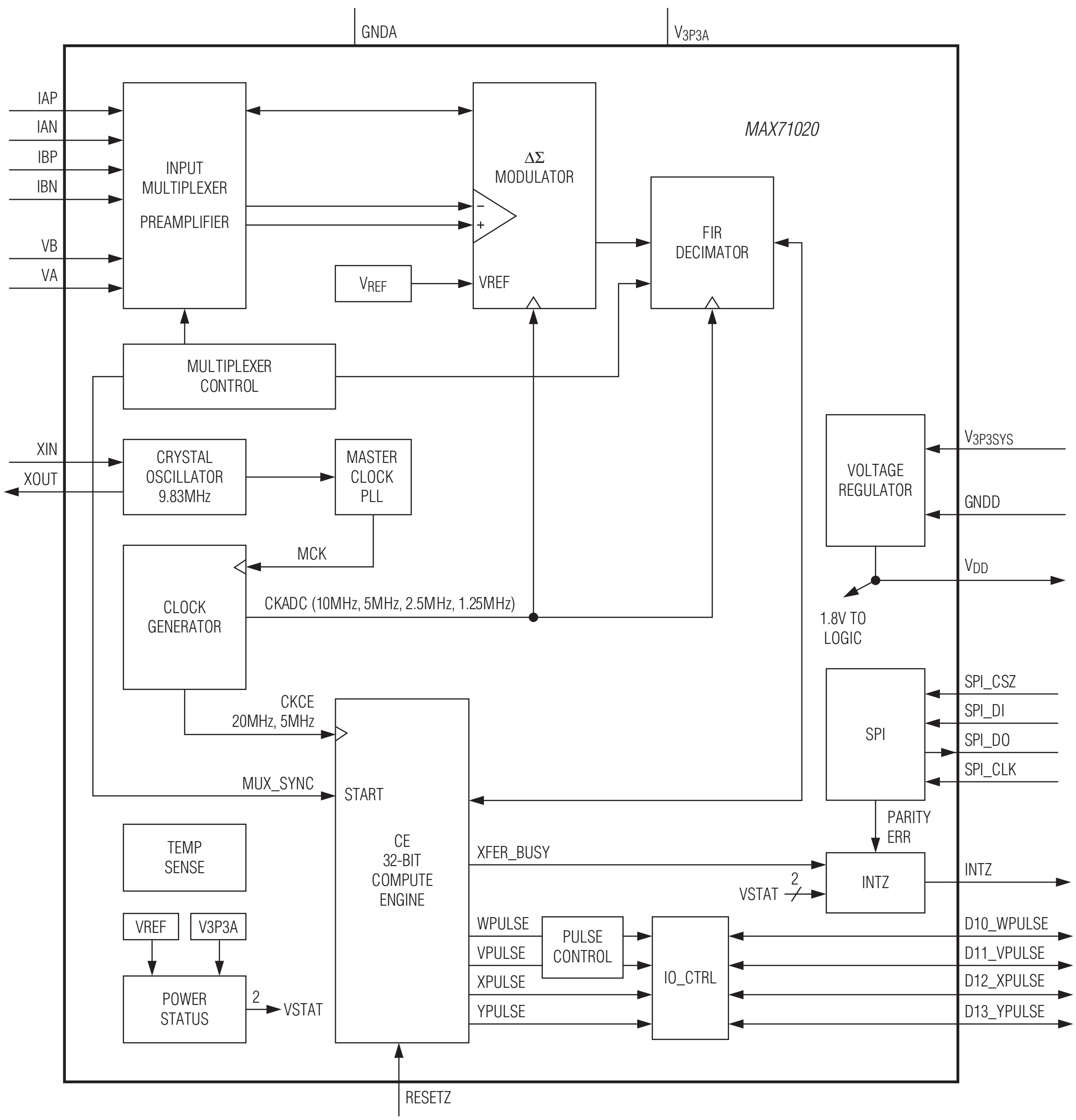


Figure 1. I/O Equivalent Circuits

Functional Block Diagram



Hardware Description

Hardware Overview

The MAX71020 energy meter analog front-end (AFE) integrates all primary functional blocks required to implement a solid-state residential electricity meter. Included on the chip are:

- An analog front-end (AFE) featuring a 22-bit second-order sigma-delta ADC
- An independent 32-bit digital computation engine (CE) to implement DSP functions
- A precision voltage reference (VREF)
- A temperature sensor for digital temperature compensation
- Four I/O pins
- A zero-crossing interrupt
- Resistive shunt and current transformers are supported
- A SPI slave for connection to a host microcontroller

In a typical application, the 32-bit compute engine (CE) of the MAX71020 sequentially processes the samples from the voltage inputs on analog input pinsand performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the host microcontroller.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement, e.g., to meet the requirements of ANSI and IEC standards.

Temperature-dependent external components such as crystal oscillator, resistive shunts, current transformers (CTs) and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

Communications with the host is conducted over a SPI interface. The communications protocol between the host and the MAX71020 provides a redundant information transfer ensuring the correctness of commands transferred from the host to the AFE, and of data transferred from the AFE to the host.

In addition, the MAX71020 has one pin dedicated as an interrupt output to the host. In this way, the MAX71020 notifies the host of asynchronous events.

Analog Section

Signal Input Pins

The MAX71020 has four analog inputs: two single-ended inputs for voltage measurement, and two differential inputs for current measurement.

IAP, IAN, IBP, and IBN pins are current sensor inputs. The differential inputs feature preamplifiers with a selectable gain of 1 or 9, and are intended for direct connection to a shunt resistor sensor or a current transformer (CT).

The voltage inputs in the MAX71020 are single-ended, and are intended for sensing the line voltage. These single-ended inputs are referenced to the GNDA pin.

All analog signal input pins measure voltage. In the case of shunt current sensors, currents are sensed as a voltage drop in the shunt resistor sensor. In the case of Current Transformers (CT), the current is measured as a voltage across a burden resistor that is connected to the secondary winding of the CT. Meanwhile, line voltages are sensed through resistive voltage-dividers. Voltage inputs are single-ended and their common return is the GNDA pin.

Some versions of the device implement a preamplifier with a fixed gain of 9 to enhance performance when using sensors with a low-amplitude output (for example, current shunts). When using a device with the preamplifier enabled, you must ensure that the input amplitude is no greater than 27.78mV peak.

Input Multiplexer

The input multiplexer sequentially applies the input signals from the analog input pins to the input of the ADC. One complete sampling sequence is called a multiplexer frame.

The IBP-IBN differential input may be used to sense the neutral current, and VB may be optionally used to sense a second voltage channel.This configuration implies that the multiplexer applies a total of four inputs to the ADC. For this configuration, the multiplexer sequence is as shown in Figure 1. In this configuration IAP-IAN, IBP-IBN, VA and VB are sampled. The physical current sensor for the neutral current measurement and the voltage sensor for VB may be omitted if not required.

For a standard single-phase application with tamper sensor in the neutral path, two current inputs are configured for differential mode, using the pin pairs IAP-IAN and IBP-IBN. In the MAX71020, the system uses two locally connected current sensors via IAP-IAN and IBP-IBN and configured as differential inputs. The VA pin is typically connected to the phase voltage via resistor-dividers.

The MAX71020 adds the ability to sample a second phase voltage (applied at the VB pin), which makes it suitable for meters with two voltage and two current sensors, such as meters implementing Equation 2 for dual-phase operation (P = VA x IA + VB x IB).

Table 1 summarizes the AFE input configuration.

Delay Compensation

When measuring the energy of a phase (i.e., Wh and VARh) in a service, the voltage and current for that phase must be sampled at the same instant. Otherwise, the phase difference, ϕ, introduces errors.

$$\phi = \frac{t_{delay}}{T} \times 360^\circ = t_{delay} \times f \times 360^\circ$$

where f is the frequency of the input signal, T = 1/f and t_{DELAY} is the sampling delay between current and voltage.

Table 1. ADC Input Configuration

PIN	COMMENT
IAP	The ADC results are stored in register IA.
IAN	
IBP	The ADC results are stored in register IB.
IBN	
VA	The ADC result is stored in register VA.
VB	The ADC result is stored in register VB.

Traditionally, sampling is accomplished by using two ADCs per phase (one for voltage and the other one for current) controlled to sample simultaneously. Maxim's Teridian™ Single-Converter Technology®, however, exploits the 32-bit signal processing capability of its CE to implement "constant delay" allpass filters. The allpass filter corrects for the conversion time difference between the voltage and the corresponding current samples that are obtained with a single multiplexed ADC.

The constant delay allpass filter provides a broadband delay 360° - θ, which is precisely matched to the difference in sample time between the voltage and the current of a given phase. This digital filter does not affect the amplitude of the signal, but provides a precisely controlled phase response.

The ADC multiplexer samples the current first, immediately followed by sampling of the corresponding phase voltage, thus the voltage is delayed by a phase angle ϕ relative to the current. The delay compensation implemented in the CE aligns the voltage samples with their corresponding current samples by first delaying the current samples by one full sample interval (i.e., 360°), then routing the voltage samples through the allpass filter, thus delaying the voltage samples by 360° - θ, resulting in the residual phase error between the current and its corresponding voltage of $\theta - \phi$. The residual phase error is negligible, and is typically less than ±0.0015° at 100Hz, thus it does not contribute to errors in the energy measurements.

ADC Preamplifier

The ADC preamplifier is a low-noise differential amplifier with a fixed gain of 9 available on the IAP and IAN current-sensor input pins. It is provided only in versions of the MAX71020 AFE configured for use with current shunts.

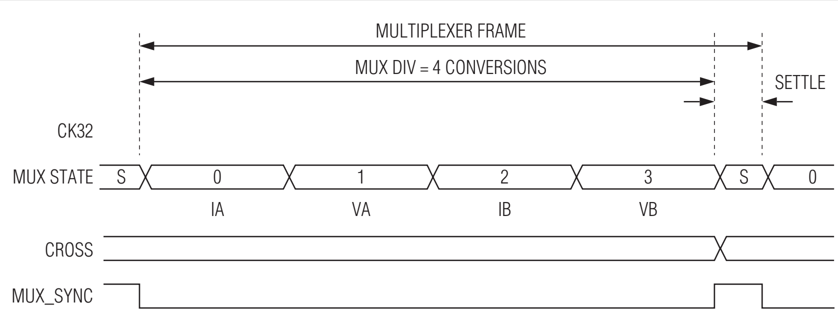


Figure 2. States in a Multiplexer Frame

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Analog-to-Digital Converter (ADC)

A single second-order delta-sigma ADC digitizes the voltage and current inputs to the device. The resolution of the ADC is dependent on several factors.

Initiation of each ADC conversion is automatically controlled by logic internal to the MAX71020. At the end of each ADC conversion, the FIR filter output data is stored into the register determined by the multiplexer selection. FIR data is stored LSB justified, but shifted left 9 bits.

FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the register determined by the multiplexer selection.

Voltage References

A bandgap circuit provides the reference voltage to the ADC. Since the VREF bandgap amplifier is chopper stabilized, the DC offset voltage, which is the most significant long-term drift mechanism in the voltage references (VREF), is automatically removed by the chopper circuit.

Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time)
- Frequency-insensitive delay cancellation on all four channels (to compensate for the delay between samples caused by the multiplexing scheme)
- 90° phase shifter (for VAR calculations)
- Pulse generation
- Monitoring of the input signal frequency (for frequency and phase information)
- Monitoring of the input signal amplitude (for sag detection)
- Scaling of the processed samples based on calibration coefficients
- Scaling of samples based on temperature compensation information
- Gain and phase compensation

Meter Equations

The MAX71020 provides hardware assistance to the CE in order to support various meter equations. This assistance is controlled through register EQU[2:0] (equation assist). The Compute Engine (CE) firmware implements the equations listed in Table 2. EQU[2:0] specifies the equation to be used based on the meter configuration and on the number of phases used for metering.

Pulse Generators

The MAX71020 provides up to four pulse generators, VPULSE, WPULSE, XPULSE, and YPULSE, as well as hardware support for the VPULSE and WPULSE pulse generators. The pulse generators are used to output CE status indicators and energy usage.

The polarity of the pulses may be inverted with control bit PLS_INV. When this bit is set, the pulses are active-high, rather than the more usual active-low. PLS_INV inverts all four pulse outputs.

The function of each pulse generator is determined by the CE code. The MAX71020 provides a mains zero-crossing indication on XPULSE and voltage sag detection on YPULSE.

A common use of the zero-crossing pulses is to generate interrupt in order to drive RTC software in places where the mains frequency is sufficiently accurate to do so and also to adjust for crystal aging. A common use for the SAG pulse is to generate an interrupt that alerts the host processor when mains power is about to fail, so that the host processor can store accumulated energy and other data to EEPROM before the supply voltage actually drops.

Table 2. Inputs Selected in Multiplexer Cycles

EQU	DESCRIPTION	Wh and VARh FORMULA	
		ELEMENT 0	ELEMENT 1
0	1 element, 2W, 1φ with neutral current sense	VA · IA	VA · IB
1	1 element, 3-W, 1φ	VA(IA-IB)/2	VA · IB/2
2	2 element, 3-W	VA · IA	VB · IB

Table 3. Pulse Output Function Assignments

OUTPUT	FUNCTION
XPULSE	Pulse output on each zero crossing on voltage input
YPULSE	Pulse output when voltage sag detected
VPULSE	Pulse output when programmed VARh consumption has occurred
WPULSE	Pulse output when programmed Wh consumption has occurred

XPULSE and YPULSE

Pulses generated by the CE may be exported to the XPULSE and YPULSE pulse output pins. Pins D2 and D3 are used for these pulses, respectively. The XPULSE and YPULSE outputs can be updated once on each pass of the CE code. See the *CE Interface Description* section for details.

VPULSE and WPULSE

By default, WPULSE and VPULSE are negative pulses (i.e., low level pulses, designed to sink current through an LED). PLS_MAXWIDTH[7:0] determines the maximum negative pulse width T_{MAX} in units of CK_FIR clock cycles based on the pulse interval T_I according to the formula:

$$T_{MAX} = (2 \times \text{PLS\_MAXWIDTH}[7:0] + 1) \times T_I$$

T_I is based on an internal value that determines the pulse interval and the ADC clock, both of which are determined by the particular characteristics of the compute engine. In the MAX71020, the default value for T_I is 65.772µs, but this value changes in customized versions of this part.

If PLS_MAXWIDTH = 255 no pulse-width checking is performed, and the pulses default to 50% duty cycle. T_{MAX} is typically programmed to 10ms (T_{MAX} = 76), which works well with most calibration systems.

The polarity of the pulses may be inverted with the control bit PLS_INV. When PLS_INV is set, the pulses are active-high. The default value for PLS_INV is zero, which selects active-low pulses.

The WPULSE and VPULSE pulse generator outputs are available on pins D0/WPULSE and D1/VPULSE, respectively.

Temperature Sensor

The MAX71020 includes an on-chip temperature sensor for determining the temperature of its bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system for the compensation of current, voltage, and energy measurement. See the *Metrology Temperature Compensation* section.

The temperature sensor is awakened on command from the host microcontroller by setting the TEMP_START control bit. The host microcontroller must wait for the TEMP_START bit to clear before reading STEMP[15:0] and before setting the TEMP_START bit once again.

The result of the temperature measurement can be read from the STEMP[15:0] register. The 16-bit value is in two's complement form and ranges from -1024 to +1023 (decimal). The sensed temperature can be computed from the 16-bit STEMP[15:0] reading using the following formula:

$$\text{Temp (°C)} = 0.325 \times \text{STEMP} + 22$$

An additional register, VSENSE[7:0], senses the level of supply voltage. Table 4 shows the registers used for temperature measurement.

Digital I/O

On reset or power-up, all DIO pins are configured as high-impedance. DIO pins can be configured independently by the host microcontroller by manipulating the D0, D1, D2, and D3 bit fields.

Table 4. Temperature Measurement Registers

NAME	RST	WK	DIR	DESCRIPTION
TBYTE_BUSY	0	0	R	Indicates that hardware is still writing the result. Additional writes to this byte are locked out while it is one. Write duration could be as long as 6ms.

Table 4. Temperature Measurement Registers (continued)

NAME	RST	WK	DIR	DESCRIPTION	
TEMP_PER[1:0]	0	—	R/W	Sets the period between temperature measurements	
				TEMP_PER	**TIME**
				0	Manual updates (see TEMP_START description)
				1	Every accumulation cycle
				2	Continuous
TEMP_START	0	—	R/W	TEMP_PER[1:0] must be zero in order for TEMP_START to function. If TEMP_PER[1:0] = 0, then setting TEMP_START starts a temperature measurement. Hardware clears TEMP_START when the temperature measurement is complete. The host microcontroller must wait for TEMP_START to clear before reading STEMP[10:0] and before setting TEMP_START again.	
STEMP[15:0]	—	—	R	The result of the temperature measurement	
VSENSE[7:0]	—	—	R	The result of voltage sense reading: V_{3P3SYS} = VSENSE[7:0]/42.7	

SPI Slave Port

The slave SPI port communicates directly with the host microcontroller and allows it to read and write the device control registers. The interface to the slave port consists of the SPI_CSZ, SPI_CLK, SPI_DI, and SPI_DO pins.

SPI Transactions

SPI transactions are configured to provide immunity to electrical noise through redundancy in the command segment and error checking in the data field. The MAX71020 SPI transaction is exactly 64 bits; transactions of any other length are rejected. Each SPI transaction has the following fields:

- A 24-bit setting packet, consisting of
  - 11-bit address, MSB first
  - 1-bit direction (1 means read)
  - 11-bit inverted address, MSB first
  - 1-bit inverted direction
- An 8-bit status, consisting of the following bits concerning the last transaction, starting from bit 7:
  - 11-bit address, MSB
  - Parity of the status byte (0 or 1 could be correct)
  - FIFO overflow status bit (1 means error)
  - FIFO underrun status bit (1 means error)
  - Read or write data parity (0 or 1 could be correct) (never both read and write; address is not included in the parity)
  - Address or direction mismatch error bit (1 means error)
  - Result of the SPI_CSZ glitch detector (1 means error)
  - A bit indicating whether or not the bit count was exactly 64 (1 means error).
  - Out of bounds address, most likely due to SPI safe bit or the memory manager (1 means error).
- A 32-bit packet of data, MSB first
  - If extra clocks are provided at the end during a read, all zero is output and the status will continue to be updated, signaling an error.
  - If extra clocks are provided at the end during a write, the write will be aborted and the status will be updated to signal an error.
- None of the fields above are optional.
- If an error is detected during the address or direction phase, no action will be taken.
- SPI_DO is high-Z while SPI_CSZ is high.
- SPI safe mode will be supported, and SPI will not be locked out of this bit during SPI safe.

A typical SPI transaction is as follows. While SPI_CSZ is high, the port is held in an initialized/reset state. During this state, SPI_DO is held in high-Z state and all transitions on SPI_CLK and SPI_DI are ignored. When SPI_CSZ falls, the port will begin the transaction on the first rising edge of SPI_CLK. As shown in Table 5, a transaction consists of a 24-bit setting field, an 8-bit

Table 5. SPI Transaction (64 Bits)

24-BIT SETTING FIELD				8-BIT STATUS								32-BIT DATA
Address	Dir	Inv Address	Inv Dir	Status from Previous Transaction: status[7:0]								Data
addr[10:0]	RD	addr_b[10:0]	RD_b	Status Parity	FIFO OverRun	FIFO UnderRun	Data Parity	Setting Mismatch	CSB Glitch	Bad CK Cnt	Bad Address	data[31:0]

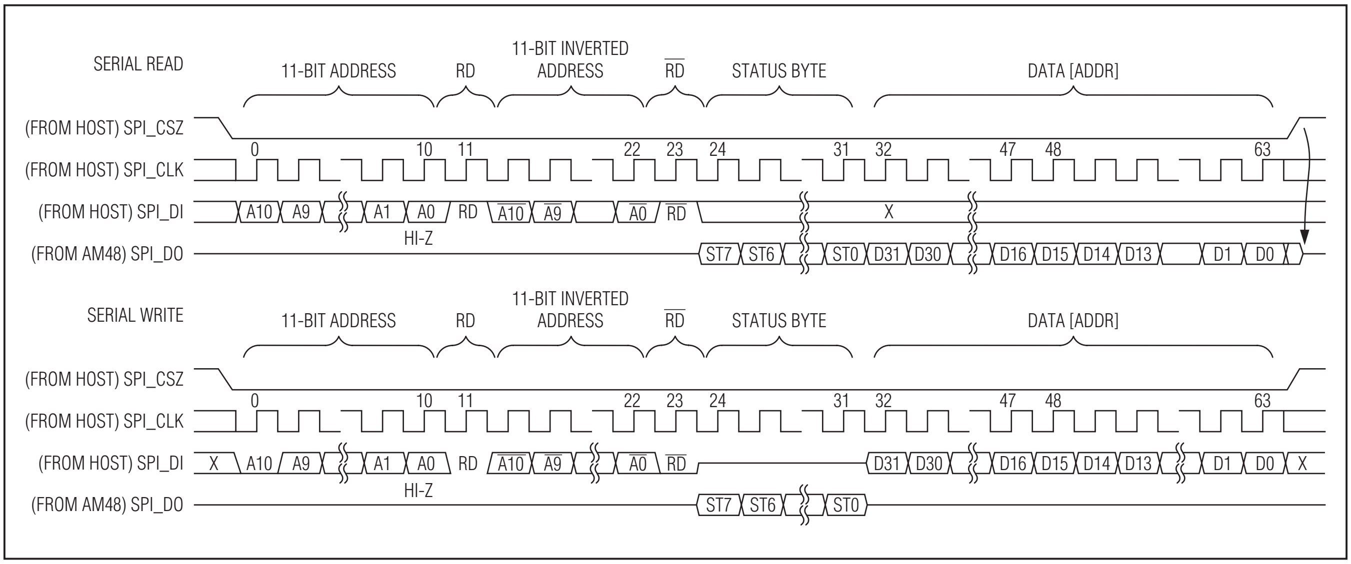

Figure 3. SPI Slave Port—Typical READ and WRITE operations

status, and a 32-bit data word. The transaction ends when SPI_CSZ is raised.

Note that the status byte indicates the status of the previous SPI transaction except for the status byte parity.

SPI Safe Mode

Sometimes it is desirable to prevent the SPI interface from writing to arbitrary registers and possibly disturbing the CE operation. For this reason, the SPI_SAFE mode is created. In this mode, all SPI writes are disabled except to the word containing the SPI_SAFE bit. This affords the host one more layer of protection from inadvertent writes.

Functional Description

Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t)I(t)dt$$

Assuming phase angles are constant, the following formulae apply:

P = Real Energy [Wh] = V x A x cos ϕ x t

Q = Reactive Energy [VARh] = V x A x sin ϕ x t

S = Apparent Energy [VAh] = $\sqrt{P^2 + Q^2}$

For a practical meter, not only voltage and current amplitudes, but also phase angles and harmonic content may constantly change. Thus, simple RMS measurements are inherently inaccurate. A modern solid-state electricity meter IC such as the MAX71020 functions by emulating the integral operation above, i.e., it processes current and voltage samples through an ADC at a constant frequency. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied with the time period of sampling yield an accurate quantity for the momentary energy. Summing the instantaneous energy quantities over time provides very accurate results for accumulated energy.

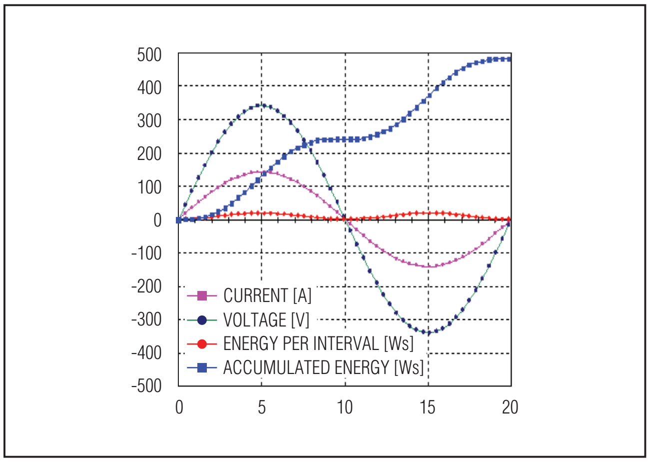

Figure 4. Voltage, Current, Momentary and Accumulated Energy

Figure 4 shows the shapes of V(t), I(t), the instantaneous power and the accumulated energy resulting from 50 samples of the voltage and current signals over a period of 20ms. The application of 240VAC and 100A results in an accumulation of 480Ws (= 0.133Wh) over the 20ms period, as indicated by the accumulated power curve. The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

Fault and Reset Behavior

Events at Power-Down

Power fault detection is performed by internal comparators that monitor the voltage at the V_{3P3A} pin and also monitor the internally generated V_{DD} pin voltage (1.8VDC). V_{3P3SYS} and V_{3P3A} must be connected together at the PCB level, so that the comparators, which are internally connected only to the V_{3P3A}, are able to simultaneously monitor the common V_{3P3SYS} and V_{3P3A} voltage. The following discussion assumes that V_{3P3A} and V_{3P3SYS} are connected together at the PCB level.

During a power failure, as V_{3P3A} falls, two thresholds are detected. The first threshold, at 3.0V, warns the host microcontroller that the analog modules are no longer accurate. The second threshold, at 2.8V, warns the host microcontroller that a serious reduction in supply voltage has occurred. OTP reads may be affected.

Reset Sequence

When the MAX71020 receives a reset signal, either from the RESETZ pin or from the SPI, it asynchronously halts what it was doing. It then clears RAM and initializes configuration bits. An errant RESET can occur during an ESD event. If this happens, the host must be notified. This is accomplished by holding the INTZ output low until the host clears it.

Applications Information

Sensor Connection

Figure 5 to Figure 8 show voltage-sensing resistive dividers, current-sensing current transformers (CTs) and current-sensing resistive shunts and how they are connected to the voltage and current inputs of the MAX71020. All input signals to the MAX71020 sensor inputs are voltage signals providing a scaled representation of either a sensed voltage or current.

CAUTION The analog input pins of the MAX71020 are designed for sensors with low source impedance. RC filters with resistance values higher than those implemented in the demo boards must not be used. Refer to the demo board schematics for complete sensor input circuits and corresponding component values.

Table 6. VSTAT[1:0]

VSTAT[1:0]	DESCRIPTION
00	System Power-OK. V_{V3P3A} > 3.0V. Analog modules are functional and accurate.
01	System Power is low. 2.8V < V_{V3P3A} < 3.0V. Analog modules not accurate.
11	System power below 2.8V. Ability to monitor power is about to fail.

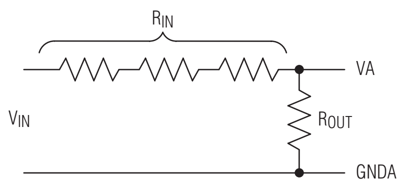

Figure 5. Resistive Voltage-Divider (Voltage Sensing)

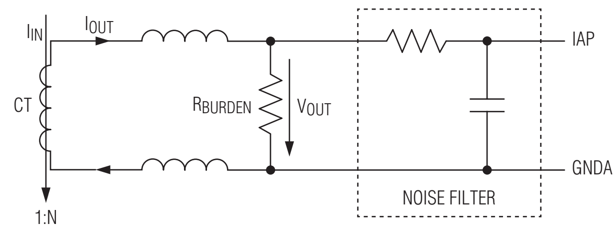

Figure 6. CT With Single-Ended Input Connection (Current Sensing)

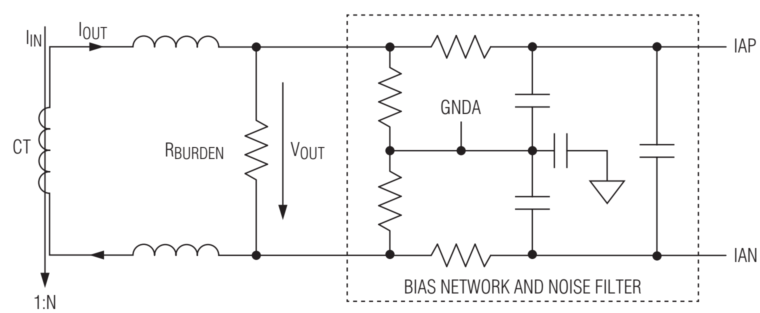

Figure 7. CT With Differential Input Connection (Current Sensing)

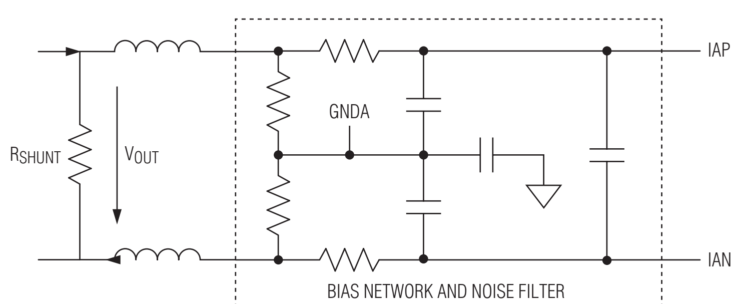

Figure 8. Differential Resistive Shunt Connections (Current Sensing)

Connecting the MAX71020

Figure 9 shows a typical MAX71020 configuration. The IAP-IAN current channel may be directly connected to either a shunt resistor or a CT, while the IBP-IBN channel is connected to a CT and is therefore isolated. This configuration implements a single-phase measurement with tamper-detection using one current sensor to measure the neutral current. This configuration can also be used to create a split phase meter (e.g., ANSI Form 2S).

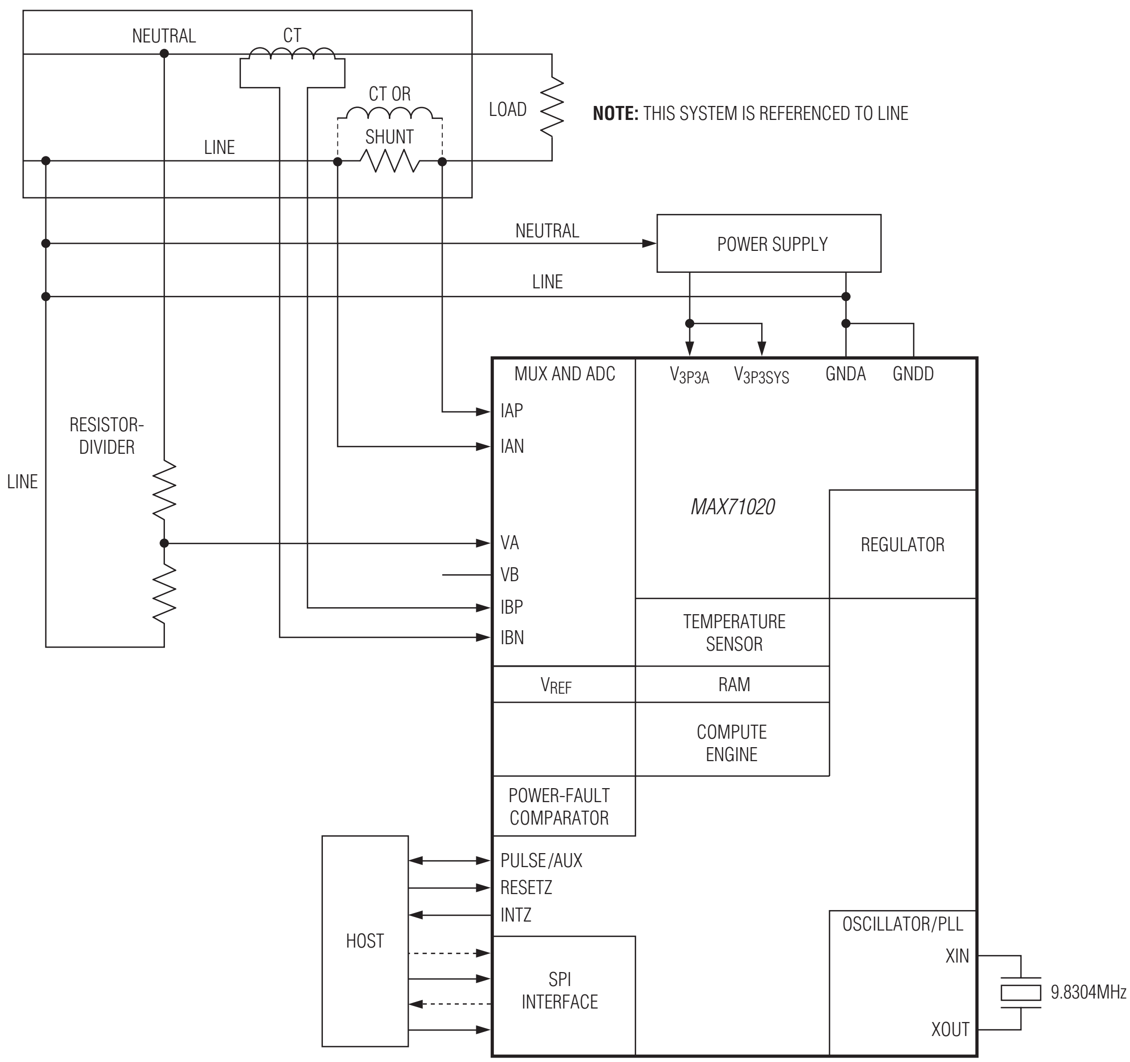

Figure 9. Connecting the MAX71020

Metrology Temperature Compensation

Voltage Reference Precision

Since the VREF bandgap amplifier is chopper-stabilized the DC offset voltage, which is the most significant long-term drift mechanism in the voltage references, is automatically removed by the chopper circuit. Maxim trims the VREF voltage reference during the device manufacturing process to ensure the best possible accuracy.

The reference voltage (VREF) is trimmed to a target value of 1.205V nominal. During this trimming process, the TRIMT[7:0] value is stored in nonvolatile fuses. TRIMT[7:0] is trimmed to a value that results in minimum VREF variation with temperature.

The TRIMT[7:0] value can be read by the host microcontroller during initialization to calculate parabolic temperature compensation coefficients suitable for each individual device. The resulting temperature coefficient for VREF is ±40ppm/°C.

Considering the factory calibration temperature of VREF to be +22°C and the industrial temperature range (-40°C to +85°C), the VREF error at temperature extremes can be calculated as:

$$(85°C - 22°C) \times 40ppm/°C = +2520ppm = +1.252\%$$

and

$$(-40°C - 22°C) \times 40ppm/°C = +2480ppm = -0.248\%$$

The above calculation implies that both the voltage and the current measurements are individually subject to a theoretical maximum error of approximately ±0.25%. When the voltage sample and current sample are multiplied together to obtain the energy per sample, the voltage error and current error combine resulting in approximately ±0.5% maximum energy measurement error. However, this theoretical ±0.5% error considers only the voltage reference (VREF) as an error source. In practice, other error sources exist in the system. The principal remaining error sources are the current sensors (shunts or CTs) and their corresponding signal conditioning circuits, and the resistor voltage-divider used to measure the voltage. The 0.5% grade devices should be used in class 1% designs, allowing sufficient margin for the other error sources in the system.

Crystal Oscillator

The oscillator drives an AT cut microprocessor crystal at a frequency of 9.8304MHz. Board layouts with minimum capacitance from XIN to XOUT require less current. Good layouts have XIN and XOUT shielded from each other and from digital signals.

CAUTION Since the oscillator is self-biasing, an external resistor must not be connected across the crystal.

Meter Calibration

Once the MAX71020 energy meter device has been installed in a meter system, it must be calibrated. A complete calibration includes the following:

- Establishment of the reference temperature (e.g., typically 22°C).
- Calibration of the metrology section, i.e., calibration for tolerances of the current sensors, voltage-dividers, and signal conditioning components as well as of the internal reference voltage (VREF) at the reference temperature (e.g., typically 22°C).

The metrology section can be calibrated using the gain and phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by the current sensors or by the effects of reactive power supplies.

The MAX71020 supports common industry-standard calibration techniques, such as single-point (energy-only) and multipoint (energy, V_{RMS}, I_{RMS}).

Register Map

Table 7. Register Map

<table>
<tr><th>NAME</th><th>BYTE ADDRESS</th><th>R/W</th><th>DEFAULT VALUE</th><th>DESCRIPTION</th></tr>
<tr><td>CAL_IA</td><td>0x010</td><td>R/W</td><td>0x0000 4000</td><td>Calibration constant for current channel A. Unity gain = 0x0000 4000.</td></tr>
<tr><td>CAL_VA</td><td>0x011</td><td>R/W</td><td>0x0000 4000</td><td>Calibration constant for current channel B. Unity gain = 0x0000 4000.</td></tr>
<tr><td>ADJ_A</td><td>0x012</td><td>R/W</td><td>0x0000 0000</td><td>—</td></tr>
<tr><td>CAL_IB</td><td>0x013</td><td>R/W</td><td>0x0000 4000</td><td>Calibration constant for voltage channel A. Unity gain = 0x0000 4000.</td></tr>
<tr><td>CAL_VB</td><td>0x014</td><td>R/W</td><td>0x0000 4000</td><td>Calibration constant for voltage channel B. Unity gain = 0x0000 4000.</td></tr>
<tr><td>ADJ_B</td><td>0x015</td><td>R/W</td><td>0x0000 0000</td><td>—</td></tr>
<tr><td>CECONFIG</td><td>0x020</td><td>R/W</td><td>0x0030 DB00</td><td>Configures internal CE operation
<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>PULSE_SLOW</td><td>Reduces pulse output rate by a factor of 64. Must not be used with PULSE_FAST.</td></tr>
<tr><td>1</td><td>PULSE_FAST</td><td>Increases pulse output rate by a factor of 16. Must not be used with PULSE_SLOW.</td></tr>
<tr><td>5:2</td><td>Reserved</td><td>—</td></tr>
<tr><td>6</td><td>FREQSEL</td><td>Select phase for frequency measurement: 0 = A, 1 = B</td></tr>
<tr><td>7</td><td>Reserved</td><td>—</td></tr>
<tr><td>19:8</td><td>SAG_CNT</td><td>Number of consecutive voltage samples below SAG_THR before a sag event is declared</td></tr>
<tr><td>20</td><td>SAG_INT</td><td>Enable sag detect output on YPULSE</td></tr>
<tr><td>21</td><td>EDGE_INT</td><td>Enable zero-crossing output on XPULSE</td></tr>
<tr><td>31:22</td><td>Reserved</td><td>—</td></tr>
</table></td></tr>
<tr><td>WRATE</td><td>0x021</td><td>R/W</td><td>0x0000 0223</td><td>Sets meter constant for pulse outputs. See the Pulse Generation section.</td></tr>
<tr><td>KVAR</td><td>0x022</td><td>R/W</td><td>0x0000 192C</td><td>Scale factor for VAR measurements</td></tr>
<tr><td>SAG_THR</td><td>0x024</td><td>R/W</td><td>0x016C AF60</td><td>Voltage threshold for sag warnings. See the CE Status and Control section.</td></tr>
<tr><td>QUANT_VA</td><td>0x025</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for voltage phase A</td></tr>
<tr><td>QUANT_IA</td><td>0x026</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for current phase A</td></tr>
<tr><td>QUANT_A</td><td>0x027</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for real power phase A</td></tr>
<tr><td>QUANT_VARA</td><td>0x028</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for reactive power phase A</td></tr>
<tr><td>QUANT_VB</td><td>0x029</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for voltage phase B</td></tr>
<tr><td>QUANT_IB</td><td>0x02A</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for current phase B</td></tr>
<tr><td>QUANT_B</td><td>0x02B</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for real power phase B</td></tr>
<tr><td>QUANT_VARB</td><td>0x02C</td><td>R/W</td><td>0x0000 0000</td><td>Truncation/noise compensation for reactive power phase B</td></tr>
<tr><td>GAIN_ADJ0</td><td>0x040</td><td>R/W</td><td>0x0000 4000</td><td>Scale value for voltage inputs VA and VB. Default value of 16,384 is unity gain.</td></tr>
</table>

Table 7. Register Map (continued)

<table>
<tr><th>NAME</th><th>BYTE ADDRESS</th><th>R/W</th><th>DEFAULT VALUE</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>GAIN_ADJ1</td><td>0x041</td><td>R/W</td><td>0x0000 4000</td><td colspan="3">Scale value for current input IA. Default value of 16,384 is unity gain.</td></tr>
<tr><td>GAIN_ADJ2</td><td>0x042</td><td>R/W</td><td>0x0000 4000</td><td colspan="3">Scale value for current input IB. Default value of 16,384 is unity gain.</td></tr>
<tr><td>WPULSE_CTR</td><td>0x045</td><td>R</td><td>—</td><td colspan="3">Pulse generator counter (real power)</td></tr>
<tr><td>WPULSE_FRAC</td><td>0x046</td><td>R</td><td>—</td><td colspan="3">Pulse generator numerator (real power)</td></tr>
<tr><td>WSUM_ACCUM</td><td>0x047</td><td>R</td><td>—</td><td colspan="3">Pulse generator rollover accumulator (real power)</td></tr>
<tr><td>VPULSE_CTR</td><td>0x049</td><td>R</td><td>—</td><td colspan="3">Pulse generator counter (reactive power)</td></tr>
<tr><td>VPULSE_FRAC</td><td>0x04A</td><td>R</td><td>—</td><td colspan="3">Pulse generator numerator (reactive power)</td></tr>
<tr><td>VSUM_ACCUM</td><td>0x04B</td><td>R</td><td>—</td><td colspan="3">Pulse generator rollover accumulator (reactive power)</td></tr>
<tr><td rowspan="7">CESTATUS</td><td rowspan="7">0x080</td><td rowspan="7">R</td><td rowspan="7">—</td><td colspan="3">Status of the Compute Engine</td></tr>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>SAG_A</td><td>Sag status, voltage phase A</td></tr>
<tr><td>1</td><td>SAG_B</td><td>Sag status, voltage phase B</td></tr>
<tr><td>2</td><td>Reserved</td><td>—</td></tr>
<tr><td>3</td><td>F0</td><td>Square wave at exact line frequency</td></tr>
<tr><td>31:4</td><td>Reserved</td><td>—</td></tr>
<tr><td>FREQ_X</td><td>0x082</td><td>R</td><td>—</td><td colspan="3">Fundamental line frequency in units of (2520.6 x 2^{-32})Hz</td></tr>
<tr><td>MAINEDGE_X</td><td>0x083</td><td>R</td><td>—</td><td colspan="3">Number of zero crossings of either direction during previous accumulation period</td></tr>
<tr><td>WSUM_X</td><td>0x084</td><td>R</td><td>—</td><td colspan="3">Signed sum of real energy from both wattmeter elements</td></tr>
<tr><td>W0SUM_X</td><td>0x085</td><td>R</td><td>—</td><td colspan="3">Real energy from wattmeter element 0</td></tr>
<tr><td>W1SUM_X</td><td>0x086</td><td>R</td><td>—</td><td colspan="3">Real energy from wattmeter element 1</td></tr>
<tr><td>VARSUM_X</td><td>0x088</td><td>R</td><td>—</td><td colspan="3">Signed sum of reactive energy from both wattmeter elements</td></tr>
<tr><td>VAR0SUM_X</td><td>0x089</td><td>R</td><td>—</td><td colspan="3">Reactive energy from wattmeter element 0</td></tr>
<tr><td>VAR1SUM_X</td><td>0x08A</td><td>R</td><td>—</td><td colspan="3">Reactive energy from wattmeter element 1</td></tr>
<tr><td>I0SQSUM_X</td><td>0x08C</td><td>R</td><td>—</td><td colspan="3">Sum of squared samples from current sensor 0</td></tr>
<tr><td>I1SQSUM_X</td><td>0x08D</td><td>R</td><td>—</td><td colspan="3">Sum of squared samples from current sensor 1</td></tr>
<tr><td>V0SQSUM_X</td><td>0x090</td><td>R</td><td>—</td><td colspan="3">Sum of squared samples from voltage sensor 0</td></tr>
<tr><td>V1SQSUM_X</td><td>0x091</td><td>R</td><td>—</td><td colspan="3">Sum of squared samples from voltage sensor 1</td></tr>
<tr><td>IA</td><td>0x100</td><td>R</td><td>—</td><td colspan="3">Most recent result of ADC conversion for current channel A</td></tr>
<tr><td>IB</td><td>0x102</td><td>R</td><td>—</td><td colspan="3">Most recent result of ADC conversion for current channel B</td></tr>
<tr><td>VB</td><td>0x109</td><td>R</td><td>—</td><td colspan="3">Most recent result of ADC conversion for voltage channel B</td></tr>
<tr><td>VA</td><td>0x10A</td><td>R</td><td>—</td><td colspan="3">Most recent result of ADC conversion for voltage channel A</td></tr>
</table>

Table 7. Register Map (continued)

<table>
<tr><th>NAME</th><th>BYTE ADDRESS</th><th>R/W</th><th>DEFAULT VALUE</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="5">DEVICEID</td><td rowspan="5">0x301</td><td rowspan="5">R</td><td rowspan="5">0x0000 1100</td><td colspan="3">Contains identifying information for the device</td></tr>
<tr><td>BIT</td><td>NAME</td><td>DESCRIPTION</td></tr>
<tr><td>7:0</td><td>Reserved</td><td>—</td></tr>
<tr><td>15:8</td><td>VERSION</td><td>Version index. Currently, on 0x11 is defined as die type AM48A0A.</td></tr>
<tr><td>31:16</td><td>CHIP_ID</td><td>Family tag and feature tag of the device, currently 0x0000</td></tr>
<tr><td>STEMP</td><td>0x30A</td><td>R</td><td>—</td><td colspan="3">Result of the temperature measurement. Only bits 26:16 are significant; all other bits return zero.</td></tr>
<tr><td>BSENSE</td><td>0x30B</td><td>R</td><td>—</td><td colspan="3">Result of the device V_{DD} measurement. Only bits 23:16 are significant; all other bits return zero.</td></tr>
</table>

Table 7. Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE	BIT	NAME	DESCRIPTION
IOCFG	0x30C	R/W	0x0000 0F00	Contains the characteristics of the four digital I/O pins		
				0	DI0	Reflects logic state on DIO0
				1	DI1	Reflects logic state on DIO1
				2	DI2	Reflects logic state on DIO2
				3	DI3	Reflects logic state on DIO3
				7:4	Reserved	—
				8	D_OD0	Configures DIO0 as open drain if configured as output
				9	D_OD1	Configures DIO1 as open drain if configured as output
				10	D_OD2	Configures DIO2 as open drain if configured as output
				11	D_OD3	Configures DIO3 as open drain if configured as output
				15:12	Reserved	—
				17:16	DO	Configures DIO0. 00: Hi-Z 01: WPULSE 10: Logic 1 11: Logic 0
				19:18	D1	Configures DIO1. 00: Hi-Z 01: VPULSE 10: Logic 1 11: Logic 0
				21:20	D2	Configures DIO2. 00: Hi-Z 01: XPULSE 10: XFER_BUSY 11: Logic 0
				23:22	D3	Configures DIO3. 00: Hi-Z 01: YPULSE 10: CE_BUSY 11: Logic
				31:24	Reserved	—
METER_CFG	0x30D	R/W	0xFF00 0080	Configures hardware aspects of the AFE		
				14:0	Reserved	—
				15	PLS_INV	Force meter pulses to be positive-going rather than negative-going
				23:16	Reserved	—
				31:24	PLS_MAXWID	Determines the maximum width of a meter pulse

Table 7. Register Map (continued)

<table>
<tr><th>NAME</th><th>BYTE ADDRESS</th><th>R/W</th><th>DEFAULT VALUE</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="13">INT_CFG</td><td rowspan="13">0x30F</td><td rowspan="13">R/W</td><td rowspan="13">0x0000 8000</td><td colspan="3">Interrupt configuration register: configure the behavior of the INTZ pin</td></tr>
<tr><td>BIT</td><td>NAME</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>IE_WPULSE</td><td>Enables an interrupt to occur on the leading edge of WPULSE</td></tr>
<tr><td>1</td><td>IE_VPULSE</td><td>Enables an interrupt to occur on the leading edge of VPULSE</td></tr>
<tr><td>2</td><td>IE_YPULSE</td><td>Enables an interrupt to occur on the leading edge of YPULSE</td></tr>
<tr><td>3</td><td>IE_XPULSE</td><td>Enables an interrupt to occur on the leading edge of XPULSE</td></tr>
<tr><td>4</td><td>IE_XDATA</td><td>Enables an interrupt to occur at the conclusion of the accumulation interval, indicating that fresh data is available</td></tr>
<tr><td>5</td><td>IE_CEBUSY</td><td>Enables an interrupt to occur when the CE cycles is complete</td></tr>
<tr><td>6</td><td>Reserved</td><td>—</td></tr>
<tr><td>7</td><td>IE_VSTAT</td><td>Enables an interrupt to occur when the VSYS status changes</td></tr>
<tr><td>11:8</td><td>INT_POL</td><td>Interrupt polarity for the PULSE edges. The default polarity is falling edge.
INT_POL[3]=1: Interrupt on rising edge of YPULSE
INT_POL[2]=1: Interrupt on rising edge of XPULSE
INT_POL[1]=1: Interrupt on rising edge of VPULSE
INT_POL[0]=1: Interrupt on rising edge of WPULSE</td></tr>
<tr><td>14:12</td><td>Reserved</td><td>—</td></tr>
<tr><td>15</td><td>D_ODINTZ</td><td>Enable open-drain on the INTZ output. By default, the pin is configured as a CMOS totem-pole output.</td></tr>
<tr><td></td><td></td><td></td><td></td><td>31:16</td><td>Reserved</td><td>—</td></tr>
</table>

Table 7. Register Map (continued)

NAME	BYTE ADDRESS	R/W	DEFAULT VALUE	BYTE ADDRESS		
M_STAT	0x310	R	0x0100 0100	Reflects the status of several asynchronous events in the AFE		
				BIT	**NAME**	**DESCRIPTION**
				0	F_WPULSE	Set on start of WPULSE
				1	F_VPULSE	Set on start of VPULSE
				2	F_XPULSE	Set on start of YPULSE
				3	F_YPULSE	Set on start of XPULSE
				4	F_XDATA	Set when data available
				5	F_CEBUSY	Set at end of CE code pass
				6	Reserved	—
				7	F_VSTAT	Set when VSYS status changes
				8	F_RESET	Set following AFE reset
				15:9	Reserved	—
				16	F_WPULSE	Copy of bit 0
				17	F_VPULSE	Copy of bit 1
				18	F_XPULSE	Copy of bit 2
				19	F_YPULSE	Copy of bit 3
				20	F_XDATA	Copy of bit 4
				21	F_CEBUSY	Copy of bit 5
				23:22	Reserved	—
				24	F_RESET	Copy of bit 8
				31:25	Reserved	—

Table 7. Register Map (continued)

<table>
<tr><th rowspan="2">NAME</th><th rowspan="2">BYTE ADDRESS</th><th rowspan="2">R/W</th><th rowspan="2">DEFAULT VALUE</th><th colspan="3">DESCRIPTION</th></tr>
<tr></tr>
<tr><td rowspan="21">M_STAT_B</td><td rowspan="21">0x311</td><td rowspan="21">R</td><td rowspan="21">0x0100 0100</td><td colspan="3">Backup of M_STAT – updated when M_STAT is read</td></tr>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>FB_WPULSE</td><td>Set on start of WPULSE</td></tr>
<tr><td>1</td><td>FB_VPULSE</td><td>Set on start of VPULSE</td></tr>
<tr><td>2</td><td>FB_XPULSE</td><td>Set on start of YPULSE</td></tr>
<tr><td>3</td><td>FB_YPULSE</td><td>Set on start of XPULSE</td></tr>
<tr><td>4</td><td>FB_XDATA</td><td>Set when data available</td></tr>
<tr><td>5</td><td>FB_CEBUSY</td><td>Set at end of CE code pass</td></tr>
<tr><td>7:6</td><td>Reserved</td><td>—</td></tr>
<tr><td>8</td><td>FB_RESET</td><td>Set following AFE reset</td></tr>
<tr><td>15:9</td><td>Reserved</td><td>—</td></tr>
<tr><td>16</td><td>FB_WPULSE</td><td>Copy of bit 0</td></tr>
<tr><td>17</td><td>FB_VPULSE</td><td>Copy of bit 1</td></tr>
<tr><td>18</td><td>FB_XPULSE</td><td>Copy of bit 2</td></tr>
<tr><td>19</td><td>FB_YPULSE</td><td>Copy of bit 3</td></tr>
<tr><td>20</td><td>FB_XDATA</td><td>Copy of bit 4</td></tr>
<tr><td>21</td><td>FB_CEBUSY</td><td>Copy of bit 5</td></tr>
<tr><td>23:22</td><td>Reserved</td><td>—</td></tr>
<tr><td>24</td><td>FB_RESET</td><td>Copy of bit 8</td></tr>
<tr><td>31:25</td><td>Reserved</td><td>—</td></tr>
<tr></tr>
<tr><td>VSTAT</td><td>0x312</td><td>R</td><td>—</td><td colspan="3">AFE Supply Voltage Status. Bits 1:0 reflect system power status:
00: System power-OK: $V_{V3P3A} > 3.0V$
01: System power-low: $2.8V < V_{V3P3A} < 3.0V$
11: System power-fail: $V_{V3P3A} < 2.8V$</td></tr>
<tr><td>RESET</td><td>0x322</td><td>WO</td><td>—</td><td colspan="3">Write 0x8100 0000 to this register to reset the AFE.</td></tr>
</table>

Table 7. Register Map (continued)

<table>
<tr><th>NAME</th><th>BYTE ADDRESS</th><th>R/W</th><th>DEFAULT VALUE</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="6">TEMP_CNF</td><td rowspan="6">0x323</td><td rowspan="6">R/W</td><td rowspan="6">0x0000 0000</td><td colspan="3">Configures aspects of the temperature measurement subsystem</td></tr>
<tr><td>BIT</td><td>NAME</td><td>DESCRIPTION</td></tr>
<tr><td>1:0</td><td>Reserved</td><td>—</td></tr>
<tr><td>3:2</td><td>TEMP_PER</td><td>Sets the period between temperature measurements.
01: Measure every accumulation cycle
10: Continuous measurement
Other values disable automatic updates.</td></tr>
<tr><td>4</td><td>TEMP_SYS</td><td>When set, VSYS is measured at every temperature measurement cycle</td></tr>
<tr><td>31:5</td><td>Reserved</td><td>—</td></tr>
<tr><td>TEMP_START</td><td>0x324</td><td>R/W</td><td>0x0000 0000</td><td colspan="3">Write 0x8000 0000 to start a temperature conversion cycle. When conversion is complete, the AFE will clear bit 31 and return the register to zero.</td></tr>
<tr><td>SPI_SAFE</td><td>0x325</td><td>R/W</td><td>0x0000 0000</td><td colspan="3">Write 0x8000 0000 to this word to lock the SPI port. When the SPI port is locked, no read or write operations are possible except to the SPI_SAFE register. Clearing this register to zero disables the SPI lock and restores normal operation.</td></tr>
<tr><td rowspan="5">METER_EN</td><td rowspan="5">0x326</td><td rowspan="5">R/W</td><td rowspan="5">0x0000 0000</td><td colspan="3">Enables aspects of the AFE</td></tr>
<tr><td>BIT</td><td>NAME</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>ADC_E</td><td>Enable ADC and VREF buffer. Must be set by host following initialization.</td></tr>
<tr><td>1</td><td>CE_E</td><td>Enable CE. Must be set by host following initialization.</td></tr>
<tr><td>31:2</td><td>Reserved</td><td>—</td></tr>
</table>

CE Interface Description

The CE reads the ADC and stores its results in the 1KB block at 0x000. Since all CE operations are 32 bits wide, the CE data memory occupies the first 256 32-bit locations, from 0x000 to 0x0FF.

Note: The CE interface described in the data sheet is a description of a CE codebase that was available at the time of the writing. Changes may have occurred in the codebase in the interim, and may not be reflected in this document. Please contact your representative or Maxim technical support for the latest information.

CE Data Format

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement format (-1 = 0xFFFFFFFF). Calibration parameters are copied to CE data memory by the host microcontroller before enabling the CE. Internal variables are used in internal CE calculations. Input variables allow the MPU to control the behavior of the CE code.

Constants

Constants used in the CE Data Memory tables are:

- f_0 is the fundamental frequency of the mains phases.
- I_{MAX} is the external RMS current corresponding to the maximum allowed voltage on the current inputs. For the IB input, this is 250mV peak (176.8mV$_{RMS}$). In the MAX71020, IA normally has a preamplifier enabled on the IA inputs, so I_{MAX} needs to be adjusted to 27.78mV peak (19.64mV$_{RMS}$) for the IAP-IAN inputs. For a 250μΩ shunt resistor, I_{MAX} becomes 78A (19.64mV$_{RMS}$/250μΩ = 78.57A) for IA, and 707A (176.8mV$_{RMS}$/250μΩ = 707.2A$_{RMS}$) for IB.
- V_{MAX} is the external RMS voltage corresponding to 250mV peak at the VA and VB inputs.
- N_{ACC}, the accumulation count for energy measurements (typically 2520).
- The duration of the accumulation interval for energy measurements is N_{ACC}/F_S = 2520/2,520.6 ≈ 1s.
- X is a gain constant of the pulse generators. Its value is determined by PULSE_FAST and PULSE_SLOW(see Table 13).
- Voltage LSB (for sag threshold) = V_{MAX} x 7.879810 - 9V.

The system constants I_{MAX} and V_{MAX} are used by the host processor to convert internal digital quantities (as used by the CE) to external, real-world metering quantities. Their values are determined by the scaling of the voltage and current sensors used in an actual meter. The LSB values used in this document relate digital quantities at the CE or MPU interface to external meter input quantities. For example, if a SAG threshold of 80V$_{RMS}$ is desired at the meter input, the digital value that should be programmed into SAG_THR (register 0x024) would be 80V$_{RMS}$ x SQRT(2)/SAG_THR$_{LSB}$, where SAG_THR$_{LSB}$ is the LSB value in the description of SAG_THR (see Table 14).

Environment

Before starting the CE (that is, before setting the CE_E bit) the host processor must establish the equation to be applied in EQU[2:0]. By default, default settings are assumed to be V_{MAX} = 600V, I_{MAX} = 707A, and kH = 1.

CE Calculations

In Table 8, The MPU selects the desired equation by writing the EQU[2:0] (register 0x30D[14:12]).

Table 8. CE EQU Equations and Element Input Mapping

EQU	WATT AND VAR FORMULA (WSUM/VARSUM)	INPUTS USED FOR ENERGY/CURRENT CALCULATION			
		W0SUM/ VAR0SUM	W1SUM/ VAR1SUM	I0SQ SUM	I1SQ SUM
0	VA IA – 1 element, 2W 1ϕ	VA x IA	VA x IB	IA	—
1	VA x (IA-IB)/2 – 1 element, 3W 1ϕ	VA x (IA-IB)/2	—	IA-IB	IB
2	VA x IA + VB x IB– 2 element, 3W 1ϕ	VA x IA	VB x IB	IA	IB

Table 9. CE Raw Data Access Locations

PIN	REGISTER
IA	0x100
VA	0x101
IB	0x102
VB	0x103

Table 10. CESTATUSRegister

CE ADDRESS	NAME	DESCRIPTION
0x80	CESTATUS	See the description of CESTATUS bits in Table 11

Table 11. CESTATUS (Register 0x080) Bit Definitions

CESTATUS BIT	NAME	DESCRIPTION
31:4	Not Used	These unused bits are always zero
3	F0	F0 is a square wave at the line frequency
2	Not Used	This unused bit is always zero
1	SAG_B	Set when VB remains below SAG_THR for SAG_CNT samples. Automatically clears when VB rises above SAG_THR.
0	SAG_A	Set when VA remains below SAG_THR for SAG_CNT samples. Automatically clears when VA rises above SAG_THR.

CE Front-End Data (Raw Data)

Access to the raw data provided by the AFE is possible by reading registers 0x100–0x003 as shown in Table 9.

CE Status and Control

The CE Status Word, CESTATUS, is useful for generating early warnings to the host processor (Table 10). It contains sag warnings for phase A and B, as well as F0, the derived clock operating at the line frequency. The host microcontroller can read the CE status word at every CE_BUSY interrupt.

CESTATUS provides information about the status of voltage and input AC signal frequency, which are useful for generating an early power-fail warning to initiate necessary data storage. CESTATUS represents the status flags for the preceding CE code pass (CE_BUSY interrupt). The significance of the bits in CESTATUS is shown in Table 11.

Table 12. CECONFIG Register

CE ADDRESS	NAME	DATA	DESCRIPTION
0x20	CECONFIG	0x0030DB00	See the description of the CECONFIG bits in Table 13

Table 13. CECONFIG Bit Definitions

<table>
<tr><th>CECONFIG BIT</th><th>NAME</th><th>DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>21</td><td>EDGE_INT</td><td>1</td><td colspan="3">When 1, XPULSE produces a pulse for each zero-crossing of the mains phase selected by FREQSEL[1:0] that can be used to interrupt the host microcontroller</td></tr>
<tr><td>20</td><td>SAG_INT</td><td>1</td><td colspan="3">When 1, activates YPULSE output when a sag condition is detected</td></tr>
<tr><td>19:8</td><td>SAG_CNT</td><td>252
(0xFC)</td><td colspan="3">The number of consecutive voltage samples below SAG_THR (register 0x24) before a sag alarm is declared. The default value is equivalent to 100ms</td></tr>
<tr><td rowspan="5">7:6</td><td rowspan="5">FREQSEL[1:0]</td><td rowspan="5">0</td><td colspan="3">FREQSEL[1:0] selects the phase to be used for the frequency monitor, sag detection, and for the zero-crossing counter (MAINEDGE_X, register 0x083)</td></tr>
<tr><th colspan="2">FREQ SEL[1:0]</th><th>PHASE SELECTED</th></tr>
<tr><td>0</td><td>0</td><td>A</td></tr>
<tr><td>0</td><td>1</td><td>B</td></tr>
<tr><td>1</td><td>X</td><td>Not allowed</td></tr>
<tr><td>5:2</td><td>Reserved</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">PULSE_FAST</td><td rowspan="2">0</td><td colspan="3">When PULSE_FAST = 1, the pulse generator input is increased 16x. When PULSE_SLOW = 1, the pulse generator input is reduced by a factor of 64. These two parameters control the pulse gain factor X (see table below). Allowed values are either 1 or 0. Default is 0 for both (X = 6).</td></tr>
<tr><th>PULSE_FAST</th><th>PULSE_SLOW</th><th>X</th></tr>
<tr><td rowspan="4">0</td><td rowspan="4">PULSE_SLOW</td><td rowspan="4">0</td><td>0</td><td>0</td><td>$1.5 \times 2^2 = 6$</td></tr>
<tr><td>1</td><td>0</td><td>$1.5 \times 2^6 = 96$</td></tr>
<tr><td>0</td><td>1</td><td>$1.5 \times 2^{-4} = 0.09375$</td></tr>
<tr><td>1</td><td>1</td><td>Do not use</td></tr>
</table>

The CE is initialized by the host microcontroller using CECONFIG (Table 12). This register contains the SAG_CNT, FREQSEL[1:0], PULSE_SLOW, and PULSE_FAST fields. The CECONFIG bit definitions are given in Table 13.

The FREQSEL[1:0] field in CECONFIG (register 0x020[7:6]) selects the phase that is utilized to generate a sag interrupt. Thus, a SAG_INT event occurs when the selected phase has satisfied the sag event criteria as set by SAG_THR (register 0x24) and the SAG_CNT field in CECONFIG (register 0x020[19:8]). When the SAG_INT bit (register 0x020[20]) is set to 1, a sag event generates a transition on the YPULSE output. In a two-phase system, and after a sag interrupt, the host microcontroller should change the FREQSEL[1:0] setting to select the other phase, if it is powered. Even though a sag interrupt is only generated on the selected phase, both phases are simultaneously checked for sag. The presence of power on a given phase can be sensed by directly checking the SAG_A and SAG_B bits in CESTATUS (register 0x080[1:0]).

The CE controls the pulse rate based on WSUM_X (register 0x084) and VARSUM_X (register 0x088).

CE Transfer Variables

When the host microcontroller receives the XFER_BUSY interrupt, it knows that fresh data is available in the transfer variables. CE transfer variables are modified during the CE code pass that ends with an XFER_BUSY interrupt. They remain constant throughout each accumulation interval. In this data sheet, the names of CE transfer variables always end with "_X". The transfer variables can be categorized as:

- Fundamental energy measurement variables
- Instantaneous (RMS) values
- Other measurement parameters

Fundamental Energy Measurement Variables

Table 15 describes each transfer variable for fundamental energy measurement. All variables are signed 32-bit integers. Accumulated variables such as WSUM are internally scaled so that internal values are no more than 50% of the full-scale range when the integration time is one second. Additionally, the hardware does not permit output values to fold back upon overflow.

WSUM_X (register 0x084) and VARSUM_X (register 0x088) are the signed sum of Phase-A and Phase-B Wh or VARh values according to the metering equation specified in EQU[2:0](register 0x30D[14:12]). WxSUM_X (x = 0 or 1, registers 0x085 and 0x086) is the watt-hour value accumulated for phase x in the last accumulation interval and can be computed based on the specified LSB value.

Table 14. Sag Threshold and Gain Adjust Control

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x24	SAG_THR	2.39×10^7	The voltage threshold for sag warnings. The default value is equivalent to 113Vpk or $80V_{RMS}$ if $V_{MAX} = 600V_{RMS}$. $SAG\_THR = \frac{V_{RMS} \times \sqrt{2}}{V_{MAX} \times 7.8798 \times 10^{-9}}$
0x40	GAIN_ADJ0	16384	This register scales the voltage measurement channels VA and VB. The default value of 16384 is equivalent to unity gain (1.000).
0x41	GAIN_ADJ1	16384	This register scales the IA current channel for Phase A. The default value of 16384 is equivalent to unity gain (1.000).
0x42	GAIN_ADJ2	16384	This register scales the IB current channel for Phase B. The default value of 16384 is equivalent to unity gain (1.000).

Table 15. CE Transfer Variables

CE ADDRESS	NAME	DESCRIPTION	CONFIGURATION
0x84	WSUM_X	The signed sum: W0SUM_X + W1SUM_X. Not used for EQU[2:0] = 0 (register 0x30D[14:12]) and EQU[2:0] = 1.	Figure 8
0x85	W0SUM_X	The sum of Wh samples from each wattmeter element. $LSB_W = 6.08040 \times 10^{-13} \times V_{MAX} \times I_{MAX}$ Wh	
0x86	W1SUM_X		
0x88	VARSUM_X	The signed sum: VAR0SUM_X + VAR1SUM_X. Not used for EQU[2:0] = 0 and EQU[2:0] = 1.	
0x89	VAR0SUM_X	The sum of VARh samples from each wattmeter element. $LSB_W = 6.08040 \times 10^{-13} \times V_{MAX} \times I_{MAX}$ VARh	
0x8A	VAR1SUM_X		

Instantaneous Energy Measurement Variables

I_SQSUM_X and V_SQSUM (see Table 16) are the sum of the squared current and voltage samples acquired during the last accumulation interval.

The RMS values can be computed by the host microcontroller from the squared current and voltage samples as follows:

$$I_{RMS} = \sqrt{\frac{I\_SQSUM \times LSB_I \times 9{,}074{,}160}{N_{ACC}}}$$

Other

$$V_{RMS} = \sqrt{\frac{V\_SQSUM \times LSB_V \times 9{,}074{,}160}{N_{ACC}}}$$

Other transfer variables include those available for frequency and those reflecting the count of the zero-crossings of the mains voltage. These transfer variables are listed in Table 17.

MAINEDGE_X (register 0x083) reflects the number of half-cycles accounted for in the last accumulated interval for the AC signal of the phase specified in the FREQSEL[1:0] field in CECONFIG (register 0x020[7:6]). MAINEDGE_X is useful for implementing a real-time clock based on the input AC signal.

Pulse Generation

Table 18 describes the CE pulse generation parameters.

The combination of the CECONFIG:PULSE_SLOW and CECONFIG:PULSE_FAST bits (register 0x020[0:1]) controls the speed of the pulse rate. The default zero values of these configuration bits maintain the original pulse rate given by the Kh equation, follows in this section.

WRATE (register 0x021) controls the number of pulses that are generated per measured Wh and VARh. The lower WRATE is, the slower the pulse rate for the measured energy quantity; or conversely, the greater the measured energy per pulse. By default, the pulse generators take their input from the W0SUM_X (register 0x085) and VAR0SUM_X (register 0x089) result registers.

The meter constant Kh is derived from WRATE and represents the amount of energy measured for each pulse. If Kh = 1Wh/pulse and 120V and 30A is applied in-phase to the meter, the meter will produce one pulse per second (120V and 30A results in a load of 3600W, or put another way, energy consumption of one watt-hour per second). If the load is 240V at 150A, ten pulses per second are generated. To compute the WRATE value, see Table 18.

The maximum pulse rate is 7.56kHz.

Table 16. CE Energy Measurement Variables

CE ADDRESS	NAME	DESCRIPTION	CONFIGURATION
0x8C	I0SQSUM_X	The sum of squared current samples from each element. $LSB_I = 6.08040 \times 10^{-13}\ IMAX^2\ A^2h$ When EQU = 1, I0SQSUM_X is based on IA and IB.	Figure 8
0x8D	I1SQSUM_X		
0x90	V0SQSUM_X	The sum of squared voltage samples from each element. $LSB_V = 6.08040 \times 10^{-13}\ VMAX^2\ V^2h$	
0x91†	V1SQSUM_X		

Table 17. Other Transfer Variables

CE ADDRESS	NAME	DESCRIPTION
0x82	FREQ_X	Fundamental frequency: $LSB \equiv \frac{2520.6Hz}{2^{32}} \approx 0.509 \times 10^{-6}$
0x83	MAINEDGE_X	The number of edge crossings of the selected voltage in the previous accumulation interval. Edge crossings are either direction and are debounced.

See the VPULSE and WPULSE section for details on how to adjust the timing of the output pulses. The maximum time jitter is 1/6 of the multiplexer cycle period (nominally 67µs) and is independent of the number of pulses measured. Thus, if the pulse generator is monitored for one second, the peak jitter is 67ppm. After 10s, the peak jitter is 6.7ppm. The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it simply outputs at its maximum rate without exhibiting any rollover characteristics. The actual pulse rate, using WSUM as an example, is:

$$RATE = \frac{WRATE \times WSUM \times f_S \times X}{2^{46}} Hz$$

where f_S = sampling frequency (2520.6Hz), X = pulse speed factor derived from the CE variables PULSE_SLOW (register 0x020[0]) and PULSE_FAST (register 0x020[1]).

Other CE Parameters

Table 19 shows the CE parameters used for suppression of noise due to scaling and truncation effects.

CE Calibration Parameters

Table 20 lists the parameters that are typically entered to effect calibration of meter accuracy.

CE Flow Diagrams

Figure 10 to Figure 12 show the data flow through the CE in simplified form. Functions not shown include delay compensation, sag detection, scaling, and the processing of meter equations.

Table 18. CE Pulse Generation Parameters

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x21	WRATE	547	$Kh = \frac{K \times V_{MAX} \times I_{MAX}}{SUM\_SAMPS \times WRATE \times X}$ Wh/pulse where: K = 42.7868 See Table 13 for the definition of X. The default value yields 1.0 Wh/pulse for V_{MAX} = 600V and I_{MAX} = 208A. The maximum value for WRATE is 32,768 (2^{15}).
0x22	KVAR	6444	Scale factor for VAR measurement
0x45	WPULSE_CTR	0	WPULSE counter
0x46	WPULSE_FRAC	0	Unsigned numerator, containing a fraction of a pulse. The value in this register always counts up towards the next pulse.
0x47	WSUM_ACCUM	0	Rollover accumulator for WPULSE
0x4A	VPULSE_CTR	0	VPULSE counter
0x4A	VPULSE_FRAC	0	Unsigned numerator, containing a fraction of a pulse. The value in this register always counts up towards the next pulse.
0x4B	VSUM_ACCUM	0	Rollover accumulator for VPULSE

Table 19. CE Parameters for Noise Suppression and Code Version

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x25	QUANT_VA	0	Compensation factors for truncation and noise in voltage, current, real energy, and reactive energy for phase A.
0x26	QUANT_IA	0	
0x27	QUANT_A	0	
0x28	QUANT_VARA	0	
0x29	QUANT_VB	0	Compensation factors for truncation and noise in voltage, current, real energy, and reactive energy for phase B.
0x2A	QUANT_IB	0	
0x2B	QUANT_B	0	
0x2C	QUANT_VARB	0	

$$\mathrm{QUANT\_Ix\_LSB} = 3.28866 \times 10^{-13} \times I_{MAX}{}^{2} (\mathrm{Amps}^{2})$$

$$\mathrm{QUANT\_Wx\_LSB} = 6.73518 \times 10^{-10} \times V_{MAX} \times I_{MAX} (\mathrm{Watts})$$

$$\mathrm{QUANT\_VARx\_LSB} = 6.73518 \times 10^{-10} \times V_{MAX} \times I_{MAX} (\mathrm{Vars})$$

Table 20. CE Calibration Parameters

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x10	CAL_IA	16384	These constants control the gain of their respective channels. The nominal value for each parameter is 2^{14} = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be increased by 1%.
0x11	CAL_VA	16384	
0x13	CAL_IB	16384	
0x14	CAL_VB	16384	
0x12	PHADJ_A	0	These constants control the CT phase compensation. Compensation does not occur when PHADJ_X = 0. As PHADJ_X is increased, more compensation (lag) is introduced. The range is ±215 – 1. If it is desired to delay the current by the angle Φ, the equations are: $\mathrm{PHADJ\_X} = 2^{20} \frac{0.02229 \times \mathrm{TAN}\Phi}{0.1487 - 0.0131 \times \mathrm{TAN}\Phi}$ at 60Hz $\mathrm{PHADJ\_X} = 2^{20} \frac{0.0155 \times \mathrm{TAN}\Phi}{0.1241 - 0.009695 \times \mathrm{TAN}\Phi}$ at 50Hz
0x15	PHADJ_B	0	

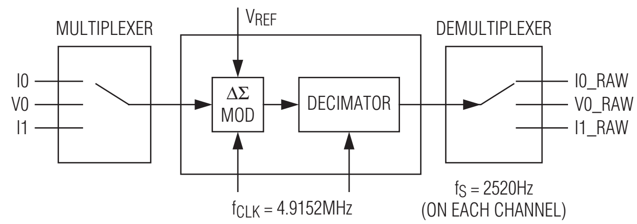

Figure 10. CE Data Flow (Multiplexer and ADC)

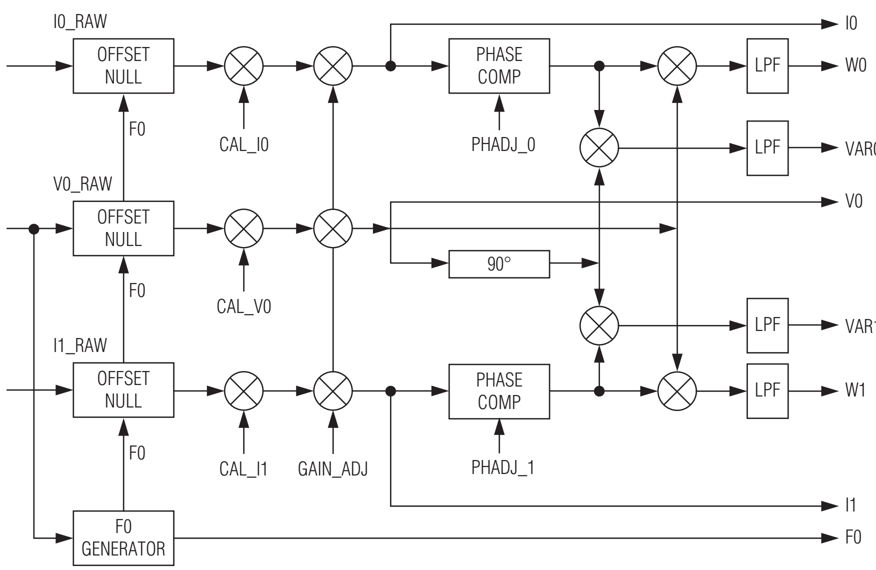

Figure 11. CE Data Flow (Scaling, Gain Control, Intermediate Variables)

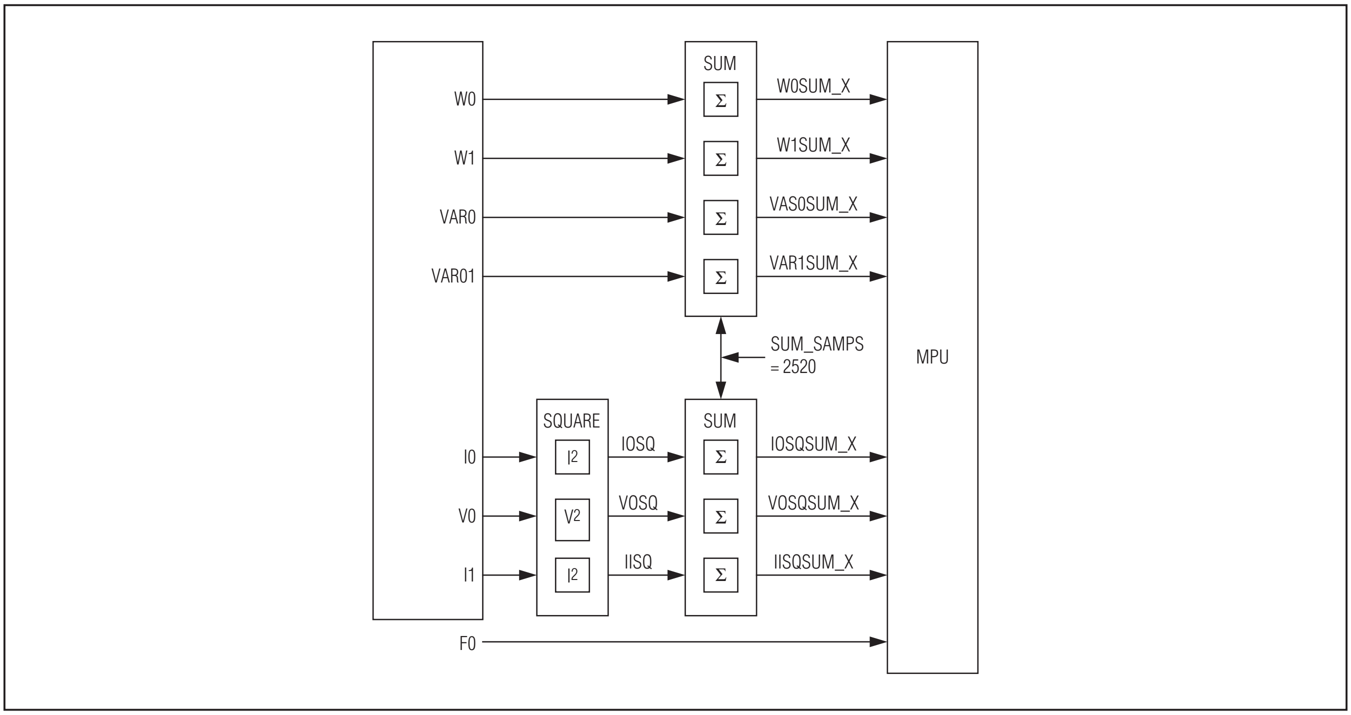

Figure 12. CE Data Flow (Squaring and Summation Stages)

Ordering Information

PART	PIN-PACKAGE	ACCURACY (%)	PACKAGING
MAX71020AEUI+	28 TSSOP	0.5	Bulk
MAX71020AEUI+R	28 TSSOP	0.5	Tape and reel

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)–free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TSSOP	U28+1	**21-0066**	**90-0171**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—