

# ADC1002S020

Single 10 bits ADC, up to 20 MHz

Rev. 03 — 2 July 2012

Product data sheet

## 1. General description

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The ADC1002S020 is a 10-bit high-speed Analog-to-Digital Converter (ADC) for professional video and other applications. It converts with 3.0 V to 5.25 V operation the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 20 MHz. All digital inputs and outputs are CMOS compatible. A standby mode allows a reduction of the device power consumption to 4 mW.

## 2. Features

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- 10-bit resolution
- 3.0 V to 5.25 V operation
- Sampling rate up to 20 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 1.0 MHz; full-scale input at  $f_{\text{clk}} = 20$  MHz)
- In-Range (IR) CMOS output
- CMOS/Transistor-Transistor Logic (TTL) compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 53 mW (typical value)
- Low analog input capacitance, no buffer amplifier required
- Standby mode
- No sample-and-hold circuit required

## 3. Applications

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- Video data digitizing
- Camera
- Camcorder
- Radio communication
- Barcode scanner



## 4. Quick reference data

**Table 1. Quick reference data**

$V_{DDA} = V7$  to  $V9 = 3.3$  V;  $V_{DDD} = V4$  to  $V3 = V18$  to  $V19 = 3.3$  V;  $V_{DDO} = V20$  to  $V21 = 3.3$  V;  $V_{SSA}$ ,  $V_{SSD}$  and  $V_{SSO}$  shorted together;  $V_{i(p-p)} = 1.83$  V;  $C_L = 20$  pF;  $T_{amb} = 0$  °C to  $70$  °C; typical values measured at  $T_{amb} = 25$  °C unless otherwise specified.

| Symbol         | Parameter                  | Conditions  | Min | Typ        | Max       | Unit |
|----------------|----------------------------|---|-----|------------|-----------|------|
| $V_{DDA}$      | analog supply voltage      |   | 3.0 | 3.3        | 5.25      | V    |
| $V_{DDD1}$     | digital supply voltage 1   |   | 3.0 | 3.3        | 5.25      | V    |
| $V_{DDD2}$     | digital supply voltage 2   |   | 3.0 | 3.3        | 5.25      | V    |
| $V_{DDO}$      | output supply voltage      |   | 3.0 | 3.3        | 5.25      | V    |
| $I_{DDA}$      | analog supply current      |   | -   | 7.5        | 10        | mA   |
| $I_{DDD}$      | digital supply current     |   | -   | 7.5        | 10        | mA   |
| $I_{DDO}$      | output supply current      | $f_{clk} = 20$ MHz;<br>ramp input;<br>$C_L = 20$ pF | -   | 1          | 2         | mA   |
| INL            | integral non-linearity     | ramp input; see<br>Figure 6                         | -   | $\pm 1$    | $\pm 2$   | LSB  |
| DNL            | differential non-linearity | ramp input; see<br>Figure 7                         | -   | $\pm 0.25$ | $\pm 0.7$ | LSB  |
| $f_{clk(max)}$ | maximum clock frequency    |   | 20  | -          | -         | MHz  |
| $P_{tot}$      | total power dissipation    | operating;<br>$V_{DDD} = 3.3$ V                     | -   | 53         | 73        | mW   |
|                |                            | standby mode  | -   | 4          | -         | mW   |

## 5. Ordering information

**Table 2. Ordering information**

| Type number   | Package |  | Version  |
|---------------|---------|--|----------|
|               | Name    | Description  |          |
| ADC1002S020HL | LQFP32  | plastic low profile quad flat package; 32 leads; body $5 \times 5 \times 1.4$ mm | SOT401-1 |

## 6. Block diagram

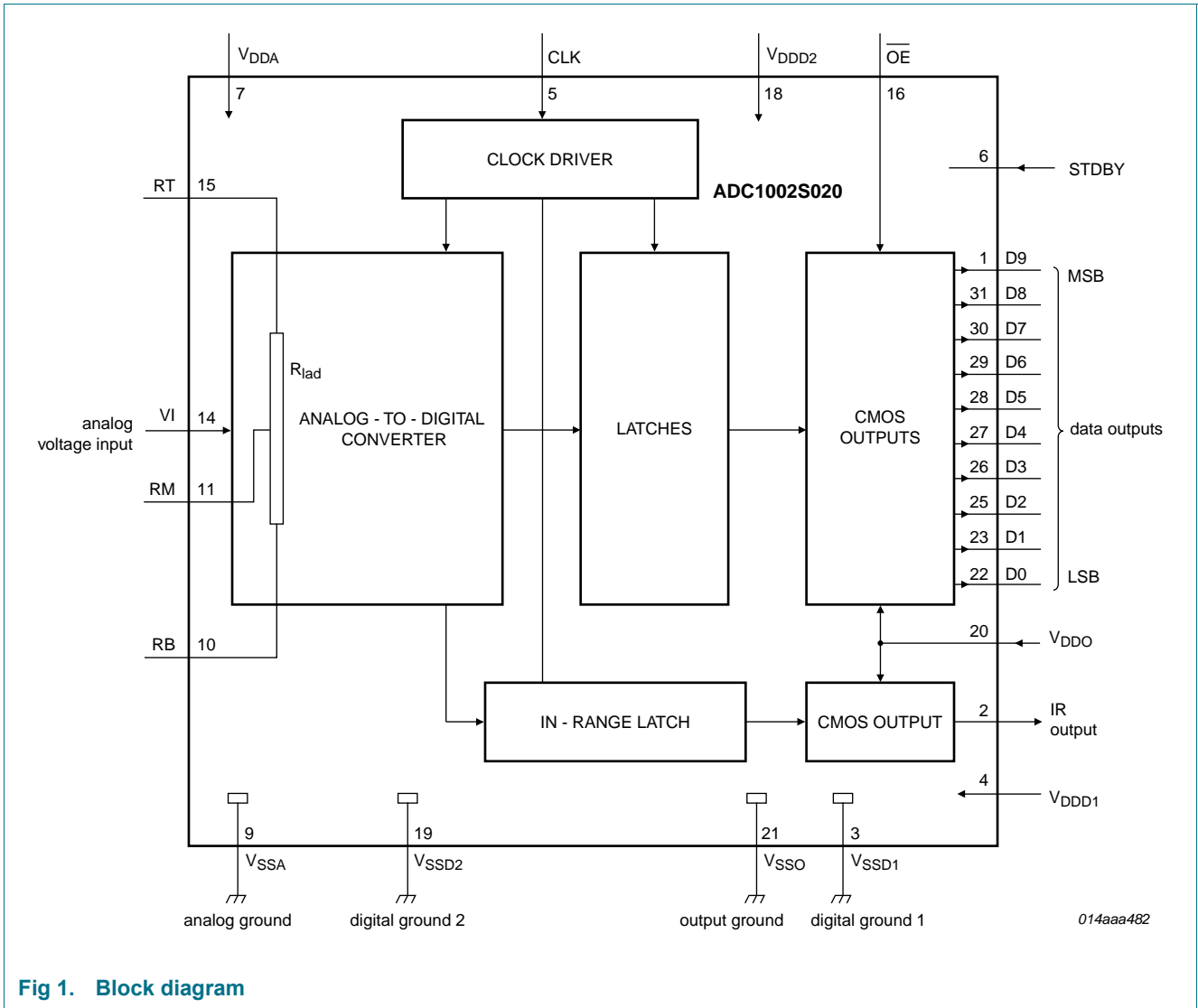
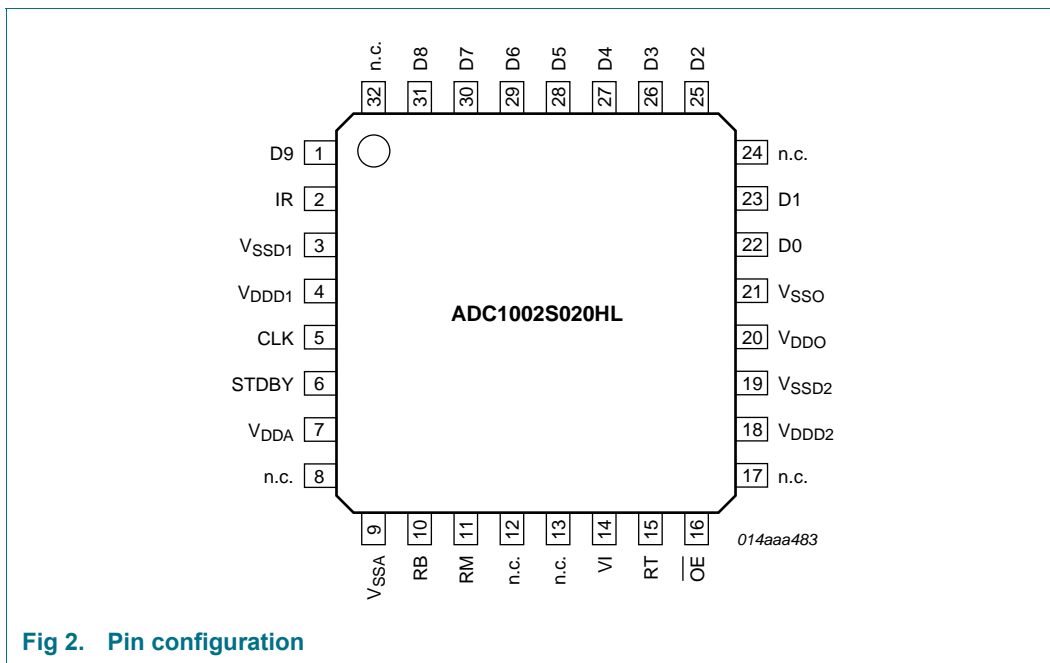


Fig 1. Block diagram

## 7. Pinning information

### 7.1 Pinning



### 7.2 Pin description

**Table 3. Pin description**

| Symbol          | Pin | Description                                     |
|-----------------|-----|---|
| D9              | 1   | data output; bit 9 (Most Significant Bit (MSB)) |
| IR              | 2   | in-range data output                            |
| VSSD1           | 3   | digital ground 1                                |
| VDD1            | 4   | digital supply voltage 1 (3.0 V to 5.25 V)      |
| CLK             | 5   | clock input                                     |
| STDBY           | 6   | standby mode input                              |
| VDDA            | 7   | analog supply voltage (3.0 V to 5.25 V)         |
| n.c.            | 8   | not connected                                   |
| VSSA            | 9   | analog ground                                   |
| RB              | 10  | reference voltage BOTTOM input                  |
| RM              | 11  | reference voltage MIDDLE input                  |
| n.c.            | 12  | not connected                                   |
| n.c.            | 13  | not connected                                   |
| VI              | 14  | analog voltage input                            |
| RT              | 15  | reference voltage TOP input                     |
| $\overline{OE}$ | 16  | output enable input (active LOW)                |
| n.c.            | 17  | not connected                                   |
| VDD2            | 18  | digital supply voltage 2 (3.0 V to 5.25 V)      |

**Table 3. Pin description ...continued**

| Symbol            | Pin | Description  |
|-------------------|-----|--|
| V <sub>SSD2</sub> | 19  | digital ground 2   |
| V <sub>DDO</sub>  | 20  | positive supply voltage for output stage (3.0 V to 5.25 V) |
| V <sub>SSO</sub>  | 21  | output stage ground  |
| D0                | 22  | data output; bit 0 (Least Significant Bit (LSB))           |
| D1                | 23  | data output; bit 1   |
| n.c.              | 24  | not connected  |
| D2                | 25  | data output; bit 2   |
| D3                | 26  | data output; bit 3   |
| D4                | 27  | data output; bit 4   |
| D5                | 28  | data output; bit 5   |
| D6                | 29  | data output; bit 6   |
| D7                | 30  | data output; bit 7   |
| D8                | 31  | data output; bit 8   |
| n.c.              | 32  | not connected  |

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                 | Parameter                         | Conditions  | Min      | Max              | Unit |
|------------------------|-----------------------------------|---|----------|------------------|------|
| V <sub>DDA</sub>       | analog supply voltage             |   | [1] -0.3 | +7.0             | V    |
| V <sub>DDD</sub>       | digital supply voltage            |   | [1] -0.3 | +7.0             | V    |
| V <sub>DDO</sub>       | output supply voltage             |   | [1] -0.3 | +7.0             | V    |
| $\Delta V_{DD}$        | supply voltage difference         | V <sub>DDA</sub> - V <sub>DDD</sub><br>V <sub>DDD</sub> - V <sub>DDO</sub><br>V <sub>DDA</sub> - V <sub>DDO</sub> | -0.1     | +4.0             | V    |
| V <sub>I</sub>         | input voltage                     | referenced to V <sub>SSA</sub>  | -0.3     | +7.0             | V    |
| V <sub>i(a)(p-p)</sub> | peak-to-peak analog input voltage | referenced to V <sub>SSD</sub>  | -        | V <sub>DDD</sub> | V    |
| I <sub>O</sub>         | output current                    |   | -        | 10               | mA   |
| T <sub>stg</sub>       | storage temperature               |   | -55      | +150             | °C   |
| T <sub>amb</sub>       | ambient temperature               |   | -20      | +75              | °C   |
| T <sub>j</sub>         | junction temperature              |   | -        | 150              | °C   |

[1] The supply voltages V<sub>DDA</sub>, V<sub>DDD</sub> and V<sub>DDO</sub> may have any value between -0.3 V and +7.0 V provided that the supply voltage  $\Delta V_{DD}$  remains as indicated.

## 9. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol               | Parameter                                   | Condition   | Value | Unit |
|----------------------|---|-------------|-------|------|
| R <sub>th(j-a)</sub> | thermal resistance from junction to ambient | in free air | 90    | K/W  |

## 10. Characteristics

**Table 6. Characteristics**

$V_{DDA} = V7$  to  $V9 = 3.3$  V;  $V_{DDD} = V4$  to  $V3 = V18$  to  $V19 = 3.3$  V;  $V_{DDO} = V20$  to  $V21 = 3.3$  V;  $V_{SSA}$ ,  $V_{SSD}$  and  $V_{SSO}$  shorted together;  $V_{i(p-p)} = 1.83$  V;  $C_L = 20$  pF;  $T_{amb} = 0$  °C to  $70$  °C; typical values measured at  $T_{amb} = 25$  °C unless otherwise specified.

| Symbol   | Parameter                 | Conditions   | Min           | Typ | Max           | Unit       |
|--|---------------------------|--|---------------|-----|---------------|------------|
| <b>Supplies</b>  |                           |  |               |     |               |            |
| $V_{DDA}$  | analog supply voltage     |  | 3.0           | 3.3 | 5.25          | V          |
| $V_{DDD1}$   | digital supply voltage 1  |  | 3.0           | 3.3 | 5.25          | V          |
| $V_{DDD2}$   | digital supply voltage 2  |  | 3.0           | 3.3 | 5.25          | V          |
| $V_{DDO}$  | output supply voltage     |  | 3.0           | 3.3 | 5.25          | V          |
| $\Delta V_{DD}$  | supply voltage difference | $V_{DDA} - V_{DDD}$ ; $V_{DDD} - V_{DDO}$ ;<br>$V_{DDA} - V_{DDO}$ | -0.2          | -   | +0.2          | V          |
| $I_{DDA}$  | analog supply current     |  | -             | 7.5 | 10            | mA         |
| $I_{DDD}$  | digital supply current    |  | -             | 7.5 | 10            | mA         |
| $I_{DDO}$  | output supply current     | $f_{clk} = 20$ MHz; ramp input;<br>$C_L = 20$ pF                   | -             | 1   | 2             | mA         |
| $P_{tot}$  | total power dissipation   | operating; $V_{DDD} = 3.3$ V                                       | -             | 53  | 73            | mW         |
|  |                           | standby mode   | -             | 4   | -             | mW         |
| <b>Inputs</b>  |                           |  |               |     |               |            |
| Clock input CLK (Referenced to $V_{SSD}$ ); <sup>[1]</sup>                     |                           |  |               |     |               |            |
| $V_{IL}$   | LOW-level input voltage   |  | 0             | -   | $0.3 V_{DDD}$ | V          |
| $V_{IH}$   | HIGH-level input voltage  | $V_{DDD} \leq 3.6$ V   | $0.6 V_{DDD}$ | -   | $V_{DDD}$     | V          |
|  |                           | $V_{DDD} > 3.6$ V  | $0.7 V_{DDD}$ | -   | $V_{DDD}$     | V          |
| $I_{IL}$   | LOW-level input current   | $V_{CLK} = 0.3 V_{DDD}$  | -1            | 0   | +1            | $\mu$ A    |
| $I_{IH}$   | HIGH-level input current  | $V_{CLK} = 0.7 V_{DDD}$  | -             | -   | 5             | $\mu$ A    |
| $Z_i$  | input impedance           | $f_{clk} = 20$ MHz   | -             | 4   | -             | k $\Omega$ |
| $C_i$  | input capacitance         | $f_{clk} = 20$ MHz   | -             | 3   | -             | pF         |
| Inputs $\overline{OE}$ and STDBY (Referenced to $V_{SSD}$ ); see Table 7 and 8 |                           |  |               |     |               |            |
| $V_{IL}$   | LOW-level input voltage   |  | 0             | -   | $0.3 V_{DDD}$ | V          |
| $V_{IH}$   | HIGH-level input voltage  | $V_{DDD} \leq 3.6$ V   | $0.6 V_{DDD}$ | -   | $V_{DDD}$     | V          |
|  |                           | $V_{DDD} > 3.6$ V  | $0.7 V_{DDD}$ | -   | $V_{DDD}$     | V          |
| $I_{IL}$   | LOW-level input current   | $V_{IL} = 0.3 V_{DDD}$   | -1            | -   | -             | $\mu$ A    |
| $I_{IH}$   | HIGH-level input current  | $V_{IH} = 0.7 V_{DDD}$   | -             | -   | 1             | $\mu$ A    |
| Analog input VI (Referenced to $V_{SSA}$ )                                     |                           |  |               |     |               |            |
| $I_{IL}$   | LOW-level input current   | $V_I = V_{RB}$   | -             | 0   | -             | $\mu$ A    |
| $I_{IH}$   | HIGH-level input current  | $V_I = V_{RT}$   | -             | 35  | -             | $\mu$ A    |
| $Z_i$  | input impedance           | $f_i = 1$ MHz  | -             | 5   | -             | k $\Omega$ |
| $C_i$  | input capacitance         | $f_i = 1$ MHz  | -             | 8   | -             | pF         |
| Reference voltages for the resistor ladder; see Table 8                        |                           |  |               |     |               |            |
| $V_{RB}$   | voltage on pin RB         |  | 1.1           | 1.2 | -             | V          |
| $V_{RT}$   | voltage on pin RT         |  | 3.0           | 3.3 | $V_{DDA}$     | V          |

**Table 6. Characteristics ...continued**

$V_{DDA} = V7$  to  $V9 = 3.3$  V;  $V_{DDD} = V4$  to  $V3 = V18$  to  $V19 = 3.3$  V;  $V_{DDO} = V20$  to  $V21 = 3.3$  V;  $V_{SSA}$ ,  $V_{SSD}$  and  $V_{SSO}$  shorted together;  $V_{i(p-p)} = 1.83$  V;  $C_L = 20$  pF;  $T_{amb} = 0$  °C to 70 °C; typical values measured at  $T_{amb} = 25$  °C unless otherwise specified.

| Symbol  | Parameter                               | Conditions                       | Min             | Typ        | Max       | Unit          |
|---|---|----------------------------------|-----------------|------------|-----------|---------------|
| $V_{ref(dif)}$  | differential reference voltage          | $V_{RT} - V_{RB}$                | 1.9             | 2.1        | 3.0       | V             |
| $I_{ref}$   | reference current                       |                                  | -               | 7.2        | -         | mA            |
| $R_{lad}$   | ladder resistance                       |                                  | -               | 290        | -         | $\Omega$      |
| $TC_{Rlad}$   | ladder resistor temperature coefficient |                                  | -               | 539        | -         | m $\Omega$ /K |
| $V_{offset}$  | offset voltage                          | BOTTOM                           | [2] -           | 135        | -         | mV            |
|   |   | TOP                              | [2] -           | 135        | -         | mV            |
| $V_{i(p-p)}$  | peak-to-peak input voltage              |                                  | [3] 1.66        | 1.83       | 2.35      | V             |
| <b>Digital outputs D9 to D0 and IR (Referenced to <math>V_{SSD}</math>)</b>   |   |                                  |                 |            |           |               |
| $V_{OL}$  | LOW-level output voltage                | $I_O = 1$ mA                     | 0               | -          | 0.5       | V             |
| $V_{OH}$  | HIGH-level output voltage               | $I_O = -1$ mA                    | $V_{DDO} - 0.5$ | -          | $V_{CCO}$ | V             |
| $I_{OZ}$  | OFF-state output current                | $0.5$ V < $V_O$ < $V_{DDO}$      | -20             | -          | +20       | $\mu$ A       |
| <b>Switching characteristics; Clock input CLK; see Figure 4<sup>[1]</sup></b> |   |                                  |                 |            |           |               |
| $f_{clk(max)}$  | maximum clock frequency                 |                                  | 20              | -          | -         | MHz           |
| $t_{w(clk)H}$   | HIGH clock pulse width                  |                                  | 15              | -          | -         | ns            |
| $t_{w(clk)L}$   | LOW clock pulse width                   |                                  | 15              | -          | -         | ns            |
| <b>Analog signal processing (<math>f_{clk} = 20</math> MHz)</b>               |   |                                  |                 |            |           |               |
| <b>Linearity</b>  |   |                                  |                 |            |           |               |
| INL   | integral non-linearity                  | ramp input; see Figure 6         | -               | $\pm 1$    | $\pm 2$   | LSB           |
| DNL   | differential non-linearity              | ramp input; see Figure 7         | -               | $\pm 0.25$ | $\pm 0.7$ | LSB           |
| <b>Input set response; see Figure 8<sup>[4]</sup></b>                         |   |                                  |                 |            |           |               |
| $t_{s(LH)}$   | LOW to HIGH settling time               | full-scale square wave           | -               | 4          | 6         | ns            |
| $t_{s(HL)}$   | HIGH to LOW settling time               | full-scale square wave           | -               | 4          | 6         | ns            |
| <b>Harmonics; see Figure 9<sup>[5]</sup></b>                                  |   |                                  |                 |            |           |               |
| THD   | total harmonic distortion               | $f_i = 1$ MHz                    | -               | -63        | -         | dB            |
| <b>Signal-to-Noise ratio; see Figure 9<sup>[5]</sup></b>                      |   |                                  |                 |            |           |               |
| S/N   | signal-to-noise ratio                   | without harmonics; $f_i = 1$ MHz | -               | 60         | -         | dB            |
| <b>Effective bits; see Figure 9<sup>[5]</sup></b>                             |   |                                  |                 |            |           |               |
| ENOB  | effective number of bits                | $f_i = 300$ KHz                  | -               | 9.5        | -         | bits          |
|   |   | $f_i = 1$ MHz                    | -               | 9.3        | -         | bits          |
|   |   | $f_i = 3.58$ MHz                 | -               | 8.0        | -         | bits          |

**Table 6. Characteristics ...continued**

$V_{DDA} = V7$  to  $V9 = 3.3$  V;  $V_{DDD} = V4$  to  $V3 = V18$  to  $V19 = 3.3$  V;  $V_{DDO} = V20$  to  $V21 = 3.3$  V;  $V_{SSA}$ ,  $V_{SSD}$  and  $V_{SSO}$  shorted together;  $V_{i(p-p)} = 1.83$  V;  $C_L = 20$  pF;  $T_{amb} = 0$  °C to  $70$  °C; typical values measured at  $T_{amb} = 25$  °C unless otherwise specified.

| Symbol   | Parameter                       | Conditions         | Min | Typ | Max | Unit |
|--|---------------------------------|--------------------|-----|-----|-----|------|
| <b>Timing (<math>f_{clk} = 20</math> MHz; <math>C_L = 20</math> pF); see Figure4<sup>[6]</sup></b> |                                 |                    |     |     |     |      |
| $t_{d(s)}$   | sampling delay time             |                    | -   | -   | 5   | ns   |
| $t_{h(o)}$   | output hold time                |                    | 5   | -   | -   | ns   |
| $t_{d(o)}$   | output delay time               | $V_{DDO} = 4.75$ V | 8   | 12  | 15  | ns   |
|  |                                 | $V_{DDO} = 3.15$ V | 8   | 17  | 20  | ns   |
| <b>3-state output delay times; see Figure 5</b>  |                                 |                    |     |     |     |      |
| $t_{dZH}$  | float to active HIGH delay time |                    | -   | 14  | 18  | ns   |
| $t_{dZL}$  | float to active LOW delay time  |                    | -   | 16  | 20  | ns   |
| $t_{dHZ}$  | active HIGH to float delay time |                    | -   | 16  | 20  | ns   |
| $t_{dLZ}$  | active LOW to float delay time  |                    | -   | 14  | 18  | ns   |
| <b>Standby mode output delay times</b>   |                                 |                    |     |     |     |      |
| $t_{TLH}$  | LOW to HIGH transition time     | stand-by           | -   | -   | 200 | ns   |
| $t_{THL}$  | HIGH to LOW transition time     | start-up           | -   | -   | 500 | ns   |

- [1] In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
- [2] Analog input voltages producing code 0 up to and including code 1023:
  - a)  $V_{offset}$  BOTTOM is the difference between the analog input which produces data equal to 00 and the reference voltage on pin RB ( $V_{RB}$ ) at  $T_{amb} = 25$  °C.
  - b)  $V_{offset}$  TOP is the difference between the reference voltage on pin RT ( $V_{RT}$ ) and the analog input which produces data outputs equal to code 1023 at  $T_{amb} = 25$  °C.
- [3] To ensure the optimum linearity performance of such a converter architecture the lower and upper extremities of the converter reference resistor ladder are connected to pins RB and RT via offset resistors  $R_{OB}$  and  $R_{OT}$  as shown in Figure 3.
  - a) The current flowing into the resistor ladder is  $I = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$  and the full-scale input range at the converter, to cover code 0 to 1023 is  $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} + V_{RB}) = 0.871 \times (V_{RT} - V_{RB})$
  - b) Since  $R_L$ ,  $R_{OB}$  and  $R_{OT}$  have similar behavior with respect to process and temperature variation, the ratio  $\frac{R_L}{R_{OB} + R_L + R_{OT}}$  will be kept reasonably constant from device to device. Consequently variation of the output codes at a given input voltage depends mainly on the difference  $V_{RT} - V_{RB}$  and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is optimized.
- [4] The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data.
- [5] Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8000 acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half the clock frequency (Nyquist frequency). Conversion to Signal-to-Noise And Distortion (SINAD) ratio:  $SINAD = ENOB \times 6.02 + 1.76$  dB.
- [6] Output data acquisition: the output data is available after the maximum delay time of  $t_{d(o)}$ .



### 11. Additional information relating to Table 6

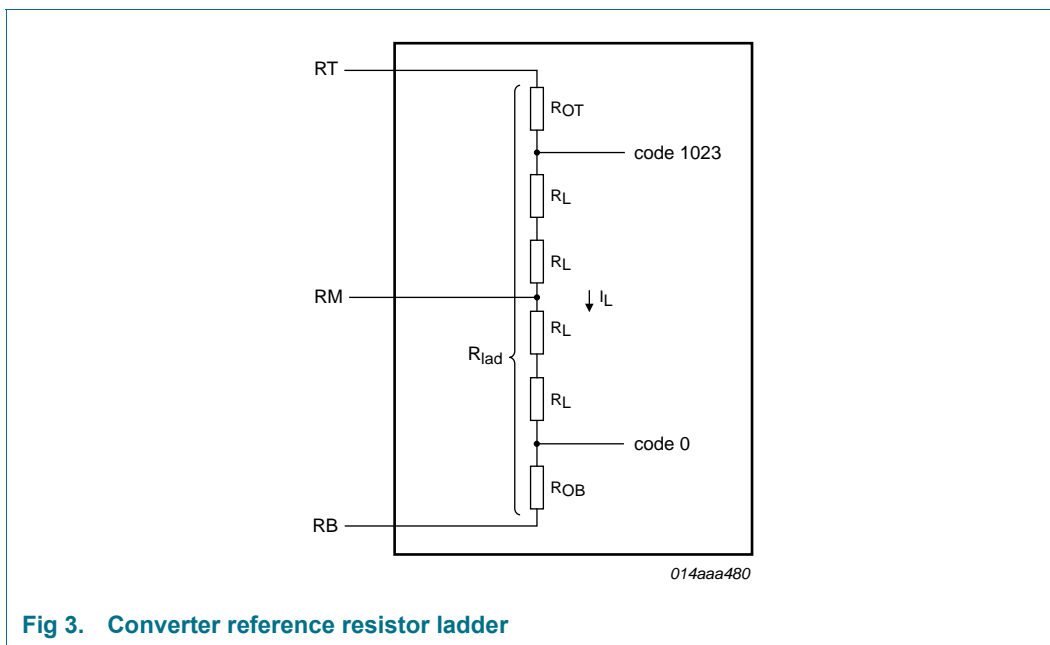


Fig 3. Converter reference resistor ladder

Table 7. Mode selection

| OE | D9 to D0       | IR             |
|----|----------------|----------------|
| 1  | high impedance | high impedance |
| 0  | active; binary | active         |

Table 8. Standby selection

| STBY | D9 to D0         | I <sub>CCA</sub> + I <sub>CCD</sub> |
|------|------------------|-------------------------------------|
| 1    | last logic state | 1.2 mA (typical value)              |
| 0    | active           | 15 mA (typical value)               |

Table 9. Output coding and input voltage (typical values; referenced to V<sub>SSA</sub>)

| Code      | V <sub>i(a)(p-p)</sub> (V) | IR | Binary outputs D9 to D0 |
|-----------|----------------------------|----|-------------------------|
| Underflow | < 1.335                    | 0  | 00 0000 0000            |
| 0         | 1.335                      | 1  | 00 0000 0000            |
| 1         | -                          | 1  | 00 0000 0001            |
| ↓         | -                          | ↓  | ↓                       |
| 1022      | -                          | 1  | 11 1111 1110            |
| 1023      | 3.165                      | 1  | 11 1111 1111            |
| Overflow  | > 3.165                    | 0  | 11 1111 1111            |

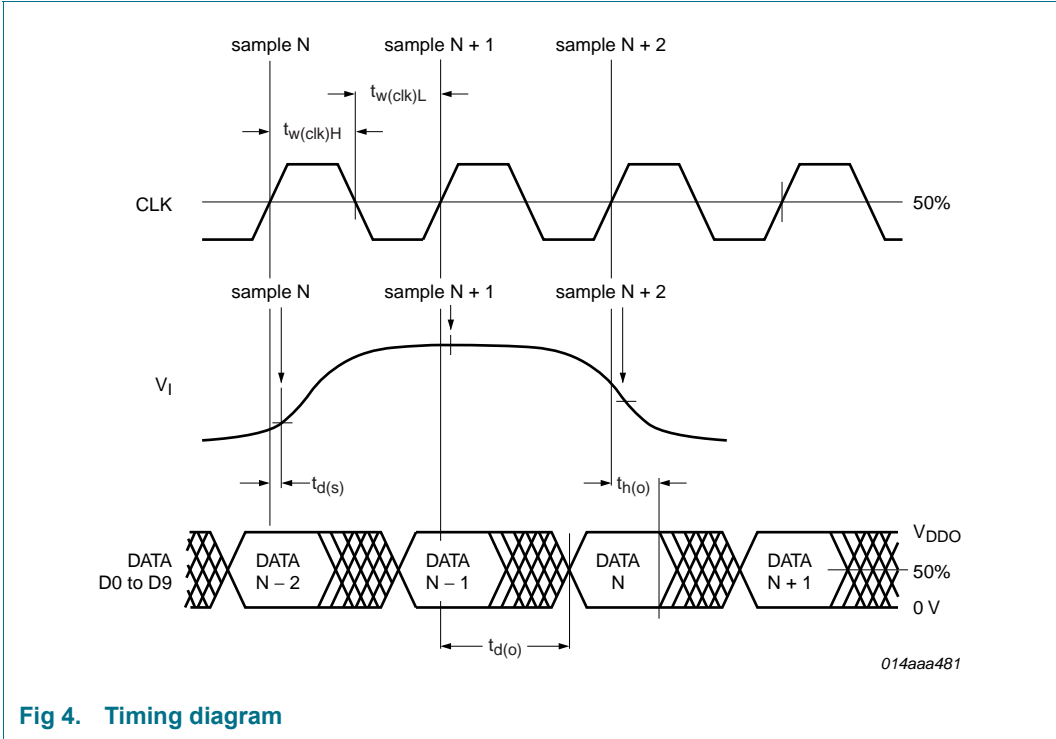
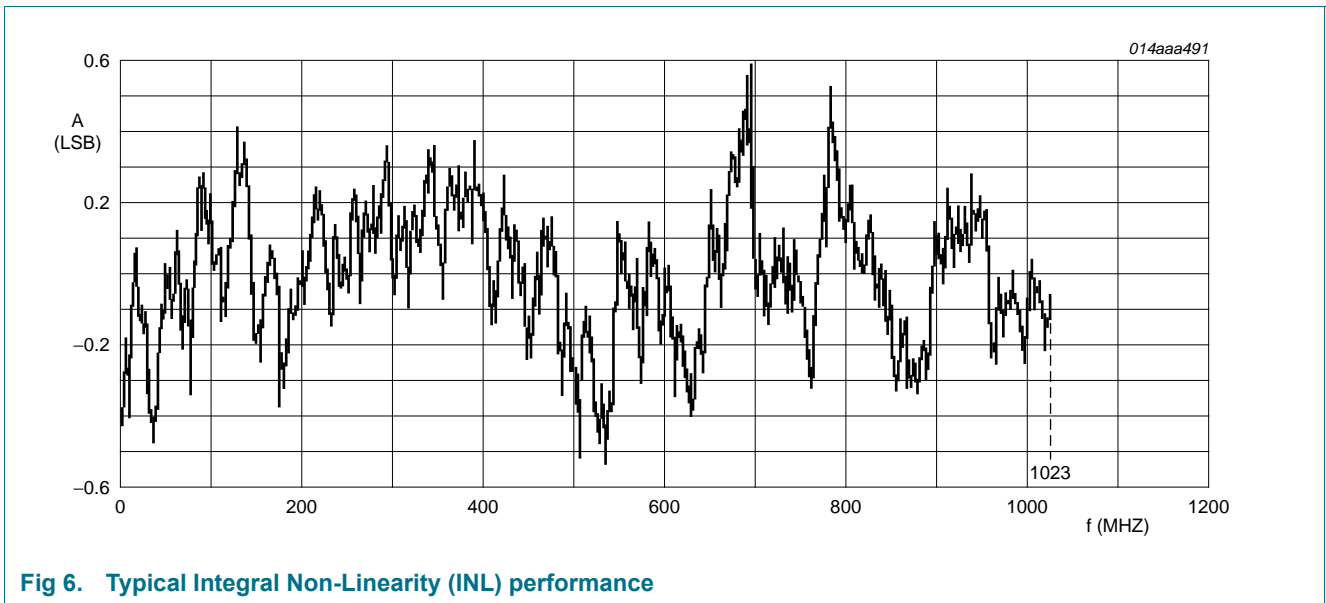
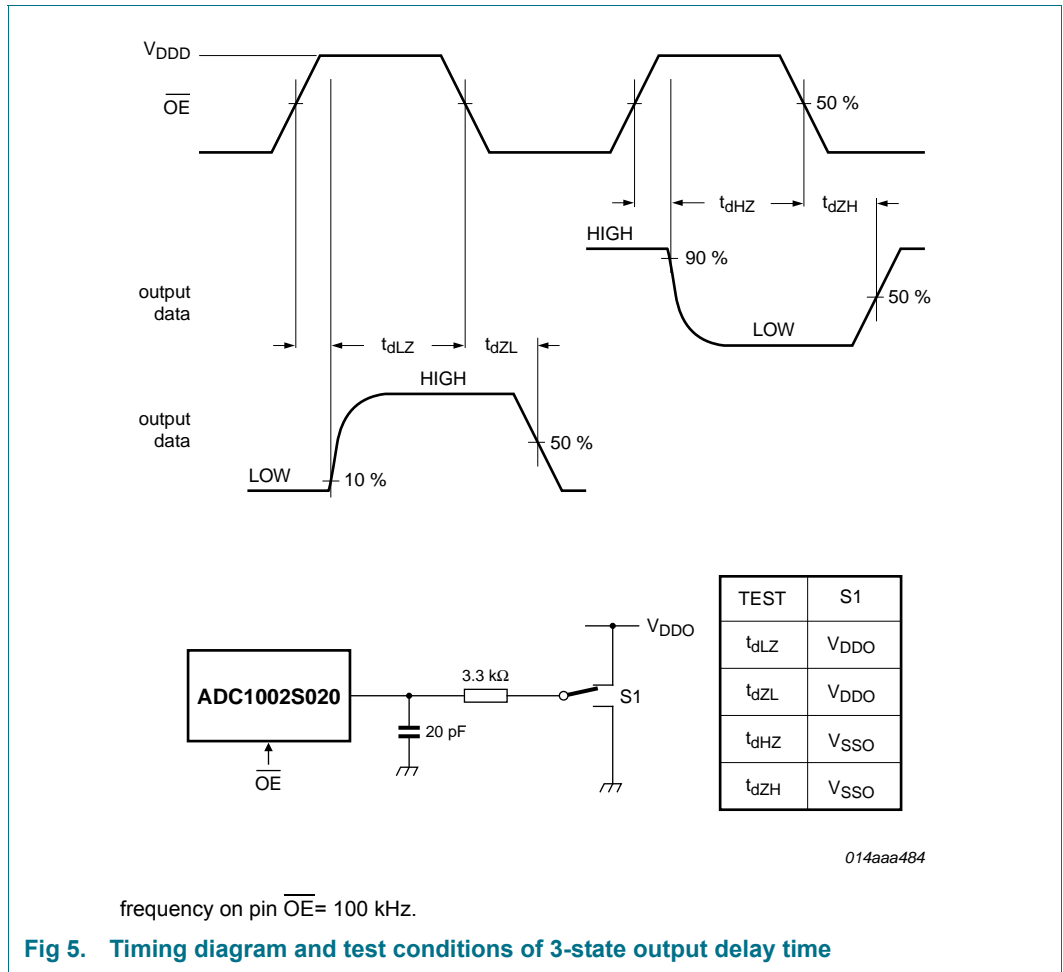
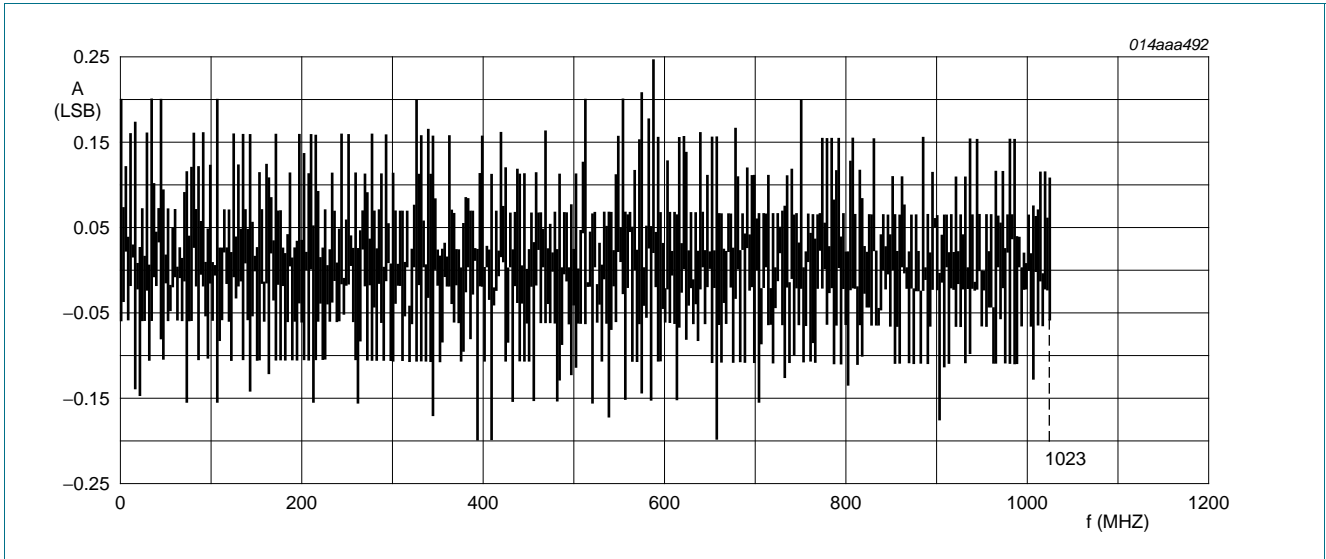
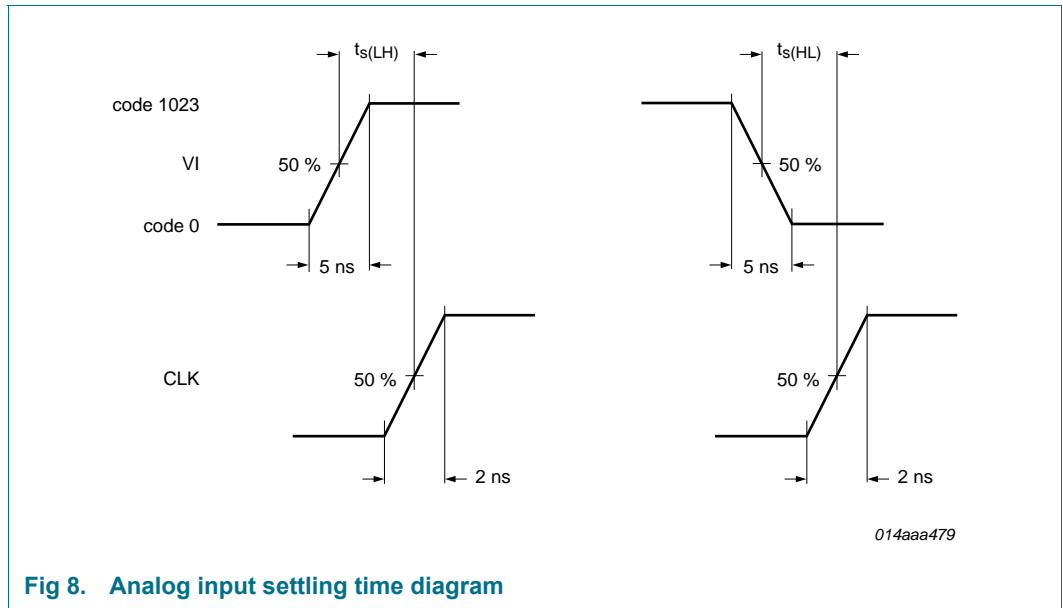


Fig 4. Timing diagram

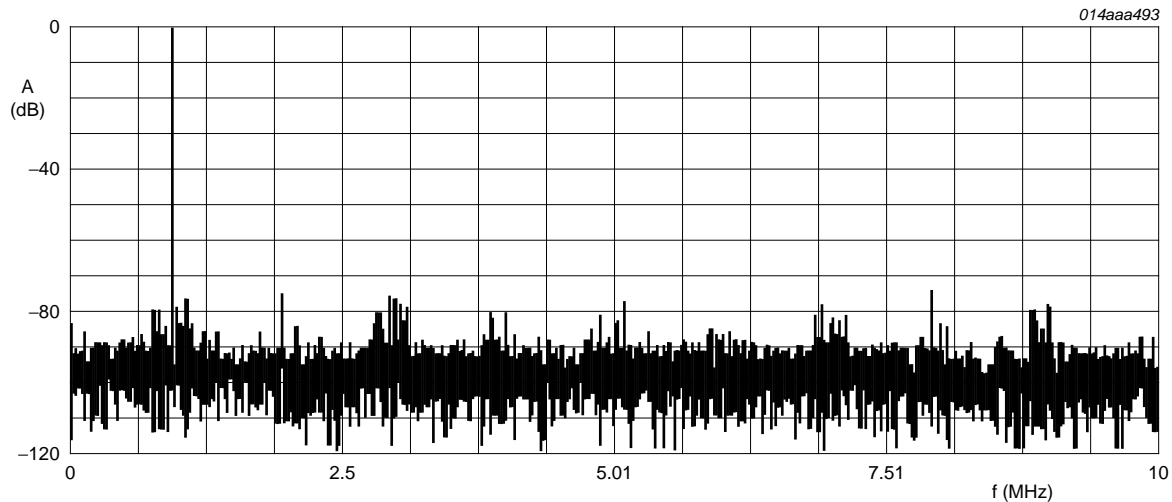




**Fig 7. Typical Differential Non-Linearity (DNL) performance**



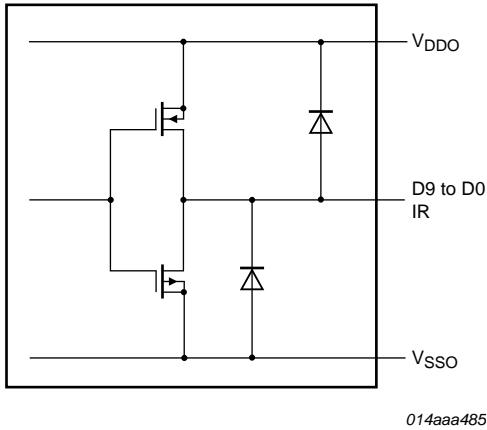
**Fig 8. Analog input settling time diagram**



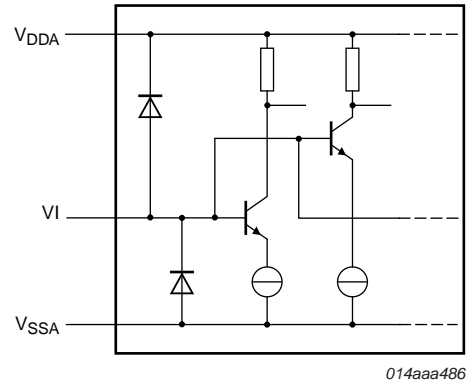
Effective bits: 9.59; THD = -76.60 dB.

Harmonic levels (dB): 2nd = -81.85; 3rd = -87.56; 4th = -88.81; 5th = -88.96; 6th = -79.58.

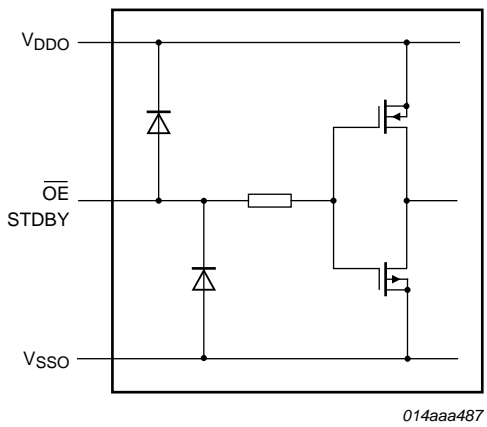
**Fig 9. Typical fast Fourier transform ( $f_{clk} = 20 \text{ MHz}$ ;  $f_i = 1 \text{ MHz}$ )**



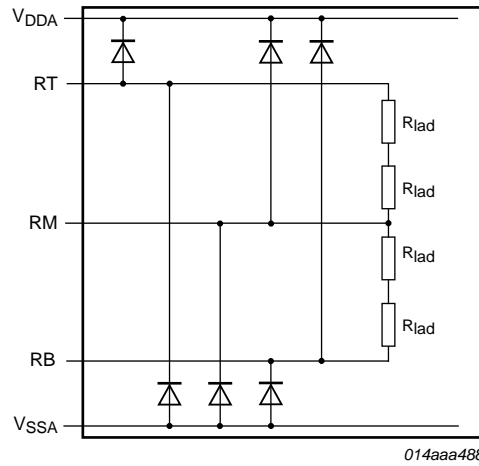
**Fig 10. D9 to D0 and IR outputs**



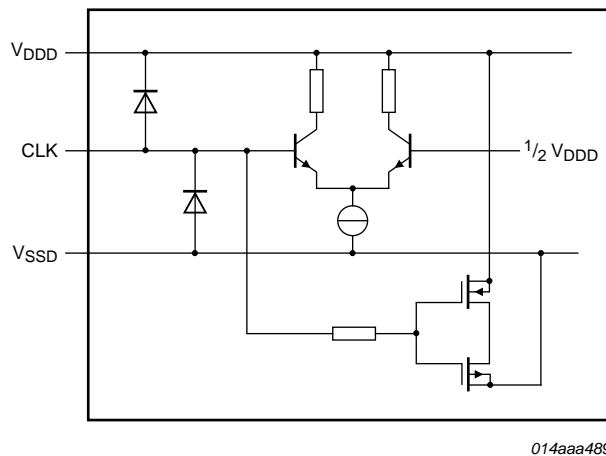
**Fig 11. VI analog input**



**Fig 12. OE and STDBY inputs**



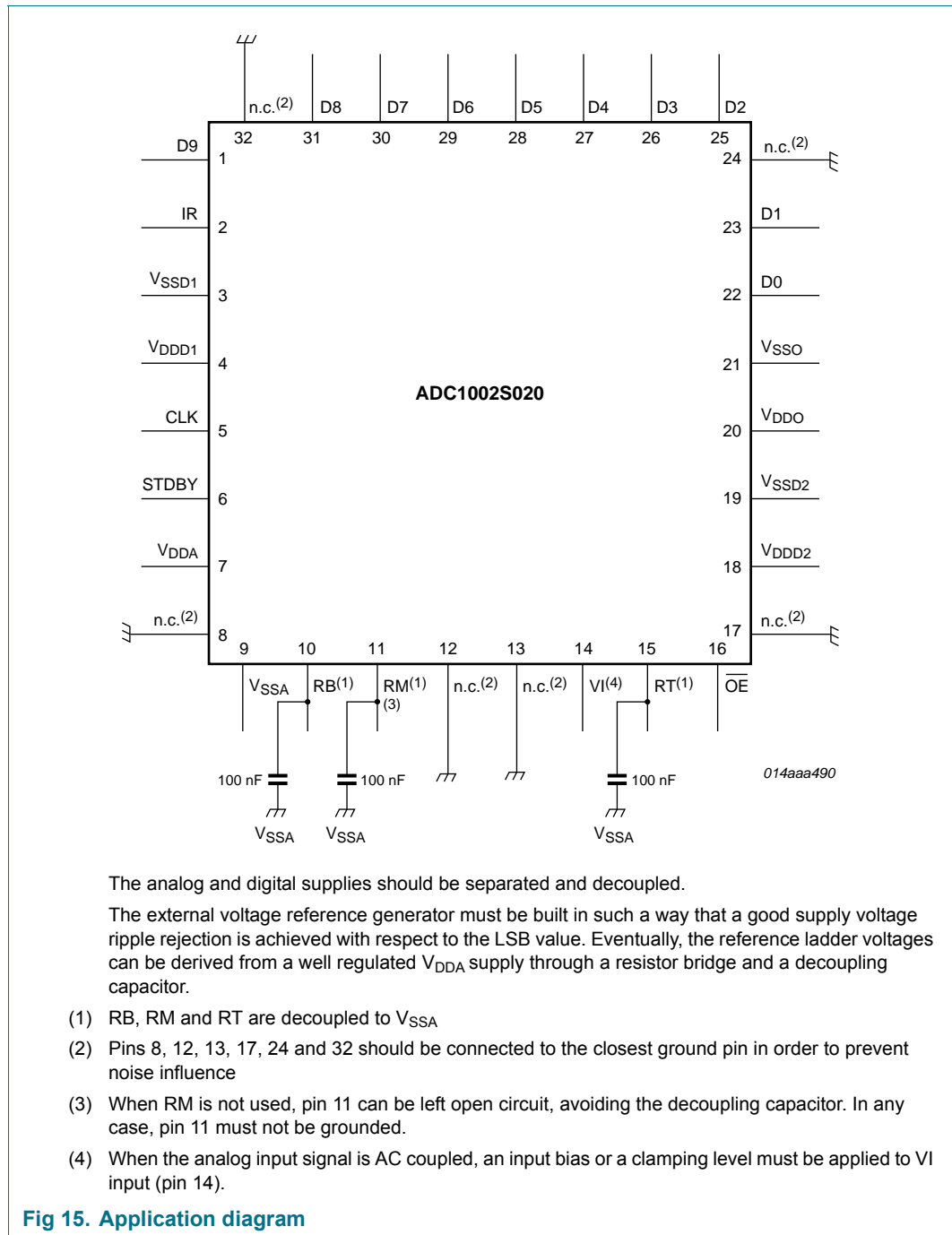
**Fig 13. RB, RM and RT inputs**



**Fig 14. CLK input**

## 12. Application information

### 12.1 Application diagram



13. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm

SOT401-1

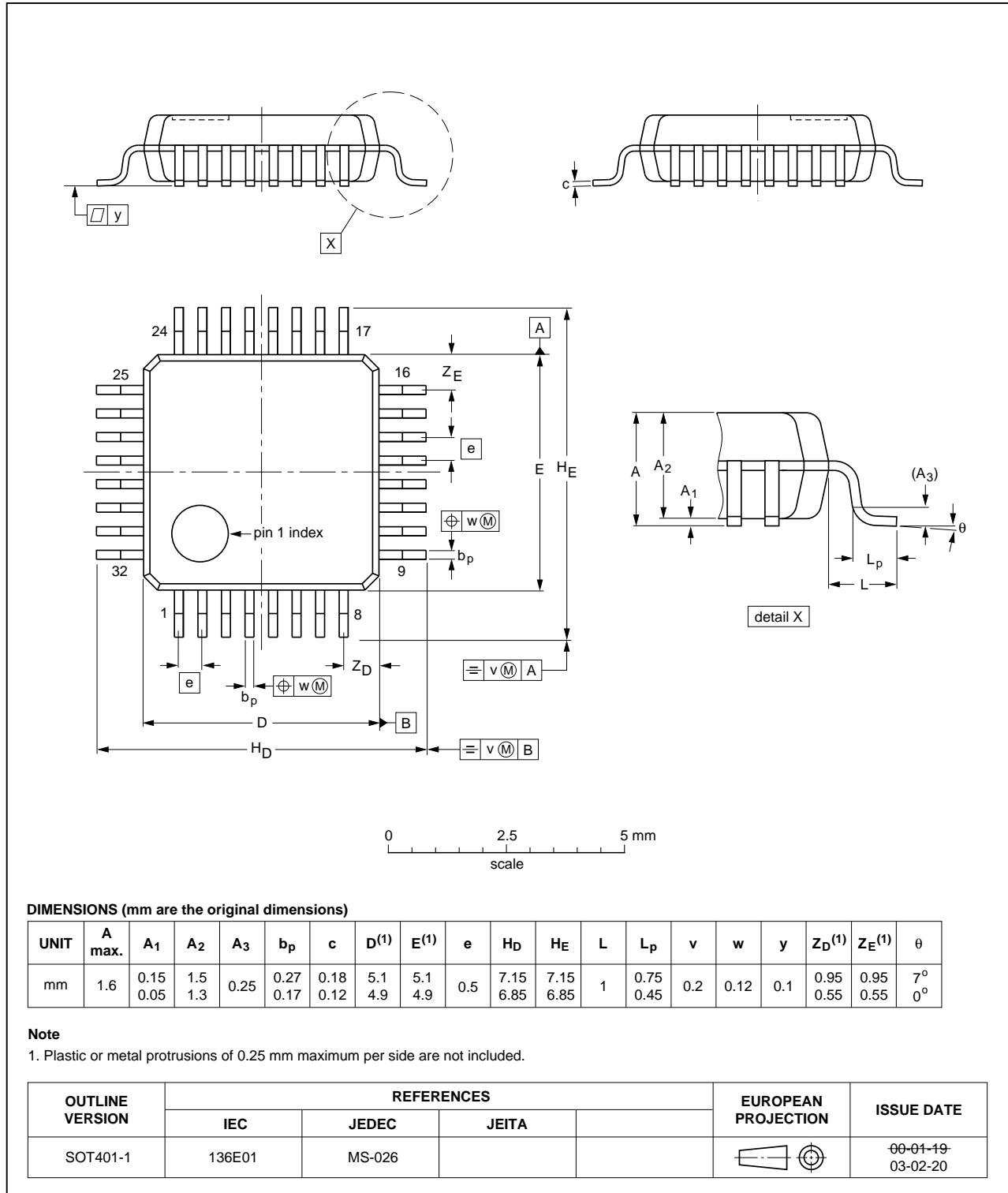


Fig 16. Package outline SOT401-1 (LQFP32)



## 14. Revision history

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Table 10. Revision history

| Document ID    | Release date   | Data sheet status  | Change notice | Supersedes    |
|----------------|--|--------------------|---------------|---------------|
| ADC1002S020_3  | 20120702   | Product data sheet | -             | ADC1002S020_2 |
| ADC1002S020_2  | 20080813   | Product data sheet | -             | ADC1002S020_1 |
| Modifications: | • Corrections made to cross references and note 3 a) in Table 6. |                    |               |               |
| ADC1002S020_1  | 20080612   | Product data sheet | -             | -             |

## 15. Contact information

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For more information or sales office addresses, please visit: <http://www.idt.com>

## 16. Contents

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