

# FG694301

Silicon N-channel MOS FET (FET1)  
Silicon P-channel MOS FET (FET2)

For switching circuits

## ■ Overview

FG694301 is N-P channel dual type small signal MOS FET employed small size surface mounting package.

## ■ Features

- Low drain-source ON resistance:  
 $R_{DS(on)}$  typ. =  $2\ \Omega$  ( $V_{GS} = 4.0\ V$ ) /  $4\ \Omega$  ( $V_{GS} = -4.0\ V$ )
- High-speed switching
- Small size surface mounting package: SSMini6-F3-B
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

## ■ Packaging

Embossed type (Thermo-compression sealing): 8000 pcs / reel (standard)

## ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

	Parameter	Symbol	Rating	Unit
FET1	Drain-source surrender voltage	$V_{DSS}$	30	V
	Gate-source surrender voltage	$V_{GSS}$	$\pm 12$	V
	Drain current	$I_D$	100	mA
	Peak drain current	$I_{DP}$	200	mA
FET2	Drain-source surrender voltage	$V_{DSS}$	-30	V
	Gate-source surrender voltage	$V_{GSS}$	$\pm 12$	V
	Drain current	$I_D$	-100	mA
	Peak drain current	$I_{DP}$	-200	mA
Overall	Total power dissipation	$P_T$	125	mW
	Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
	Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

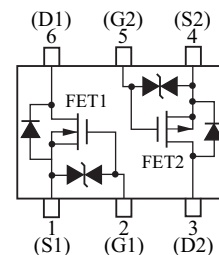
## ■ Package

- Code  
SSMini6-F3-B
- Pin Name
 

1: Source (FET1)	4: Source (FET2)
2: Gate (FET1)	5: Gate (FET2)
3: Drain (FET2)	6: Drain (FET1)

## ■ Marking Symbol: V7

## ■ Internal Connection



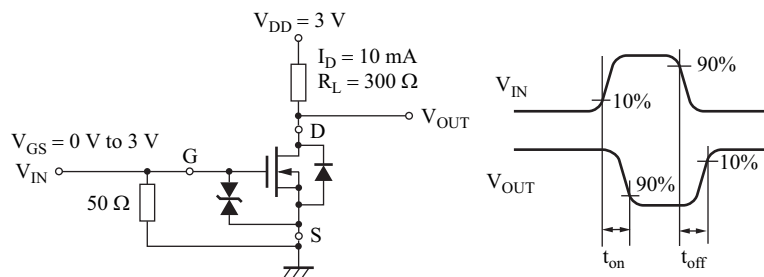
■ Electrical Characteristics  $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

• FET1

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	$V_{DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0$	30			V
Drain-source cutoff current	$I_{DSS}$	$V_{DS} = 30 \text{ V}, V_{GS} = 0$			1.0	$\mu\text{A}$
Gate-source cutoff current	$I_{GSS}$	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$			$\pm 10$	$\mu\text{A}$
Gate threshold voltage	$V_{TH}$	$I_D = 1.0 \text{ }\mu\text{A}, V_{DS} = 3.0 \text{ V}$	0.5	1.0	1.5	V
Drain-source ON resistance	$R_{DS(on)}$	$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$		3	6	$\Omega$
		$I_D = 10 \text{ mA}, V_{GS} = 4.0 \text{ V}$		2	3	
Forward transfer admittance	$ Y_{fs} $	$I_D = 10 \text{ mA}, V_{DS} = 3.0 \text{ V}$	20	55		mS
Short-circuit input capacitance (Common source)	$C_{iss}$	$V_{DS} = 3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		12		pF
Short-circuit output capacitance (Common source)	$C_{oss}$			7		pF
Reverse transfer capacitance (Common source)	$C_{rss}$			3		pF
Turn-on time *	$t_{on}$	$V_{DD} = 3 \text{ V}, V_{GS} = 0 \text{ V to } 3 \text{ V}, I_D = 10 \text{ mA}$		100		ns
Turn-off time *	$t_{off}$	$V_{DD} = 3 \text{ V}, V_{GS} = 3 \text{ V to } 0 \text{ V}, I_D = 10 \text{ mA}$		100		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*: Test circuit

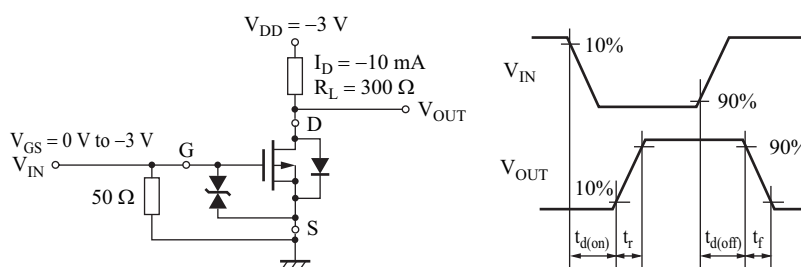


• FET2

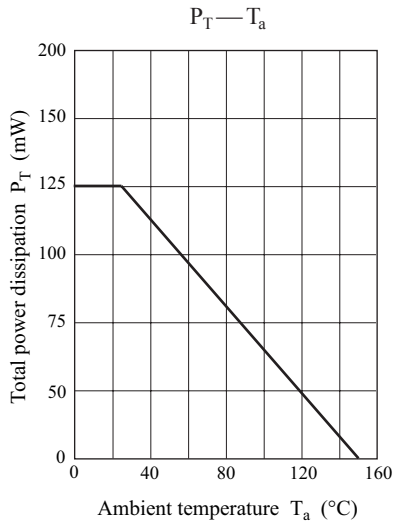
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	$V_{DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0$	-30			V
Drain-source cutoff current	$I_{DSS}$	$V_{DS} = -30 \text{ V}, V_{GS} = 0$			-1.0	$\mu\text{A}$
Gate-source cutoff current	$I_{GSS}$	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$			$\pm 10$	$\mu\text{A}$
Gate threshold voltage	$V_{TH}$	$I_D = -1.0 \text{ }\mu\text{A}, V_{DS} = -3.0 \text{ V}$	-0.5	-1.0	-1.5	V
Drain-source ON resistance	$R_{DS(on)}$	$I_D = -10 \text{ mA}, V_{GS} = -2.5 \text{ V}$		7	17	$\Omega$
		$I_D = -10 \text{ mA}, V_{GS} = -4.0 \text{ V}$		4	7	
Forward transfer admittance	$ Y_{fs} $	$I_D = -10 \text{ mA}, V_{DS} = -3.0 \text{ V}$	20	40		mS
Short-circuit input capacitance (Common source)	$C_{iss}$	$V_{DS} = -3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		12		pF
Short-circuit output capacitance (Common source)	$C_{oss}$			7		pF
Reverse transfer capacitance (Common source)	$C_{rss}$			3		pF
Turn-on time *	$t_{on}$	$V_{DD} = -3 \text{ V}, V_{GS} = 0 \text{ V to } -3 \text{ V}, I_D = -10 \text{ mA}$		100		ns
Turn-off time *	$t_{off}$	$V_{DD} = -3 \text{ V}, V_{GS} = -3 \text{ V to } 0 \text{ V}, I_D = -10 \text{ mA}$		100		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

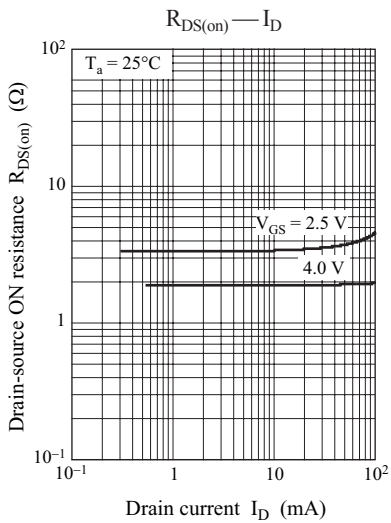
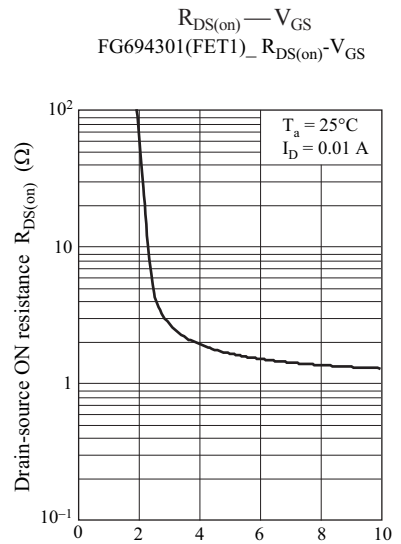
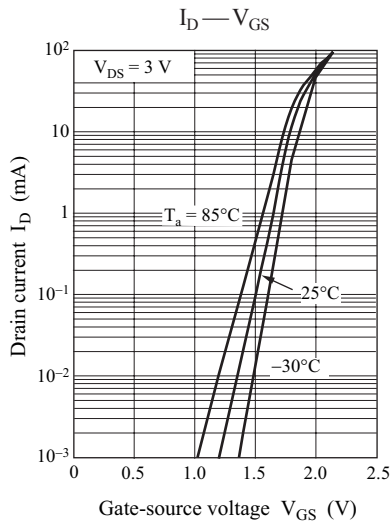
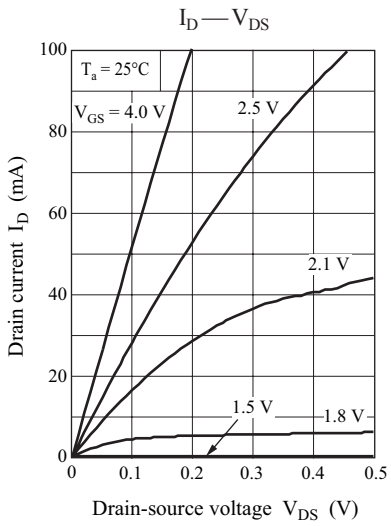
2. \*: Test circuit

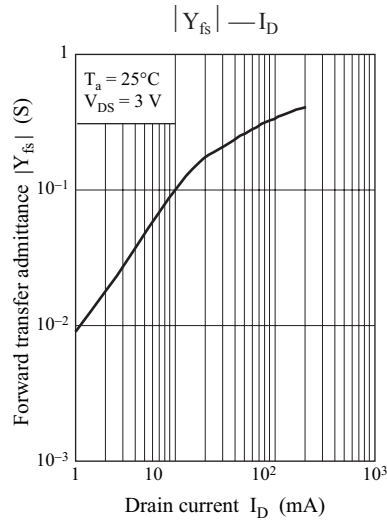
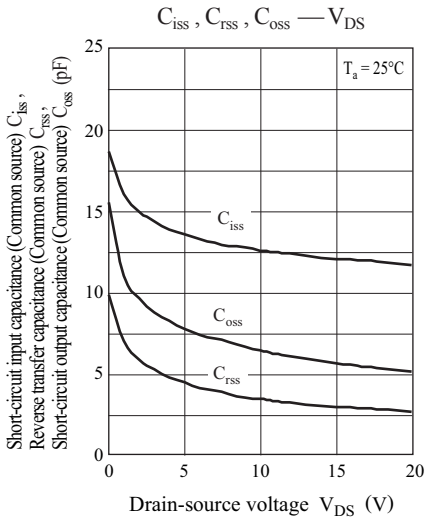


Common characteristics chart

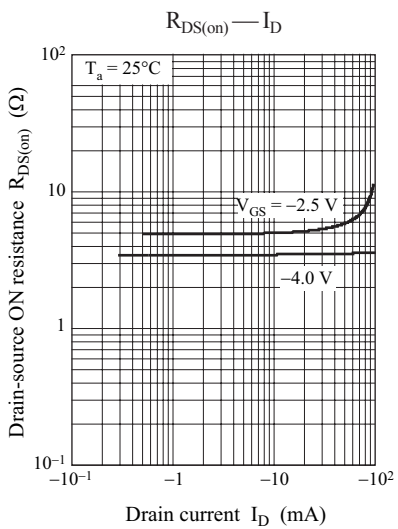
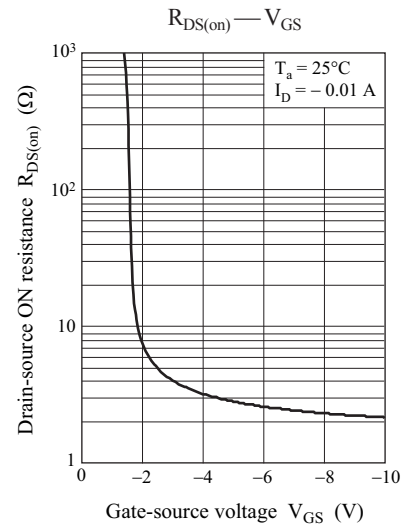
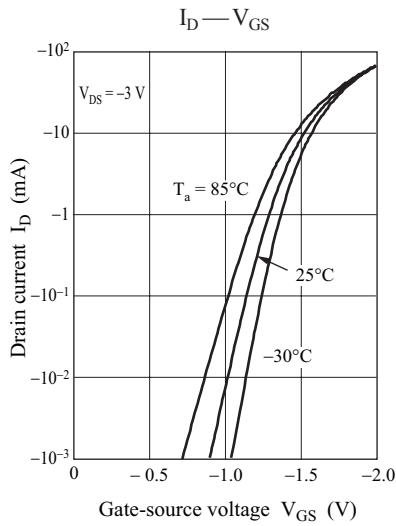
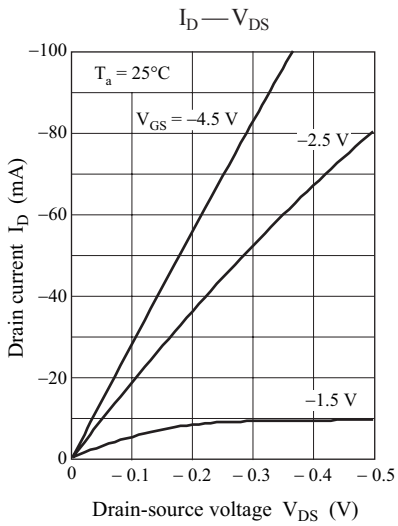


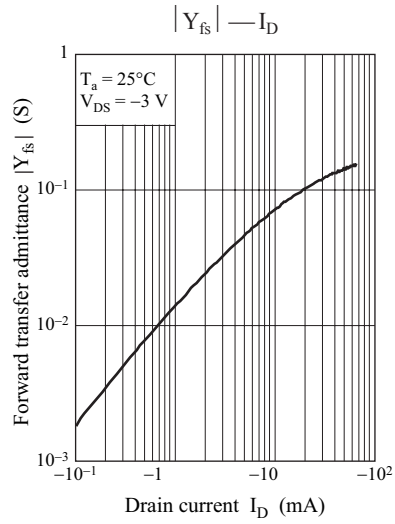
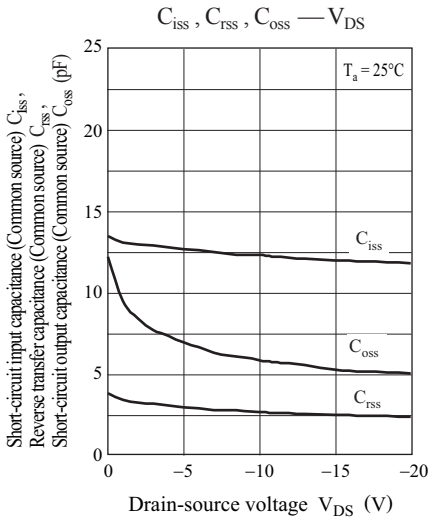
Characteristics charts of FET1





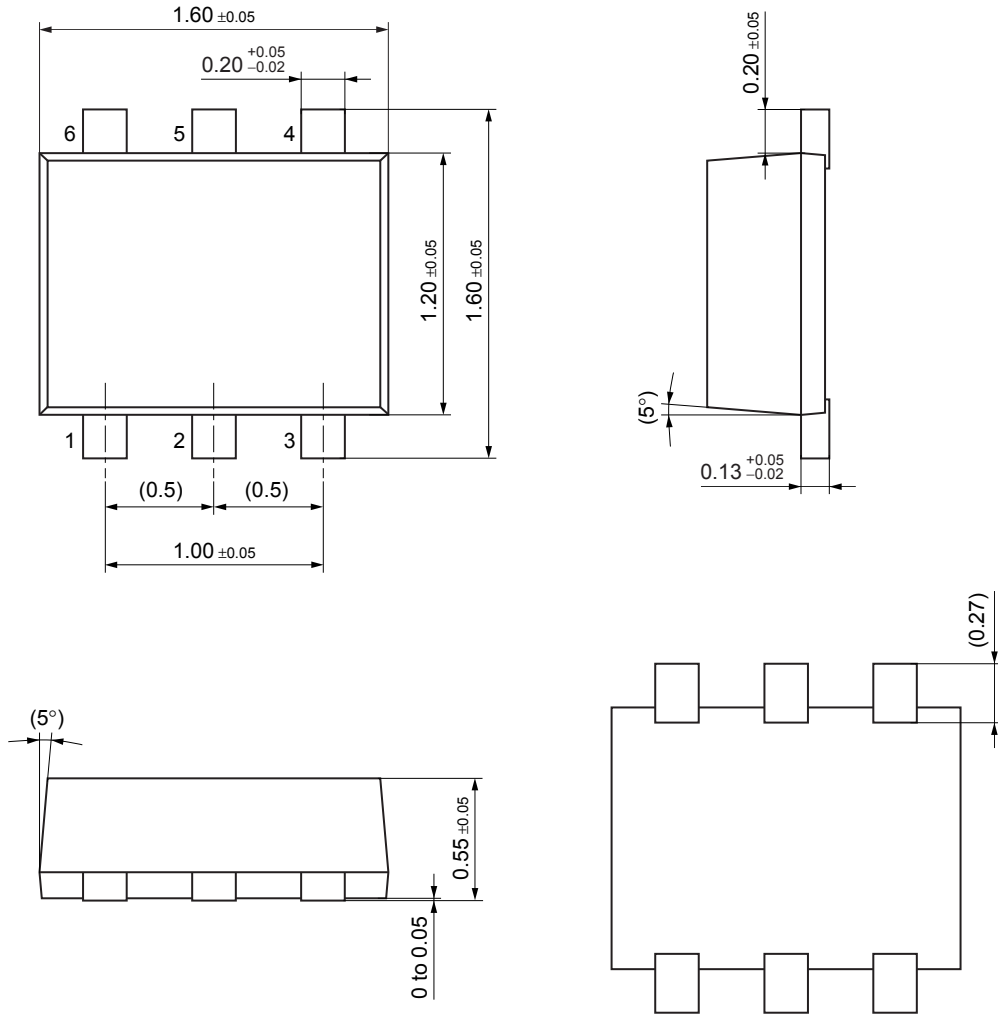
Characteristics charts of FET2





SSMini6-F3-B

Unit: mm



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