

# R2A20158NP

8-bit 8ch D/A Converter with Buffer Amplifiers for I<sup>2</sup>C BUS (Corresponds to Fast mode)

R03DS0015EJ0100

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## Description

The R2A20158NP is an integrated circuit semiconductor of CMOS structure with 8 channels of built in D/A converters with output buffer operational amplifiers. It is the electrical characteristic improvement version of the M62393.

The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring. This IC corresponds to Fast mode of I<sup>2</sup>C BUS standard.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 1.0mA or more, and it operates in the whole voltage range from V<sub>CC</sub> to ground.

Maximum 8 ICs can be connected to a bus by using 3-chip select pins, so that it is possible to handle up to 64 channels analog data.

## Features

- Guarantee Differential nonlinearity error : +/-0.7LSB, Nonlinearity error : +/-1.0LSB
- Digital data transfer format: I<sup>2</sup>C BUS serial data method (corresponds to Fast mode: 400kHz)
- Output buffer operational amplifier  
It operates in the whole range from V<sub>CC</sub> to ground.
- High output current drive capacity: 1mA over
- The very small size (4mmX4mm) QFN-20 package is added to the lineup.

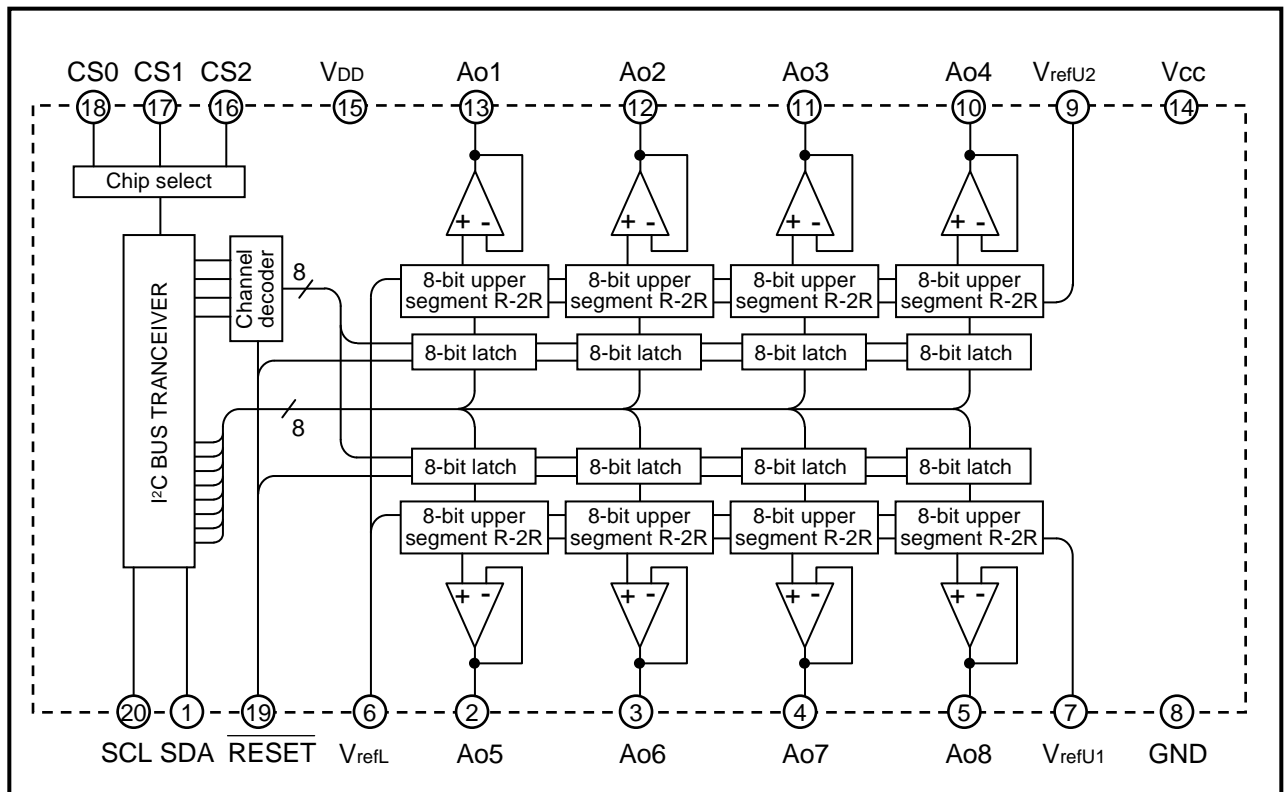
## Application

Conversion from digital data to analog control data for home-use and industrial equipment.

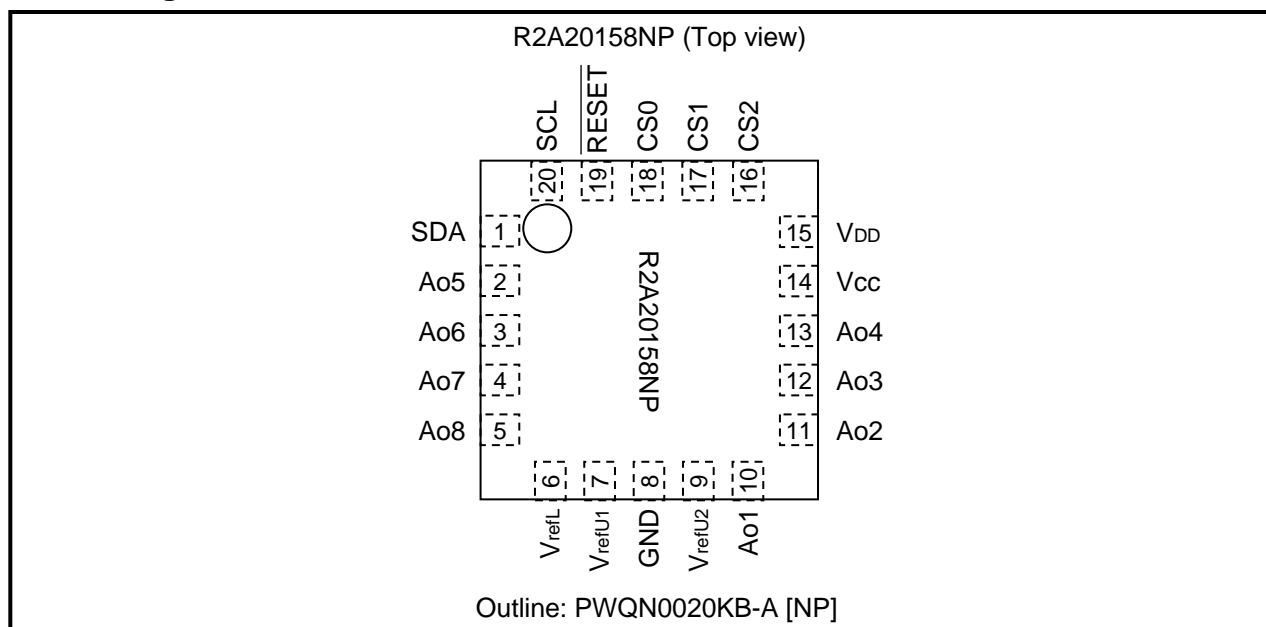
Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.

Blurring correction control or various control of the interchangeable lens of digital camera

## Block Diagram



## Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
1	SDA	Serial data input terminal
19	$\overline{\text{RESET}}$	Reset signal input terminal. A low state of $\overline{\text{RESET}}$ clear the all 8-bit latches.
20	SCL	Serial clock input terminal
10	Ao1	8-bit resolution D/A converter output terminal (After power on, analog output of every channel is set in DAC data "00h")
11	Ao2	
12	Ao3	
13	Ao4	
2	Ao5	
3	Ao6	
4	Ao7	
5	Ao8	
14	Vcc	Analog power supply terminal
15	VDD	Digital power supply terminal
8	GND	Analog and digital common GND
6	VrefL	D/A converter low level reference voltage input terminal
7	VrefU1	D/A converter high level reference voltage input terminal 1 (for ch5 to ch8)
9	VrefU2	D/A converter high level reference voltage input terminal 2 (for ch1 to ch4)
16	CS2	Chip select data input terminal 2 *1
17	CS1	Chip select data input terminal 1 *1
18	CS0	Chip select data input terminal 0 *1

\*1 : This IC can be accessed only when the slave address (A0 to A2) coincides with the chip select input (CS0 to CS2).

## Absolute Maximum Ratings

(Ta = 25 deg unless otherwise noted)

Item	Symbol	Conditions	Ratings	Unit
Analog Supply voltage	V <sub>CC</sub>		-0.3 to +6.5	V
Digital Supply voltage	V <sub>DD</sub>		-0.3 to < 6.5	V
Upper reference voltage of D/A *1	V <sub>refU1</sub> , V <sub>refU2</sub>		-0.3 to < 6.5	V
Digital input voltage	V <sub>IN D</sub>		-0.3 to V <sub>DD</sub> +0.3 ≤ 6.5	V
Buffer amplifier output current	I <sub>AO</sub>	Continuous	-2.0 to +2.0	mA
Power dissipation	P <sub>d</sub>	Ta = +85deg	290	mW
Thermal derating factor	K theta	Ta > +25deg	7.25	mW/deg
Operating temperature	T <sub>opr</sub>		-30 to +85	deg
Storage temperature	T <sub>stg</sub>		-40 to +125	deg

\*1 V<sub>DD</sub> ≥ V<sub>refU1</sub>, V<sub>refU2</sub>

## Electrical Characteristics

« Digital Part » (V<sub>CC</sub>, V<sub>DD</sub>, V<sub>refU1</sub>, V<sub>refU2</sub> = +5V +/-10%, V<sub>CC</sub> ≥ V<sub>refU1</sub>, V<sub>refU2</sub>, GND=V<sub>refL</sub>=0V, Ta=-30 to +85deg unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Supply voltage	V <sub>DD</sub>		2.7	5.0	5.5	V
Supply current	I <sub>DD</sub>	CLK = 500kHz operation, I <sub>AO</sub> = 0 μA	-	-	1.0	mA
Input leak current	I <sub>ILK</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-10	-	10	μA
Output low voltage (SDA)	V <sub>OL</sub>	I <sub>OL</sub> = 3 mA	-	-	0.4	V
Input low voltage	V <sub>IL</sub>		-	-	0.2V <sub>DD</sub>	V
Input high voltage	V <sub>IH</sub>		0.8V <sub>DD</sub>	-	-	V

« Analog Part » (V<sub>CC</sub>, V<sub>DD</sub>, V<sub>refU1</sub>, V<sub>refU2</sub> = +5V +/-10%, V<sub>CC</sub> ≥ V<sub>refU1</sub>, V<sub>refU2</sub>, GND=V<sub>refL</sub>=0V, Ta=-30 to +85deg unless otherwise noted)

Item	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Supply Voltage	V <sub>CC</sub>		2.7	-	5.5	V
Supply current	I <sub>CC</sub>	CLK=500kHz operation, I <sub>AO</sub> = 0μA	-	0.4	1.2	mA
D-A converter high level reference voltage input current	I <sub>refU1, 2</sub>	V <sub>tefU</sub> = 5V, V <sub>refL</sub> = 0V, Data condition: at maximum current for each terminal	-	0.6	1.2	mA
D-A converter high level reference voltage range *2	V <sub>refU1</sub> , V <sub>refU2</sub>		0.7V <sub>CC</sub>	-	V <sub>CC</sub>	V
D-A converter low level reference voltage range *2	V <sub>refL</sub>		GND	-	0.3V <sub>CC</sub>	V
Buffer amplifier output voltage range	V <sub>AO</sub>	I <sub>AO</sub> = +/- 100 μA	0.1	-	V <sub>CC</sub> -0.1	V
		I <sub>AO</sub> = +/- 500 μA	0.2	-	V <sub>CC</sub> -0.2	V
Buffer amplifier output current range	I <sub>AO</sub>	Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V	-1.0	-	1.0	mA
Differential nonlinearity error	S <sub>DL</sub>	V <sub>refU1</sub> , V <sub>refU2</sub> = 4.79V, V <sub>refL</sub> = 0.95V, V <sub>CC</sub> = 5.5V (15mV/LSB), Without load (I <sub>AO</sub> = 0μA)	-0.7	-	0.7	LSB
Nonlinearity error	S <sub>L</sub>		-1.0	-	1.0	LSB
Zero code error	S <sub>ZERO</sub>		-2.0	-	2.0	LSB
Full scale error	S <sub>FULL</sub>		-2.0	-	2.0	LSB
Output capacitive load	C <sub>O</sub>		-	-	0.1	μF
Buffer amplifier output impedance	R <sub>p</sub>		-	5.0	-	ohm

\*2 : The output does not necessary be the value with the reference voltage setting range.

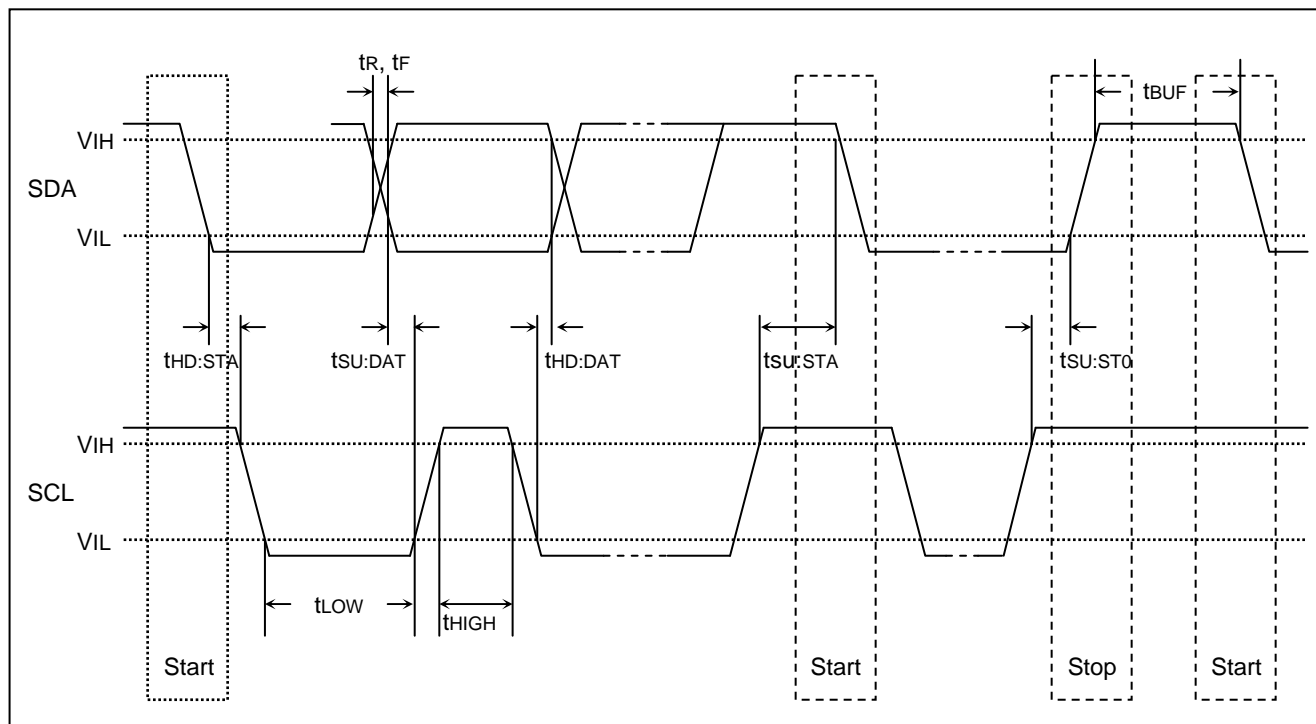
The output value is determined by the buffer amplifier output voltage range (V<sub>AO</sub>).V<sub>DD</sub> ≥ V<sub>refU1</sub>, V<sub>refU2</sub>

## I<sup>2</sup>C BUS Line Characteristics

Item	Symbol	STANDARD MODE		FAST MODE		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	fSCL	0	100	0	400	kHz
Free time: the bus must be free before a new transmission can start	tBUF	4.7	-	1.3	-	μs
Hold time START condition after this period, the first clock pulse is generated	tHD:STA	4.0	-	0.6	-	μs
Low period of the clock	tLOW	4.7	-	1.3	-	μs
High period of the clock	tHIGH	4.0	-	0.6	-	μs
Set-up time for START condition. Only relevant for a repeated START condition.	tsu:STA	4.7	-	0.6	-	μs
Data Hold time	tHD:DAT	0	3.45	0	0.9	μs
Data Set-up time	tsu:DAT	250	-	100	-	ns
Rise time of SDA and SCL signals	tR	-	1000	-	300	ns
Fall time of SDA and SCL signals	tF	-	300	-	300	ns
Set-up time for STOP condition	tsu:STO	4.0	-	0.6	-	μs
Capacitive load of bus line	Cb	-	400	-	400	pF

All of above value are corresponds to  $V_{IHmin}$  and  $V_{ILmax}$ .

## Timing Chart

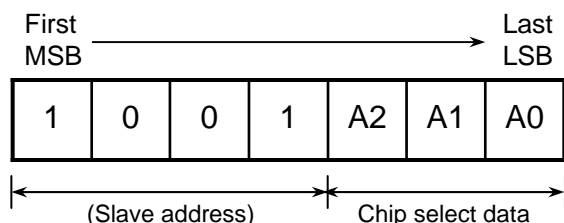


## I<sup>2</sup>C BUS Format

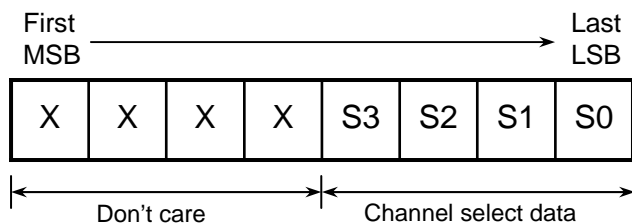
STA	Slave address	W	A	Sub address	A	DAC data	A	STP
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Note: STA: start condition, A: acknowledge bit, W: write (SDA=Low), STP: stop condition

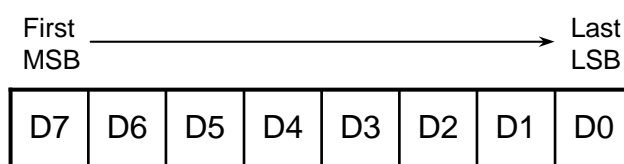
### • Slave address



### • Sub address



### • DAC data



### Chip select data

A2	A1	A0	CS2	CS1	CS0
0	0	0	L	L	L
0	0	1	L	L	H
0	1	0	L	H	L
:	:	:	:	:	:
1	1	1	H	H	H

(L=Low, H=High)

Note: This IC can be accessed only when the lower 3 bits data of slave address (A0 to A2) coincide with the input data of CS0 to CS2.

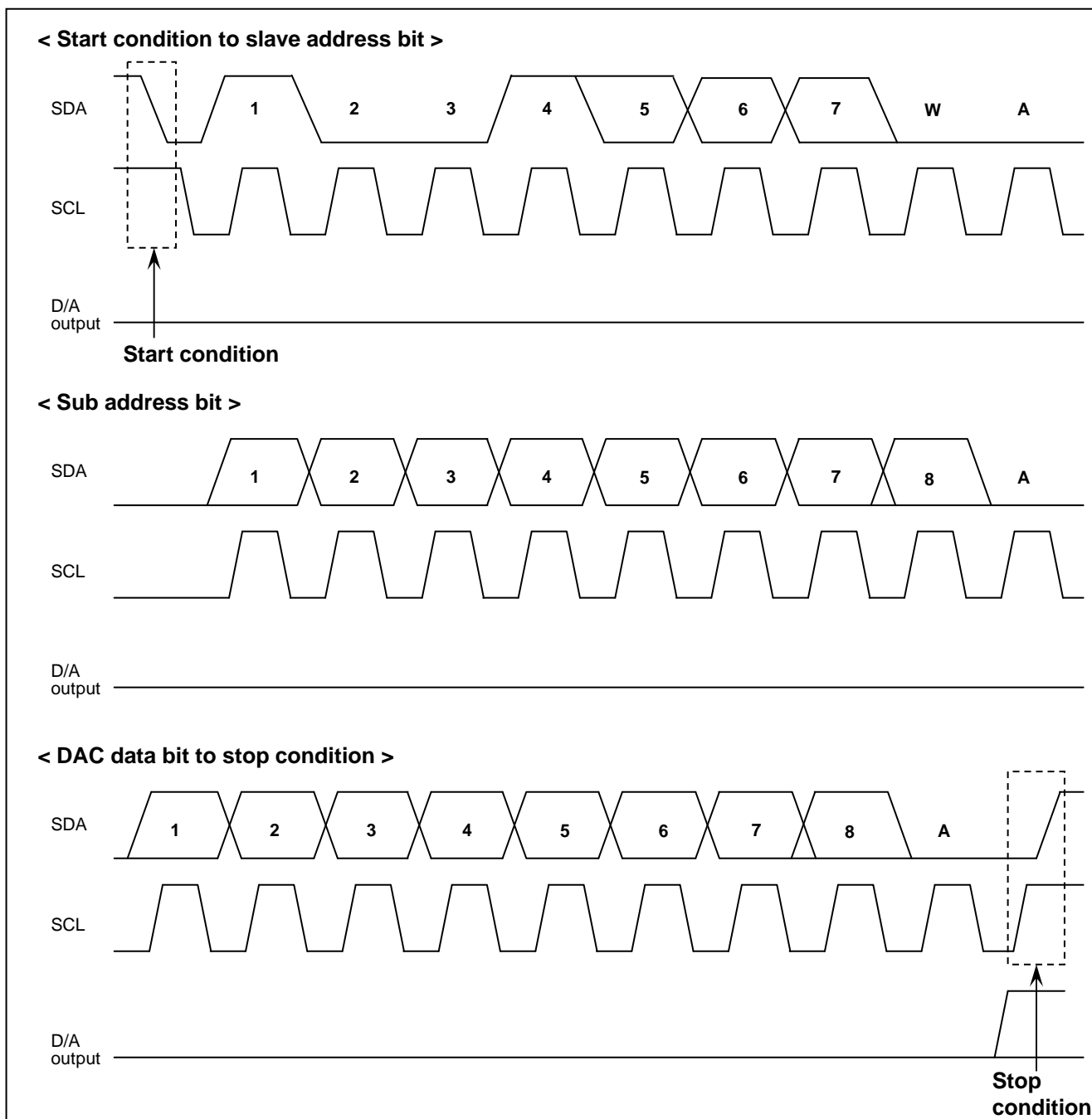
### Channel select data

S3	S2	S1	S0	Channel selection
0	0	0	0	Don't care
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
0	0	1	1	ch3 selection
0	1	0	0	ch4 selection
0	1	0	1	ch5 selection
0	1	1	0	ch6 selection
0	1	1	1	ch7 selection
1	0	0	0	ch8 selection
1	0	0	1	Don't care
:	:	:	:	:
1	1	1	1	Don't care

### DAC data

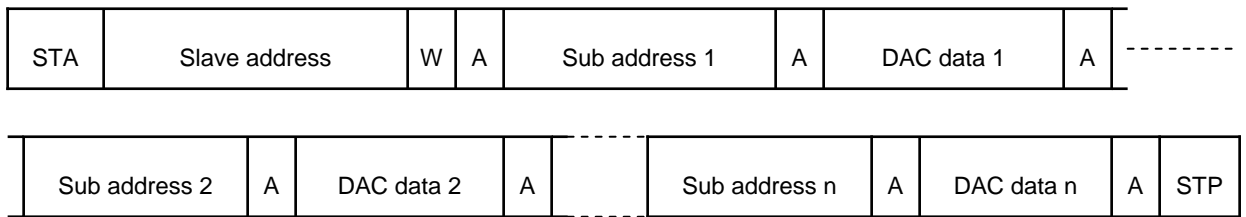
D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
0	0	0	0	0	0	0	1	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	0	0	0	0	0	1	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
0	0	0	0	0	0	1	1	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	$V_{refU}$

## Data Timing Chart SCL and SDA (Model)



- Start condition With SCL at High, SDA line goes from High to Low
- Stop condition With SCL at High, SDA line goes from Low to High  
( Under normal circumstance, SDA is changed when SCL is Low )
- Acknowledge bit The receiving IC has to pull down SDA line whenever receive slave data.  
( The transmitting IC releases the SDA line just then transmit 8-bit data. )

### Digital Data Format

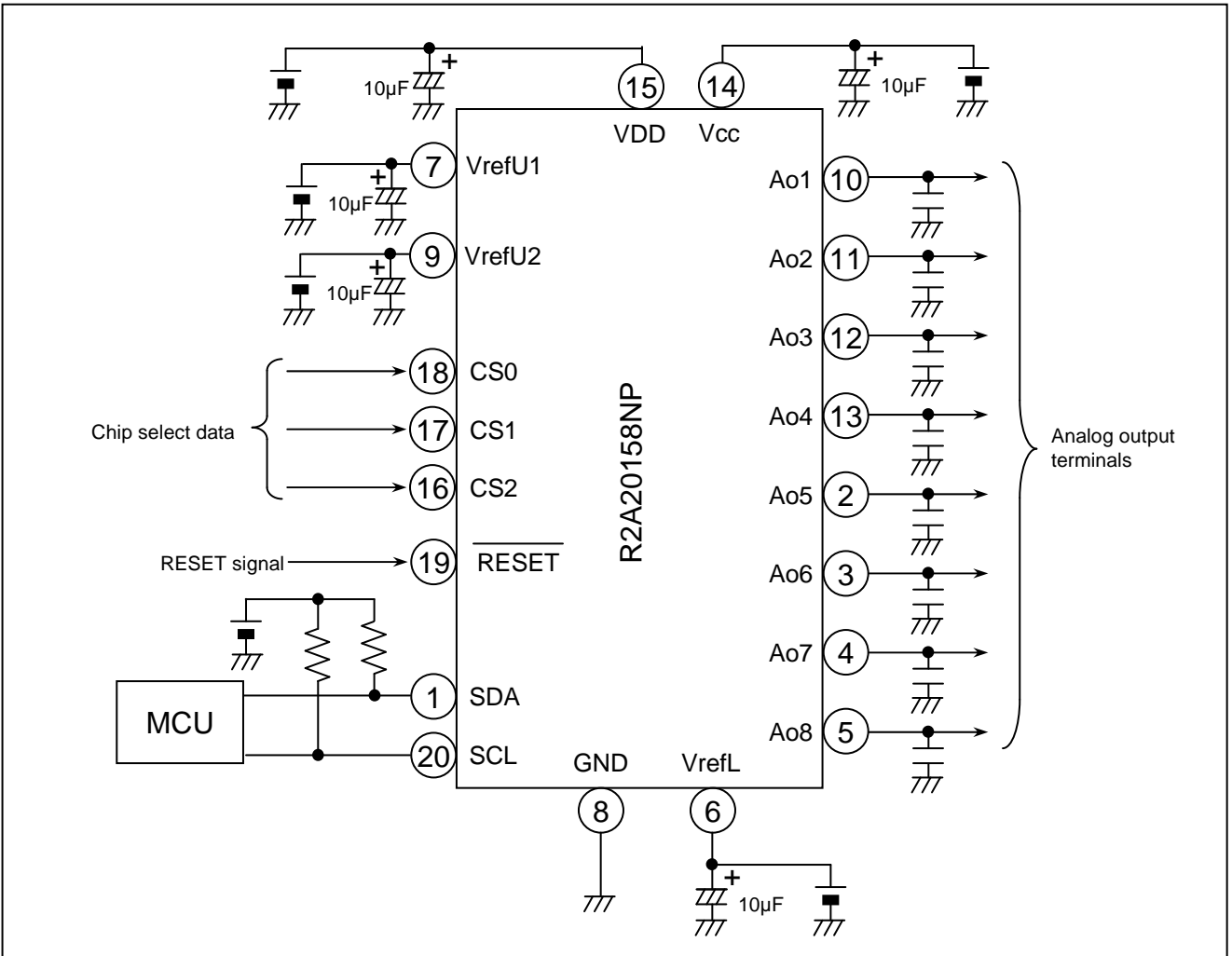


After the Start condition, the transmitting IC accesses the slave IC by Slave address, and transmits the data to each channel by two bites (Sub address and DAC data).

### Precaution For use

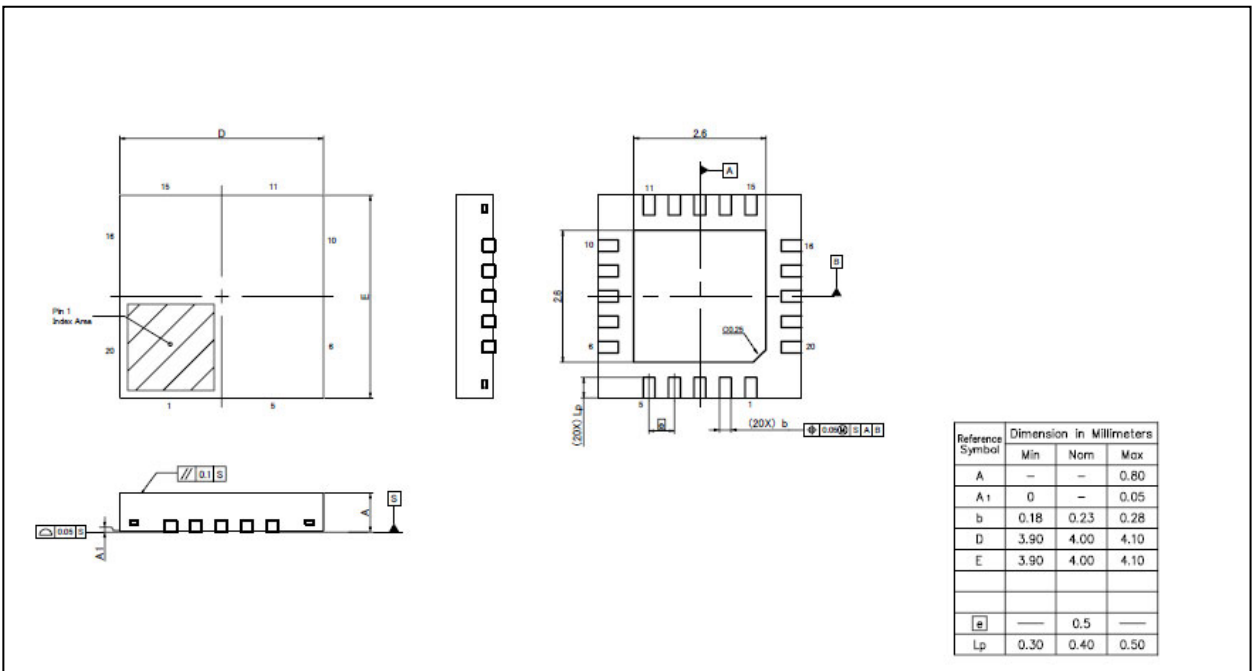
- If ripple or spike is input to D/A converter upper reference voltage terminal (VrefU1,2), accuracy of D/A converter is down, So, when use this device, please connect capacitor among Vcc to GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor ( 0.1  $\mu$ F Max ) among output to GND for every noise elimination.

### Application Example



## Package Dimensions

### PWQN0020KB-A [NP]



## Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20158NP	QFN-20	PWQN0020KB-A	NP	Embossed Taping/2,500 pcs.



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