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RF3933

90W GaN WIDE-BAND POWER AMPLIFIER

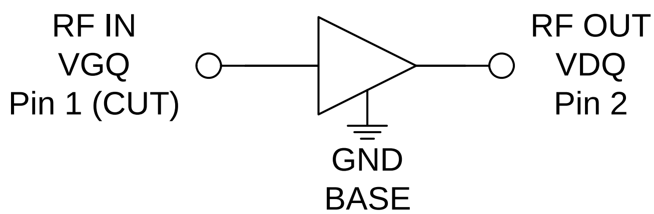
Package: Hermetic 2-Pin Flanged Ceramic

Features

- Broadband Operation DC to 3.5GHz
- Advanced GaN HEMT Technology
- Advanced Heat Sink Technology
- Small Signal Gain = 21dB at 0.9GHz
- 48V Operation Typical Performance:
  - Output Power 90W at P3dB
  - Drain Efficiency 75% at P3dB
  - -40°C to 85°C Operation

Applications

- Commercial Wireless Infrastructure
- Cellular and WiMAX Infrastructure
- Civilian and Military Radar
- General Purpose Broadband Amplifiers
- Public Mobile Radios
- Industrial, Scientific and Medical



Functional Block Diagram

Product Description

The RF3933 is a 48V, 90W high power discrete amplifier designed for commercial wireless infrastructure, cellular and WiMAX infrastructure, industrial/scientific/medical and general purpose broadband amplifier applications. Using an advanced high power density Gallium Nitride (GaN) semiconductor process, these high-performance amplifiers achieve high efficiency and flat gain over a broad frequency range in a single amplifier design. The RF3933 is an unmatched GaN transistor packaged in a hermetic, flanged ceramic package. This package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of simple, optimized matching networks external to the package that provide wideband gain and power performance in a single amplifier.

Ordering Information

RF3933S2	2-piece sample bag
RF3933SB	5-piece bag
RF3933SQ	25-piece bag
RF3933SR	100 pieces on 7” short reel
RF3933TR7	750 pieces on 7” reel
RF3933PCK-411	Fully assembled evaluation board optimized for 2.14GHz; 48V

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☑ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to +2	V
Gate Current (I_G)	54	mA
Operational Voltage	65	V
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_C)	-40 to +85	°C
Operating Junction Temperature (T_J)	200	°C
Human Body Model	Class 1A	
MTTF (T_J< 200 °C, 95% Confidence Limits)*	3 x 10^6	Hours
Thermal Resistance, R_{TH} (junction to case) measured at T_C = 85 °C, DC bias only	2.1	°C/W

* MTTF - median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values.

Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C)/R_{TH\ J\text{-}C}$ and $T_C = T_{CASE}$

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})	28		48	V	
Gate Voltage (V_{GSQ})	-4.5	-3.7	-2.5	V	
Drain Bias Current		300		mA	
Frequency of Operation	DC		3500	MHz	
Capacitance					
C_{RSS}		7		pF	V_G = -8V, V_D = 0V
C_{ISS}		30		pF	
C_{OSS}		21		pF	
DC Functional Test					
$I_{G\ (OFF)}$ – Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D\ (OFF)}$ – Drain Leakage			2.5	mA	V_G = -8V, V_D = 48V
$V_{GS\ (TH)}$ – Threshold Voltage		-4.2		V	V_D = 48V, I_D = 20mA
$V_{DS\ (ON)}$ – Drain Voltage at High Current		0.25		V	V_G = 0V, I_D = .5A
RF Functional Test					[1], [2]
$V_{GS\ (Q)}$		-3.4		V	V_D= 48V, I_D=300mA
Gain	10	12		dB	CW, P_{OUT} = 49.5dBm, f = 2140MHz
Drain Efficiency	55	60		%	CW, P_{OUT} = 49.5dBm, f = 2140MHz
Input Return Loss	-10	-12		dB	CW, P_{OUT} = 49.5dBm, f = 2140MHz

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Typical Performance					[1], [2]
Small Signal Gain		21		dB	CW, f = 900MHz
Small Signal Gain		13.5		dB	CW, f = 2140MHz
Output Power at P3dB		49.5		dBm	CW, f = 900MHz
Output Power at P3dB		49.5		dBm	CW, f = 2140MHz
Drain Efficiency at P3dB		75		%	CW, f = 900MHz
Drain Efficiency at P3dB		75		%	CW, f = 2140MHz

[1] Test Conditions: CW operation, V_{DSQ} = 48V, I_{DQ} = 300mA, T= 25 °C.
[2] Performance in a standard tuned test fixture.

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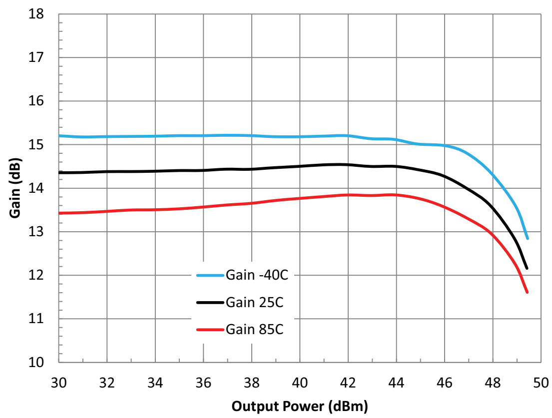
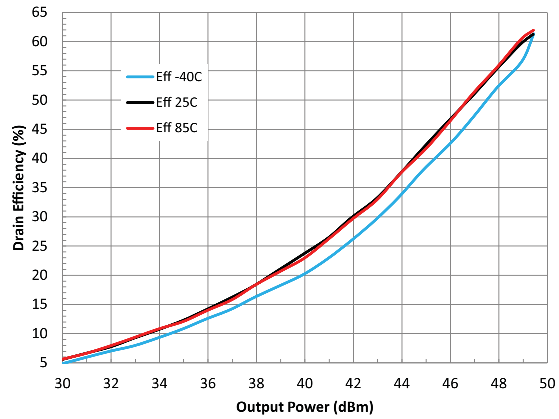
Typical Performance in Standard 2.14 GHz Tuned Test Fixture

(CW, T = 25 °C, unless otherwise noted)

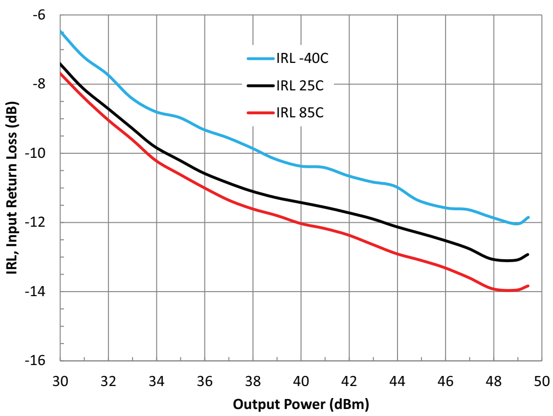
Gain vs. Output Power (f = 2140MHz)
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)



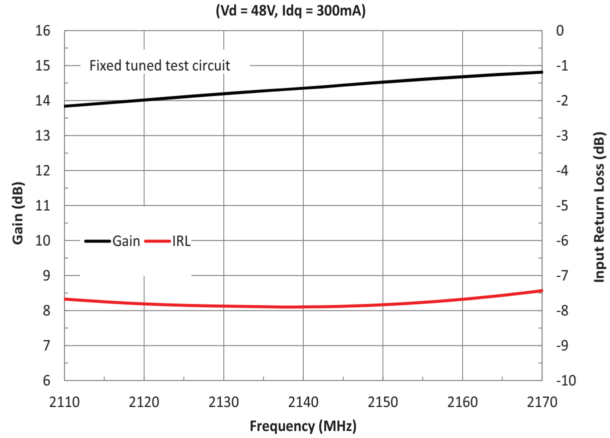
Efficiency vs. Output Power (f = 2140MHz)
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)



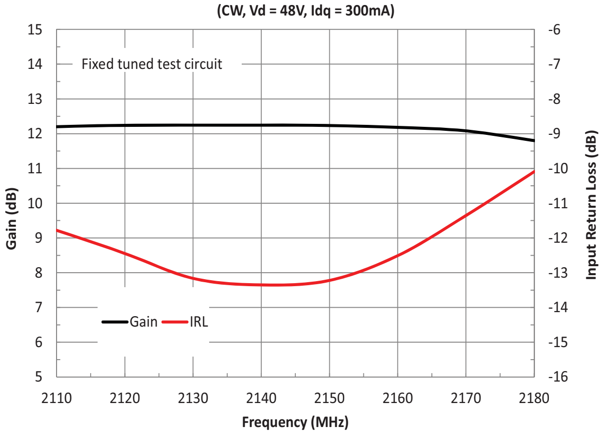
Input Return Loss vs. Output Power (f = 2140MHz)
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)



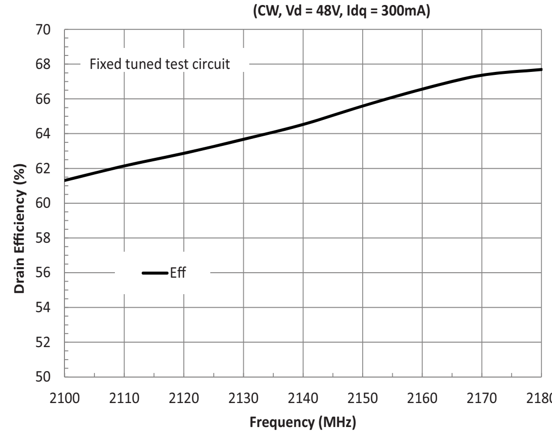
Small Signal Performance vs. Frequency, Pout = 30dBm
(Vd = 48V, Idq = 300mA)



Gain/IRL vs. Frequency, Pout = 49.5dBm
(CW, Vd = 48V, Idq = 300mA)



Drain Efficiency vs. Frequency, Pout = 49.5dBm
(CW, Vd = 48V, Idq = 300mA)



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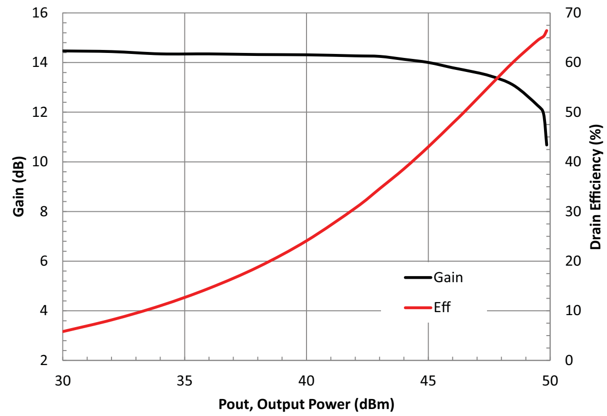
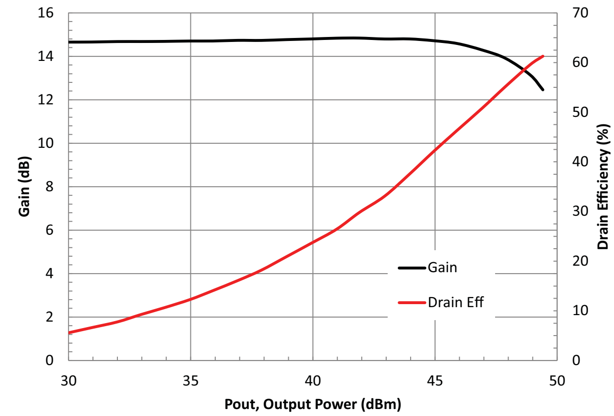
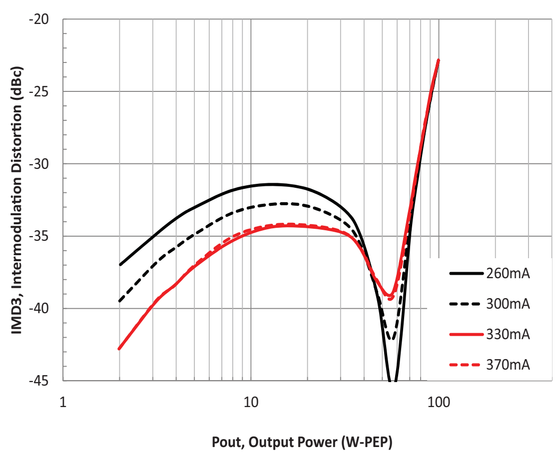
Gain/ Efficiency vs. Pout, f = 2140MHz
(CW, Vd = 48V, Idq = 300mA)



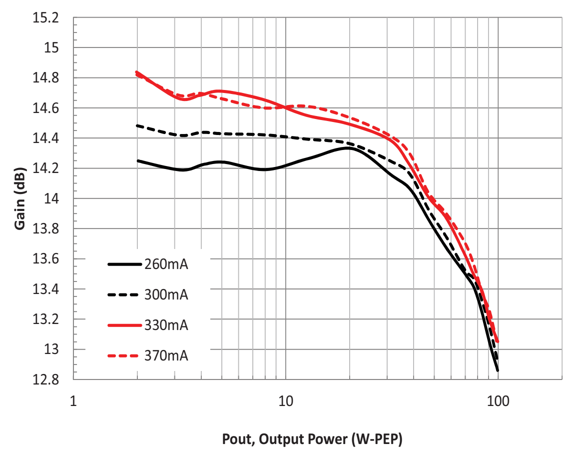
Gain/ Efficiency vs. Pout, f = 2140MHz
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)



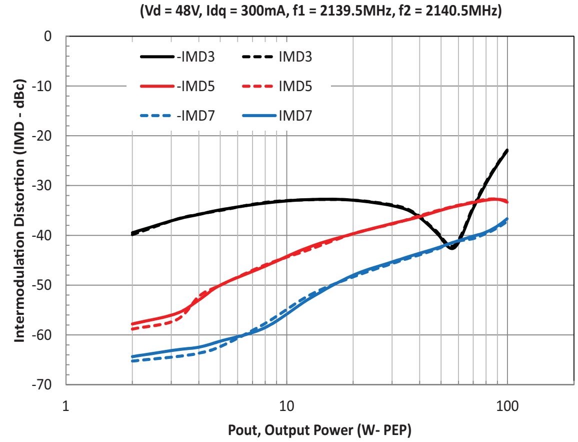
IMD3 vs. Pout
(2-Tone 1MHz Separation, Vd = 48V, Idq varied, fc = 2140MHz)



Gain vs. Pout
(2-Tone 1MHz Separation, Vd = 48V, Idq varied, fc = 2140MHz)



IMD vs. Output Power
(Vd = 48V, Idq = 300mA, f1 = 2139.5MHz, f2 = 2140.5MHz)



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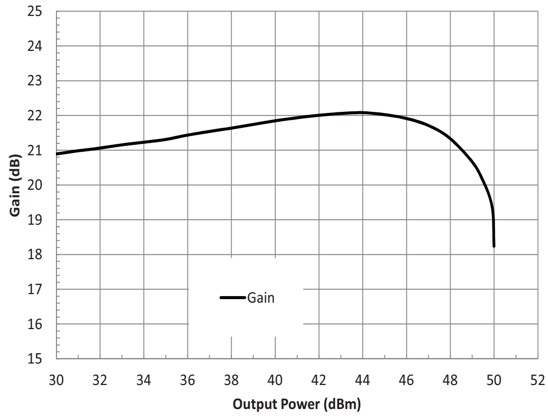
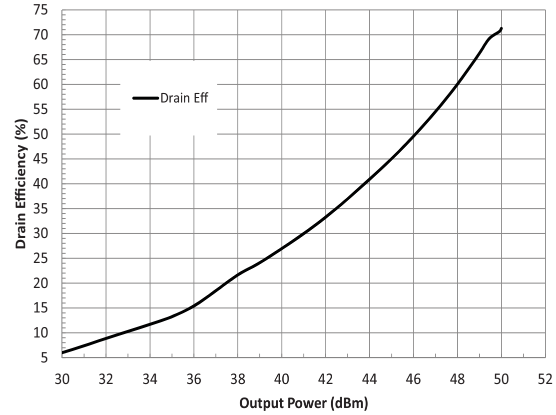
Typical Performance in Standard 900 MHz Tuned Test Fixture

(CW, T = 25 °C, unless otherwise noted)

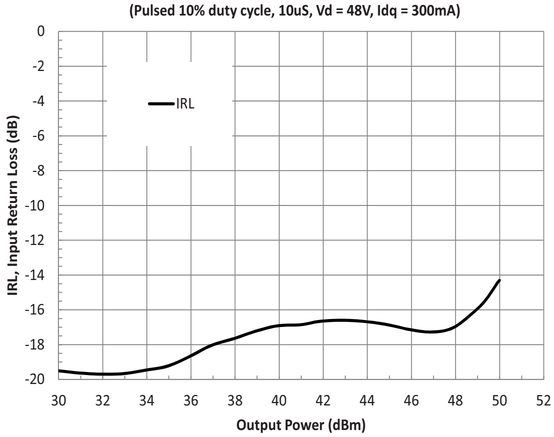
Gain vs. Output Power (f = 900MHz)
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)



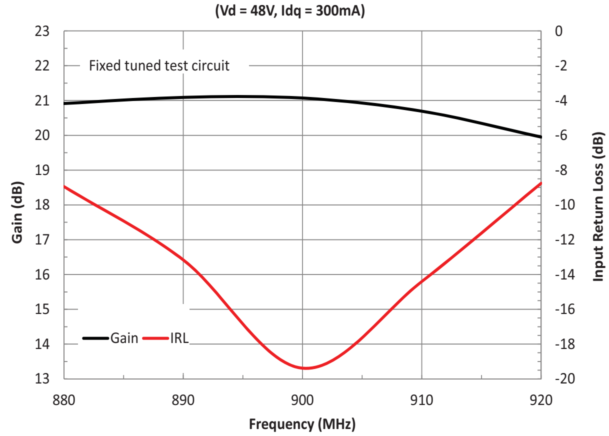
Efficiency vs. Output Power (f = 900MHz)
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)



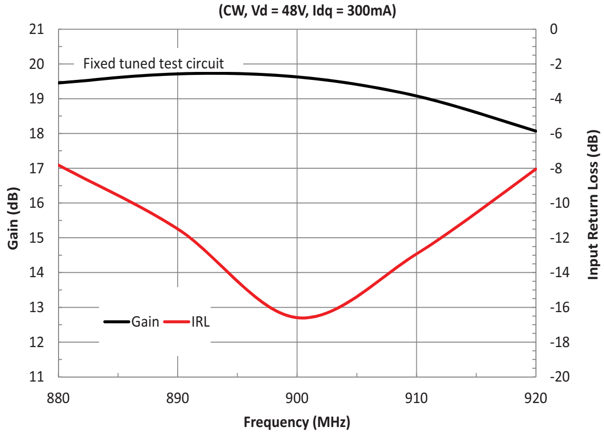
Input Return Loss vs. Output Power (f = 900MHz)
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)



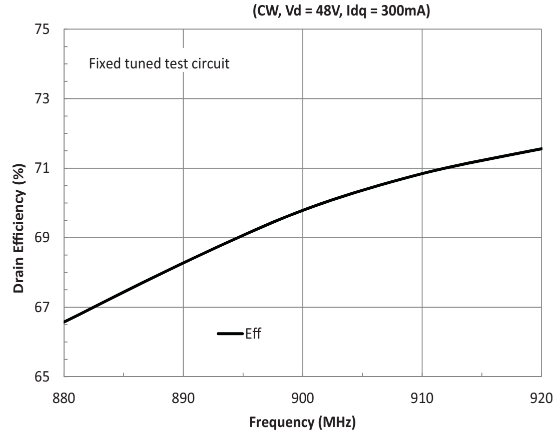
Small Signal Performance vs. Frequency, Pout = 30dBm
(Vd = 48V, Idq = 300mA)



Gain/IRL vs. Frequency, Pout = 49.5dBm
(CW, Vd = 48V, Idq = 300mA)



Drain Efficiency vs. Frequency, Pout = 49.5dBm
(CW, Vd = 48V, Idq = 300mA)



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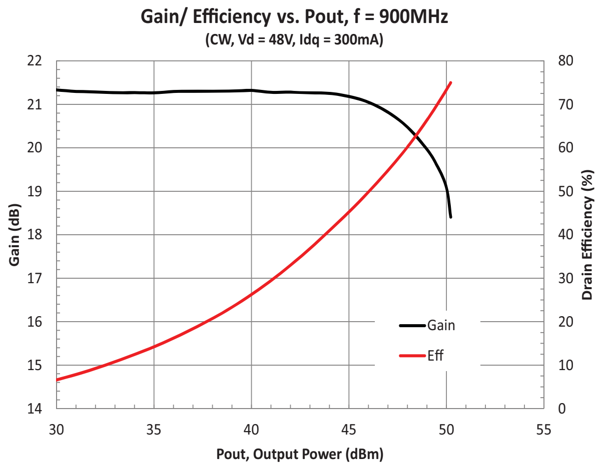
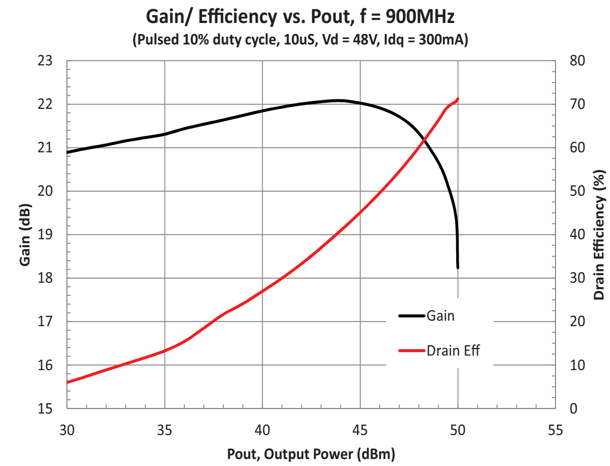
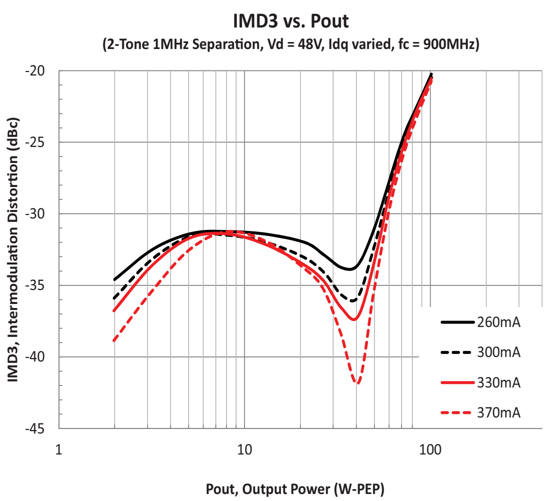
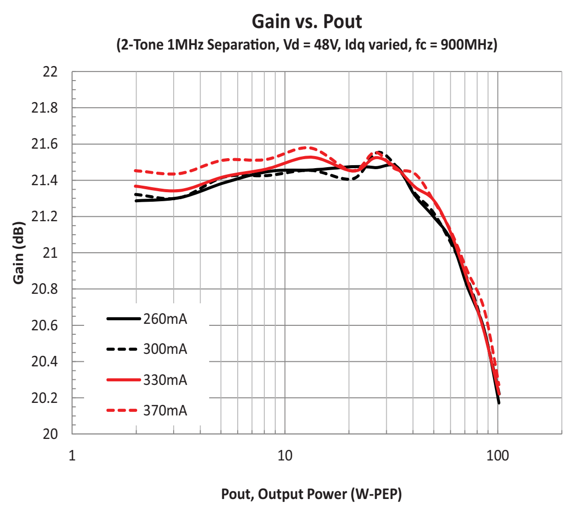
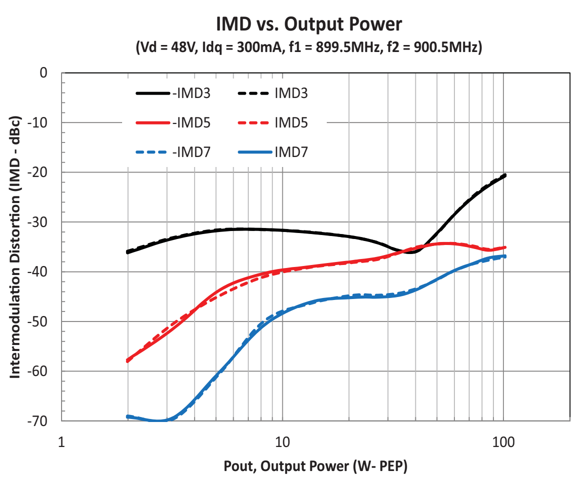

Gain/ Efficiency vs. Pout, f = 900MHz
(CW, Vd = 48V, Idq = 300mA)
Gain (dB)
Drain Efficiency (%)
Pout, Output Power (dBm)
Gain
Eff


Gain/ Efficiency vs. Pout, f = 900MHz
(Pulsed 10% duty cycle, 10uS, Vd = 48V, Idq = 300mA)
Gain (dB)
Drain Efficiency (%)
Pout, Output Power (dBm)
Gain
Drain Eff


IMD3 vs. Pout
(2-Tone 1MHz Separation, Vd = 48V, Idq varied, fc = 900MHz)
IMD3, Intermodulation Distortion (dBc)
Pout, Output Power (W-PEP)
260mA
300mA
330mA
370mA


Gain vs. Pout
(2-Tone 1MHz Separation, Vd = 48V, Idq varied, fc = 900MHz)
Gain (dB)
Pout, Output Power (W-PEP)
260mA
300mA
330mA
370mA


IMD vs. Output Power
(Vd = 48V, Idq = 300mA, f1 = 899.5MHz, f2 = 900.5MHz)
Intermodulation Distortion (IMD - dBc)
Pout, Output Power (W- PEP)
-IMD3
IMD3
-IMD5
IMD5
-IMD7
IMD7

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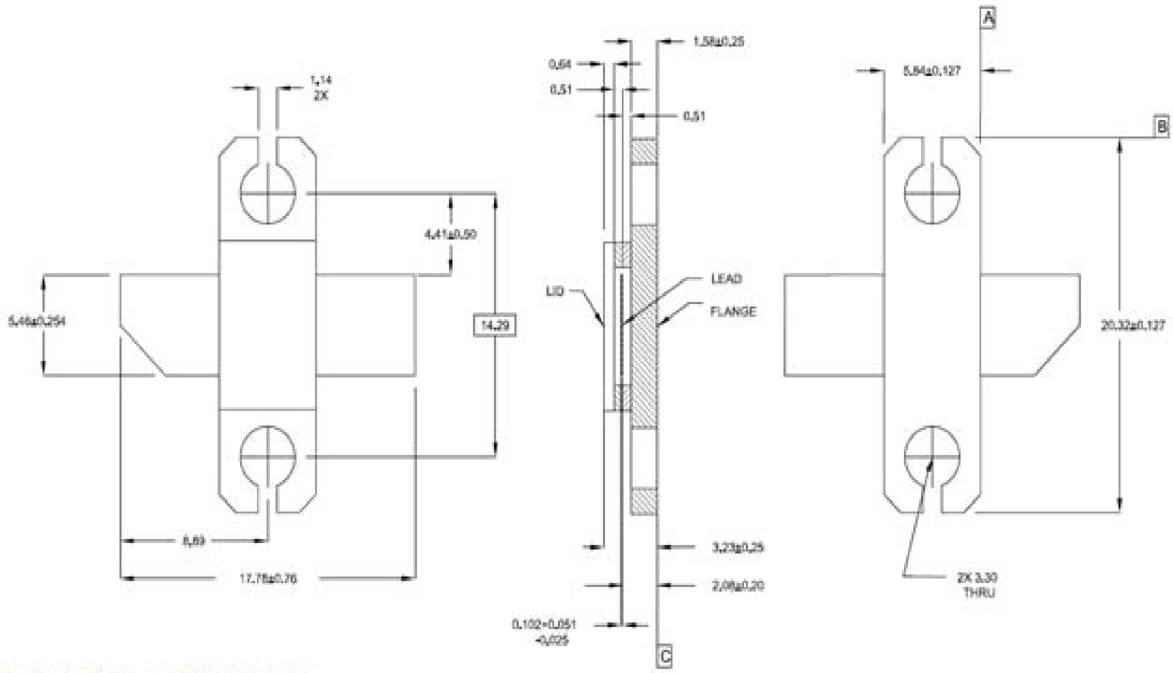
Package Drawing



Package Style: Flanged Ceramic

Pin-Out Table

Pin	Function	Description
1	Gate	Gate - VG RF Output
2	Drain	Drain - VD RF Output
3	Source	Source - Ground Base

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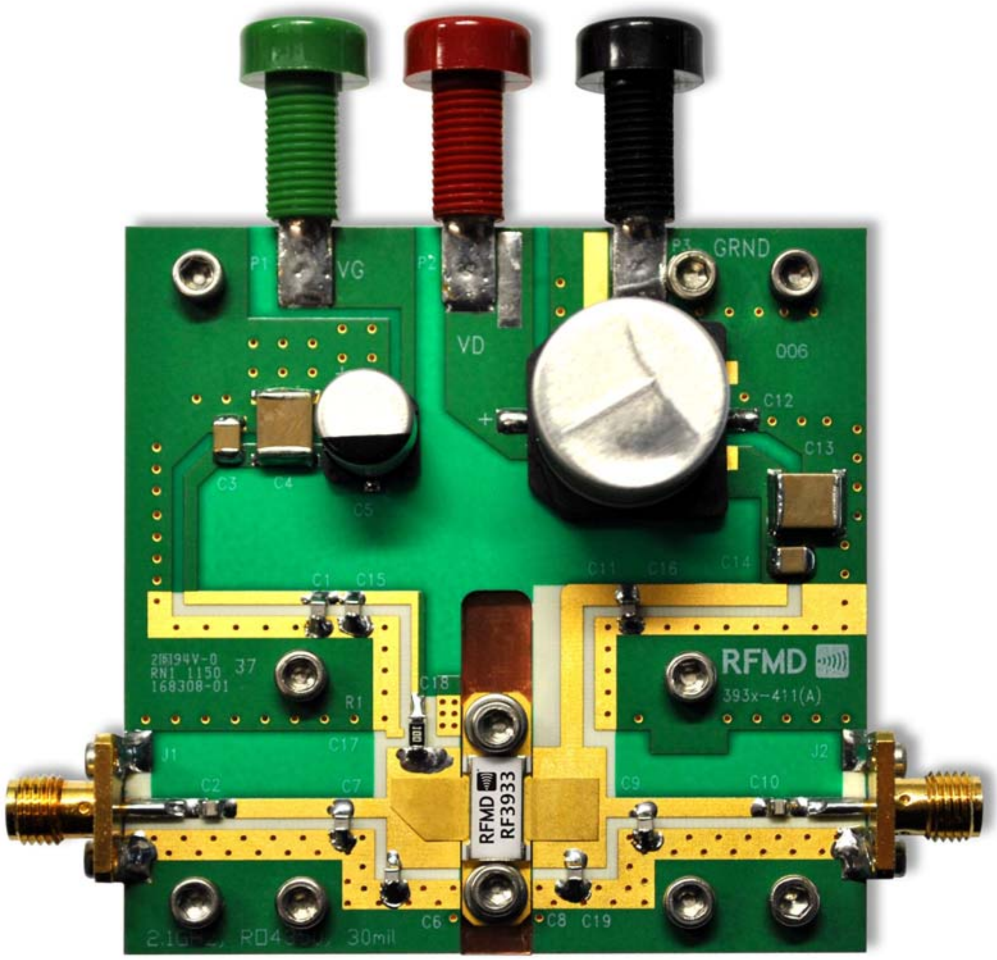
Bias Instruction for RF3933 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
Evaluation board requires additional external fan cooling.
Connect all supplies before powering up the evaluation board.

1. Connect RF cables at RF_{IN} and RF_{OUT}.
2. Connect ground to the ground supply terminal, and ensure that both the V_G and V_D grounds are also connected to this ground supply terminal.
3. Apply -8V to V_G.
4. Apply 48V to V_D.
5. Increase V_G until drain current reaches 300mA or desired bias point.
6. Turn on the RF input.



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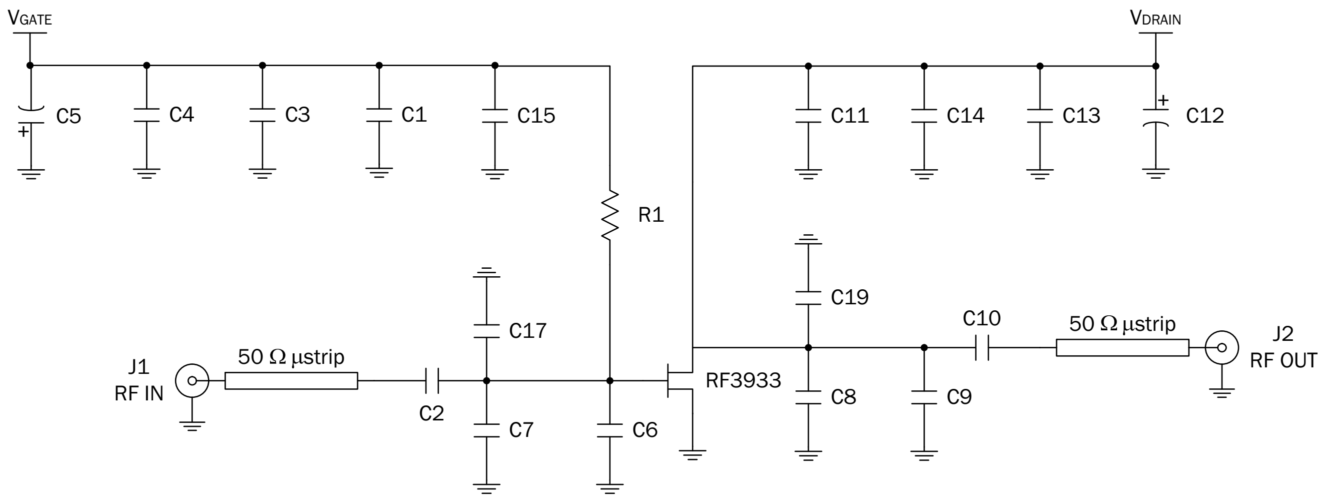
2.14GHz Evaluation Board Schematic



2.14GHz Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part Number
C1	10pF	ATC	ATC800A100JT
C2, C10, C11, C15	33pF	ATC	ATC800A330JT
C3,C14	0.1µF	Murata	GRM32NR72A104KA01L
C4,C13	4.7µF	Murata	GRM55ER72A475KA01L
C5	100µF	Panasonic	ECE-V1HA101UP
C6	1.5pF	ATC	ATC800A1R5BT
C7, C8	0.5pF	ATC	ATC800A0R5BT
C9	2.7pF	ATC	ATC800A2R7BT
C12	100µF	Panasonic	EEV-TG2A101M
C17	1.8pF	ATC	ATC800A1R8BT
C19	1.0pF	ATC	ATC800A1R0BT
R1	10Ω	Panasonic	ERJ-8GEYJ100V
C16, C18	Not used	-	-
PCB	RO4350, 0.030" thick dielectric	Rogers	-

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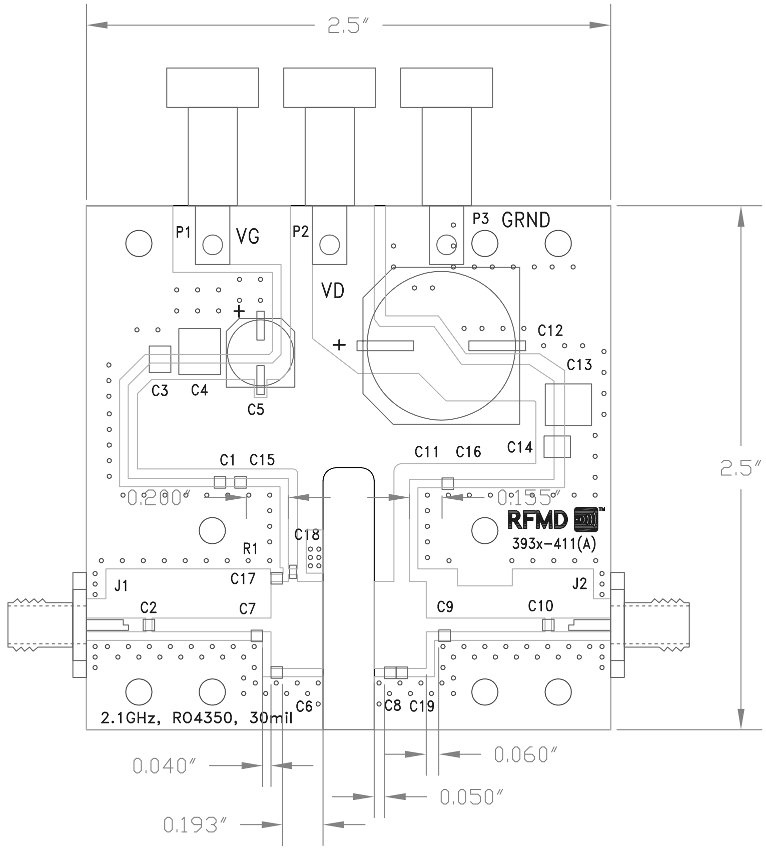
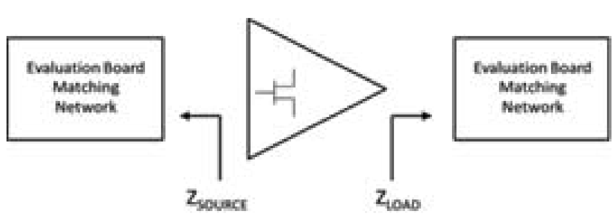
2.14GHz Evaluation Board Layout



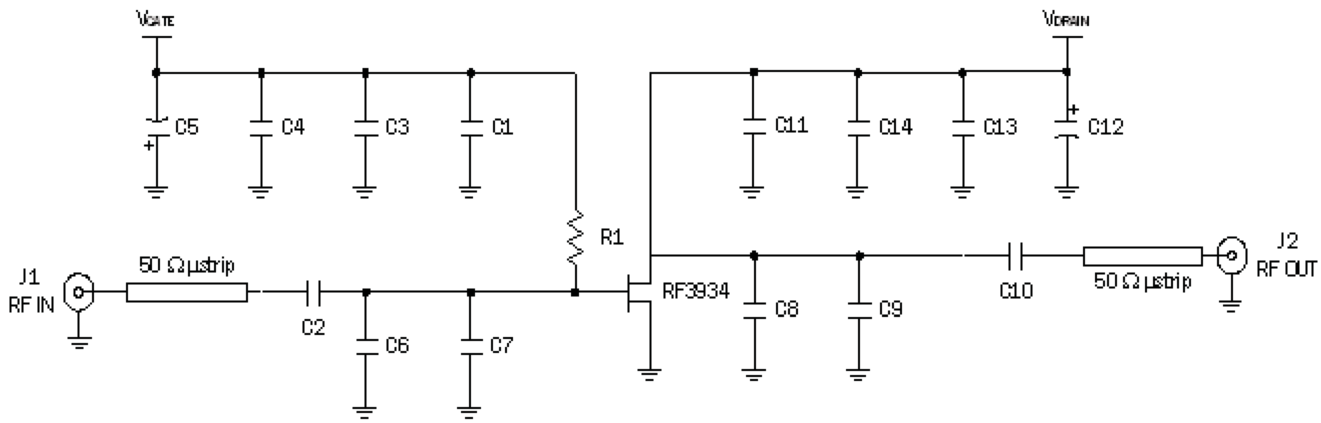
Device Impedances

Frequency	Z Source (Ω)	Z Load (Ω)
2110MHz	2.05 - j3.67	4.8 - j0.08
2140MHz	1.92 - j3.44	4.82 + j0.45
2170MHz	1.88 - j3.11	4.83 + j1.05

Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linear performance across the entire frequency bandwidth.



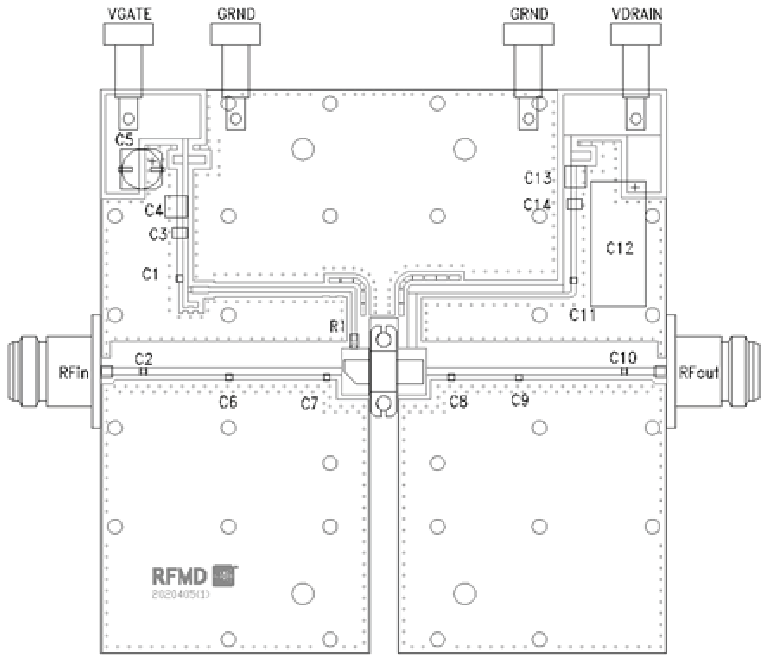
900MHz Evaluation Board Schematic



900MHz Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part Number
C1, C2, C10, C11	68pF	ATC	ATC800A680JT
C3, C14	0.1µF	Murata	GRM32NR72A104KA01L
C4, C13	4.7µF	Murata	GRM55ER72A475KA01L
C6	6.8pF	ATC	ATC800A6R8JT
C7	18pF	ATC	ATC800A180JT
C8	12pF	ATC	ATC800A120JT
C9	4.7pF	ATC	ATC800A4R7BT
C12	330µF	Panasonic	EEU-FC2A331
C5	100µF	Panasonic	ECE-V1HA101UP
R1	10Ω	Panasonic	ERJ-8GEYJ100V

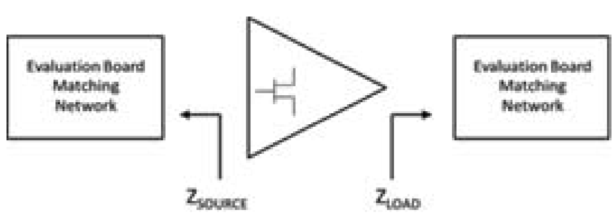
900 MHz Evaluation Board Layout



Device Impedances

Frequency	Z Source (Ω)	Z Load (Ω)
880 MHz	2.05 + j4.09	6.82 + j6.34
900 MHz	2.12 + j4.15	7.18 + j5.82
920 MHz	1.95 + j3.92	6.93 + j5.42

Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linear performance across the entire frequency bandwidth.



Device Handling/Environmental Conditions

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

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