

STRUCTURE Silicon monolithic integrated circuits

PRODUCT SERIES 2-in-1 motor driver for VTR

TYPE BD6903EFV

FUNCTION • VTR cylinder motor driver (Sensorless 3-phase full-wave soft switching drive system)

VTR loading motor driver

OAbsolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
	VCC	7	V
Supply voltage	VM	15	V
	VG	20	V
Power dissipation	Pd	1000 ^{**1}	mW
Operating temperature range	Topr	-20 ~ +75	°C
Storage temperature range	Tstg	-55 ~ +150	°C
Maximum output current (cylinder block)	lomax1	800 ^{%2}	mA
Maximum output current (loading block)	lomax2	1000 ^{**2}	mA
Junction temperature	Tjmax	+150	°C

 $^{^{**1}}$ 70mm × 70mm × 1.6mm glass epoxy board. Derating in done at 8.0mW/°C for operating above Ta=25°C.

ORecommended operating conditions (Ta= -25~+75°C)

Parameter	Symbol	Min	Тур	Max	Unit
	VCC	4.5	5	5.5	V
Supply voltage	VM	9	12	13.5	V
	VG	VM+3	17	19	V
UIN, VIN, WIN in-phase input voltage range	VBEMFD	0	-	VM	V
PG amp in-phase input voltage range	VPD	1.5	-	3.0	V

This product described in this specification isn't judged whether it applies to COCOM regulations.

Please confirm in case of export.

This product isn't designed for protection against radioactive rays.

^{**2} Do not, however exceed Pd, ASO and Tjmax=150°C.



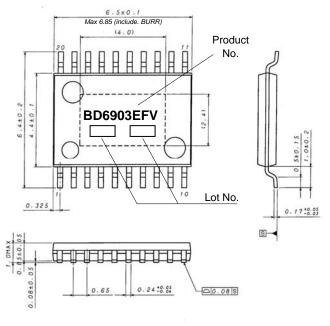
OElectrical characteristics (Unless otherwise specified, Ta=25°C, VCC=5V, VM =12V, VG=17V)

Doromotor	Cymhal		Limit		Unit	Conditions
Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Overall						
VCC total supply current	ICC	-	9.2	14.2	mA	
VM total supply current 1	IM1	-	1.4	2.8	mA	LIN=H or L
VM total supply current 2	IM2	-	1.4	2.8	mA	LIN=M
Output				1		
High-side output saturation voltage	VOH	-	0.4	0.8	V	Io=-400mA
Low-side output saturation voltage	VOL	-	0.3	0.6	V	Io=400mA
Torque reference						
EC input bias current	IEC	-	0.5	2	μΑ	
Torque reference start voltage	VECR	2.35	2.5	2.65	V	
Torque reference I/O gain	Gio	0.72	0.99	1.28	A/V	EC=2.6V-2.7V
Torque reference I/O gain	Gio	0.72	0.99	1.20	AVV	Gain output (HLM) RRNF = 0.5
Soft switch				1		
CT1, CT2 charge current	ICTD	-50	-35	-25	μΑ	
CT1, CT2 discharge current	ICTI	27	40	56	μΑ	
High CT1, CT2 clamp voltage	VCTH	4.4	4.7	-	V	
Low CT1, CT2 clamp voltage	VCTL	0.8	1.0	1.3	V	
Startup control logic						
CST charge current	ICSTD	-20	-14	-6	μΑ	
CST discharge current	ICSTI	2	6	10	μΑ	
High CST clamp voltage	VCSTH	2.4	2.8	3.3	V	
Low CST clamp voltage	VCSTL	0.8	1.0	1.3	V	
PG amp						
Input bias current	IPG-	-	0.1	0.25	μΑ	PG-=GND
DC bias voltage	VPG	2.25	2.5	2.75	V	PG-=PGOUT
Voltage gain 1	AV1	17.5	18.8	-	dB	f=1KHz
High output voltage	VOHP	3.4	3.75		V	IOH=-1mA
Low output voltage	VOLP	-	1.2	1.6	V	IOL=1mA
HYS amp						
Hysteresis width	VHYSP	-75	-100	-125	mV	
PFGpin						
High output voltage	VPFGP	4.5	-	-	V	IO=-10 μ A
Middle output voltage	VPFGM	2.25	-	2.75	V	IO=±10 μ A
Low output voltage	VPFGL	-	-	0.5	V	IO=10 μ A
Loading						
High-level LIN input	VLINH	3.5	-	-	V	Loading: Forward rotation
Middle-level LIN input	VLINM	2.35	-	2.65	V	Loading: Brake
Low-level LIN input	VLINL	-	-	1.5	V	Loading: Reverse rotation
LIN bias voltage	VLINB	2.35	2.5	2.65	V	
						IO=200mA,
Output saturation voltage	VCE	-	0.3	0.6	V	total of output transistor high-sid
				and low-side voltage		

 $[\]mbox{\%}$ Source currents are treated as negative while sinking currents are treated as positive.

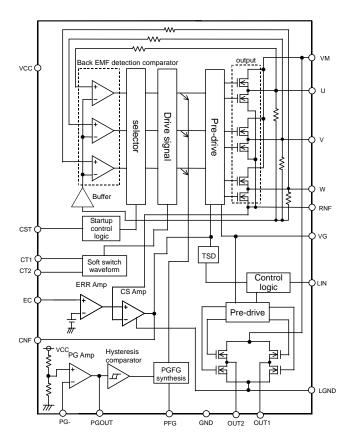


OPackage outline



HTSSOP-B20 (Unit:mm)

OBlock diagram



OPin No. / Pin name

Pin No.	Pin name
1	GND
2	LIN
3	EC
4	CT1
5	CT2
6	CST
7	CNF
8	PGOUT
9	PG-
10	VCC
11	W
12	V
13	RNF
14	U
15	VG
16	VM
17	OUT1
18	OUT2
19	LGND
20	PFG



OOperation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
170	20

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

Notes

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