

## SPICE Device Model Si7913DN Vishay Siliconix

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## **Dual P-Channel 20-V (D-S) MOSFET**

#### **CHARACTERISTICS**

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

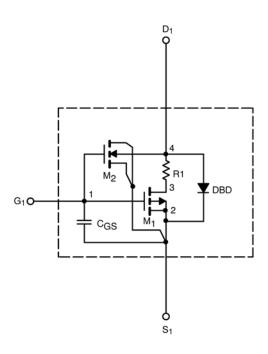
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

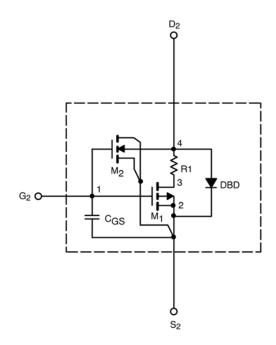
#### **DESCRIPTION**

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to  $125^{\circ}$ C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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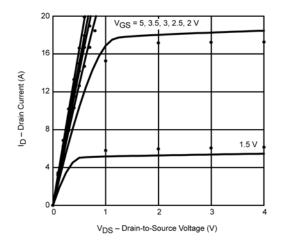
SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static	•		-	<del>-</del>	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	0.81		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	126		Α
Drain-Source On-State Resistance <sup>a</sup>	Γ <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, I_D = -7.4 \text{ A}$	0.031	0.029	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -6.5 \text{ A}$	0.038	0.038	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -1.5 A	0.048	0.051	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = -6 \text{ A}, I_{D} = -7.4 \text{ A}$	22	20	S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{\rm S}$ = -2.3 A, $V_{\rm GS}$ = 0 V	-0.82	-0.74	V
Dynamic <sup>b</sup>			-		
Total Gate Charge	$Q_g$	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -7.4 \text{ A}$	13	15.3	nC
Gate-Source Charge	$Q_{gs}$		2	2	
Gate-Drain Charge	$Q_{gd}$		3.9	3.9	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD} = -10 \text{ V, } R_L = 10 \Omega$ $I_D \cong -1 \text{ A, } V_{GEN} = -4.5 \text{ V, } R_G = 6 \Omega$	31	20	ns
Rise Time	t <sub>r</sub>		27	70	
Turn-Off Delay Time	$t_{d(off)}$		124	72	
Fall Time	t <sub>f</sub>		21	150	

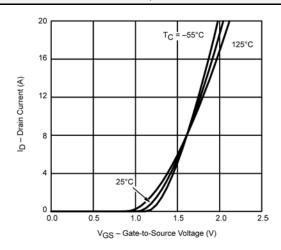
a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2%. b. Guaranteed by design, not subject to production testing.

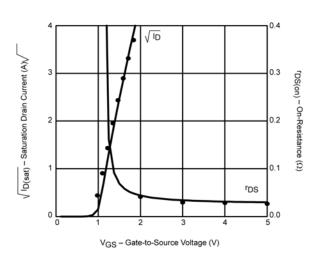


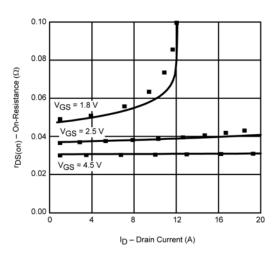
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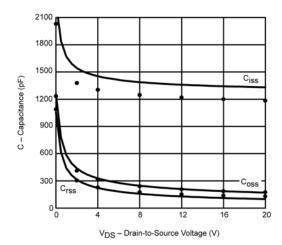
#### COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

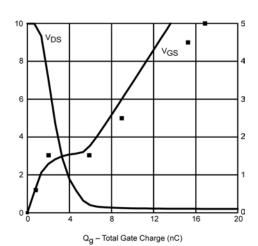












Note: Dots and squares represent measured data.



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