NCS5650

2 Amp PLC Line Driver

The NCS5650 is a high efficiency, Class A/B, low distortion power line driver. Its design is optimized to accept a signal from a Power Line Carrier modem. The output stage is designed to drive up to 2 A peak into an isolation transformer or simple coil coupling to the mains. At output current of 1.5 A, the output voltage is guaranteed to swing within 1 V or less of either rail giving the user improved SNR. Power supply options are single−sided 6 V to 12 V and dual balanced ±3.0 V to ±6.0 V. The input stage contains an operational amplifier which can be configured as a unity gain follower buffer or used to provide the first stage of a 4−pole low pass filter. In addition the NCS5650 offers a current limit programmable with a single resistor, R_{-Limit}, together with a current limit flag.

The device provides two independent thermal flags with hysteresis: a thermal warning flag to let the user know the internal junction temperature has reached a user programmable thermal warning threshold and a thermal error flag that indicates the internal junction temperature has exceeded 150°C. In shutdown mode the NCS5650 output goes into a high−impedance state. The NCS5650 comes in a 20 lead QFN package (4x4x1mm) with an exposed thermal pad for enhanced thermal reliability.

Features

- Rail−to−Rail Drop of Only ±1 V with I_{out} = 1.5 A
- V_{CC}: Single−Sided (6 V to 12 V) or Dual−Balanced ±6.0 V
- Flexible 4th−Order Filtering
- Current−Limit Set with One Resistor
- Diagnostic Flags Level Shifted to V_µc to Simplify Interface with External MCU
  - Thermal Warning Flag with Flexible Threshold Setting
  - Thermal Error flag and Shutdown
  - Overcurrent Flag
- Enable/Shutdown Control
- Extended Junction Temperature Range: −40°C to +125°C
- Small Package: 20−pin 4x4x1mm QFN with Exposed Thermal Pad
- Optimized for Operation in the Cenelec A to D Frequency Band
- This is a Pb−Free Device

Typical Applications

- Power Line Communication Driver in AMM and AMR Metering Systems
- Valve, Actuator, and Motor Driver
- Audio

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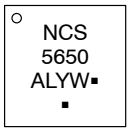
1 20

QFN20
CASE 485E

MARKING DIAGRAM



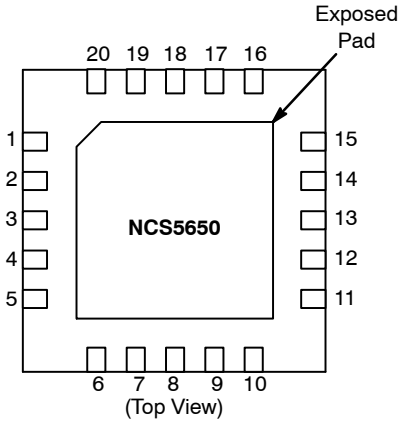
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
NCS5650MNTXG	QFN20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part or orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



NOTE: The Exposed Pad (EP) on package bottom must be attached to a heat−sinking conduit. The Exposed Pad must be electrically connected to V_{EE}.

Figure 1. Pin Connections

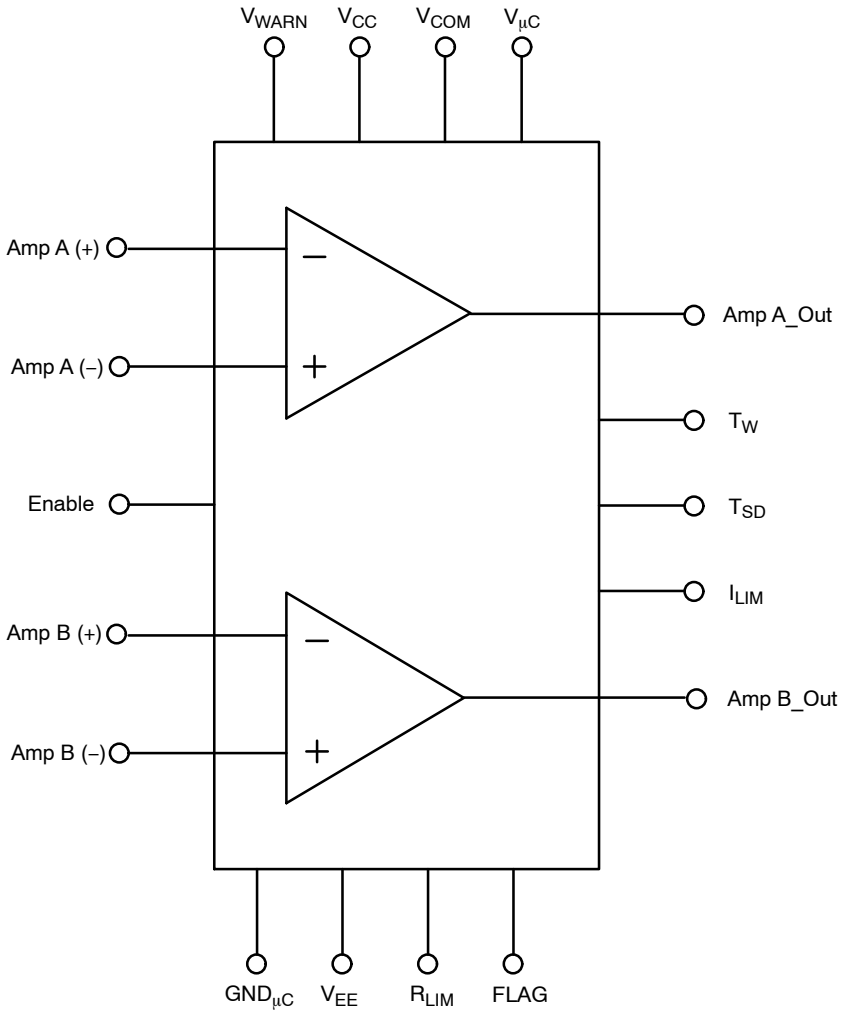


Figure 2. NCS5650 Block Diagram

PIN DESCRIPTION

Pin#	Symbol	Pin Function
1	Enable	Enable/ Shutdown Input (Low = Enable)
2	V_{com}	Virtual Common at (V_{CC} – V_{EE})/2 (See Note 1 Below)
3	Amp A (+)	Positive (+) Input of Op Amp A
4	Amp A (–)	Negative (–) Input of Op Amp A
5	Amp A Out	Output of Op Amp A
6	V_{CC}	Positive supply for amplifiers
7	V_{CC}	Positive supply for amplifiers
8	Amp B Out	Output of Op Amp B
9	Amp B Out	Output of Op Amp B
10	V_{EE}	Negative supply for amplifiers
11	V_{EE}	Negative supply for amplifiers
12	Amp B (–)	Negative (–) Input of Op Amp B
13	Amp B (+)	Positive (+) Input of Op Amp B
14	V–Warn	Thermal Warming Temp is set by a voltage determined by the ratio of two resistors (see Figure 6).
15	R–Limit	Output B Current Limit Set Resistor (R–Limit) to Pin 10
16	I_{LIM} flag	Current Limit Flag (High indicates Output Current ≥ limit set by R–Limit)
17	TSD flag	Thermal Shutdown Flag (High indicates Junction Temperature ≥ 150°C)
18	TW flag	Thermal Warning Flag (High indicates Junction Temperature ≥ threshold set by V–Warn)
19	V_μc	Digital supply for logic flag thresholds
20	GND_μc	Digital ground for logic flag thresholds
21	Exposed Pad	The exposed pad should be connected to the lowest voltage potential in the circuit.

1. The principal purpose of pin 2 is to facilitate the implementation of the 4th–order lowpass filter when operating on single–sided supply by providing a virtual common at mid–supply. When operating on dual balanced supplies, Pin 2 must be left floating and the external common of the dual supplies should be used for the filter implementation.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_S	Supply Voltage (V_{CC} to V_{EE})	13.2	V
V_{ICR}	Input Common Mode Voltage Range	(V_{EE} – 0.3V, V_{CC} + 0.3V)	V
T_J	Maximum Junction Temperature (Operating Range –40°C to 125°C)	160	°C
T_{stg}	Storage Temperature	–65 to 150	°C
	Mounting Temperature (Infrared or Convection – 30 sec)	260	
MSL	Moisture Sensitivity Level	Level 1	
θ_{JA}	Thermal Resistance 20–Pin QFN with Exposed Thermal Pad (With exposed thermal pad soldered to 9 in^2 of 2 oz Cu PCB area (62 mil thick board) using 14 vias each with an 18 mil diameter and 1.5 mils Cu walls. See Application Information.)	33	°C/W
	Logic control pins Enable, R_{LIMIT}, I_{LIM}, TSD, TW, Vμc	5.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS V_S = 12 V All limits apply over the temperature range, T_J = –40°C to +125°C, unless otherwise noted. Total supply $V_S = V_{CC} - V_{EE}$.

Parameter	Symbol	Condition	NCS5650 Min	NCS5650 Typ	NCS5650 Max	Units
INPUT OPERATIONAL AMPLIFIER (Op Amp A)						
Offset Voltage						
Input Offset Voltage	V_{OS}	V_{CC} = +12 V, V_{EE} = 0 V		±3	±10	mV
Offset vs Power Supply	PSRR	V_{CC} = +6 V, V_{EE} = –6 V		25	150	uV/V
Input Bias Current (Note 2)	I_B				1	nA
Input Voltage Noise Density	e_n	f = 1 kHz, V_{IN} = GND, BW = 131 kHz		250		nV/√Hz
Input Voltage Range						
Common–Mode Voltage Range	V_{CM}		V_{EE} – 0.1		V_{CC} – 3	V
Common–Mode Rejection Ratio	CMRR	V_{EE} – 0.1 ≤ V_{CM} ≤ V_{CC} – 3	70	85		dB
Input Impedance						
Differential				0.2 | 1.5		GΩ | pF
Common–Mode				0.2 | 3		GΩ | pF
Open–Loop Gain (Note 2)		R_L = 500 Ω	80	100		dB
Frequency Response						
Gain Bandwidth Product	GBW			80		MHz
Full Power Bandwidth (Note 2)		G = +5, V_{out} = 11 V_{PP}	200	1.5		MHz
Slew Rate	SR			60		V/μs
Total Harmonic Distortion + Noise	THD+N	G = +1, R_L = 500 Ω, V_O = 8 V_{PP}, f = 1 kHz, C_{in} = 220 μF, C_{out} = 330 μF		0.015		%
		G = +1, R_L = 50 Ω, V_O = 8 V_{PP}, f = 100 kHz, C_{in} = 220 μF, C_{out} = 330 μF		0.023		
Output						
Voltage Output Swing from Rail		V_{CC} = +12 V, V_{EE} = 0 V				
From Positive Rail	V_{OH}	R_L = 500 Ω to V_{CC}/2		0.3	1	V
From Negative Rail	V_{OL}	R_L = 500 Ω to V_{CC}/2		0.3	1	V
Short–Circuit Current	I_{SC}			280		mA
Output Impedance	Z0	Closed Loop G = +4, f = 100 kHz		0.25		Ω
Capacitive Load Drive	C_{LOAD}			100		pF
OUTPUT OPERATIONAL AMPLIFIER (Op Amp B)						
Offset Voltage						
Input Offset Voltage	V_{OS}	V_{CC} = +12 V, V_{EE} = 0 V		± 3	± 10	mV
Offset vs Power Supply	PSRR	V_{CC} = +12 V, V_{EE} = 0 V		25	150	μV/V
Input Bias Current (Note 2)	I_B				1	nA
Input Voltage Noise Density	e_n	f = 1 kHz, V_{IN} = GND, BW = 131 kHz		125		nV/√Hz
Input Voltage Range						
Common–Mode Voltage Range	V_{CM}		V_{EE} – 0.1		V_{CC} – 3	V
Common–Mode Rejection Ratio	CMRR	V_{EE} – 0.1 ≤ V_{CM} ≤ V_{CC} – 3	70	85		dB

2. Guaranteed by characterization or design.
3. Formula accuracy requires a resistor with ±1% tolerance.

ELECTRICAL CHARACTERISTICS V_S = 12 V All limits apply over the temperature range, T_J = –40°C to +125°C, unless otherwise noted. Total supply $V_S = V_{CC} - V_{EE}$.

Parameter	Symbol	Condition	NCS5650 Min	NCS5650 Typ	NCS5650 Max	Units
OUTPUT OPERATIONAL AMPLIFIER (Op Amp B)						
Input Impedance						
Differential				0.2 | 11		GΩ | pF
Common–Mode				0.2 | 22		GΩ | pF
Open–Loop Gain (Note 2)		R_L = 5 Ω	80	100		dB
Frequency Response						
Gain Bandwidth Product	GBW			60		MHz
Full Power Bandwidth (Note 2)		G = +2, V_{out} = 11 V_{PP}	200	400		kHz
Slew Rate	SR			70		V/μs
Total Harmonic Distortion + Noise	THD+N	G = +1, R_L = 50 Ω, V_O = 8 V_{PP}, f = 1 kHz		0.015		%
		G = +1, R_L = 50 Ω, V_O = 8 V_{PP}, f = 100 kHz		0.067		
Output						
Voltage Output Swing from Rail		V_{CC} = +12 V, V_{EE} = 0 V				
From Positive Rail	V_{OH}	I_{out} = 1.5 A to Mid–Supply		0.7	1	V
From Negative Rail	V_{OL}	I_{out} = 1.5 A to Mid–Supply		0.4	1	V
Voltage Output Swing from Rail		V_{CC} = +6 V, V_{EE} = –6 V				
From Positive Rail	V_{OH}	I_{out} = 1.5 A to GND		0.7	1	V
Negative Rail	V_{OL}	I_{out} = 1.5 A to GND		0.4	1	V
Output Impedance Enabled Mode Shutdown Mode	Z0	Closed Loop G = +1, f = 100 kHz		 0.065 12		 Ω MΩ
Capacitive Load Drive	C_{LOAD}			500		nF
BOTH AMPLIFIERS COMBINED						
Junction Temperature	T_J					
At Shutdown (Note 2)			+150	+160		°C
At Recovery from Shutdown				+135		°C
Thermal Warning Tolerance		$T_{warning}$ is determined by the ratio of two resistors (see Figure 8) (Note 3)		±10		°C
Current Limit Tolerance		I–Limit is determined by a single resistor (see Figure 5 text) (Note 3)		±50		mA
Power Supply						
Operating Voltage Range	V_S	Single–Supply Operation (V_{EE} Tied to System Common)		6 to 12	13.2	V
		Dual Balanced–Supply operation		±3.0 to ±6.0		
Quiescent Current Enabled Mode Shutdown Mode	I_Q	V_{CC} = +6 V, V_{EE} = –6 V		 20 120	 40 150	 mA μA
V_{COM}		V_{CC} = 12 V, V_{EE} = 0 V Internal resistor divider. Bypass purposes only.	5.8	6.0	6.2	V

2. Guaranteed by characterization or design.
3. Formula accuracy requires a resistor with ±1% tolerance.

ELECTRICAL CHARACTERISTICS V_S = 12 V All limits apply over the temperature range, T_J = –40°C to +125°C, unless otherwise noted. Total supply $V_S = V_{CC} - V_{EE}$.

Parameter	Symbol	Condition	NCS5650 Min	NCS5650 Typ	NCS5650 Max	Units
LOGIC INPUT/OUTPUT						
Logic/flag Supply Range	V_µc	Logic/flag supply for operation with external MCU	3.0		5.5	V
Reference Point for GND_µc	$V_{gµc}$	With Single−Sided Power Supply	V_{EE} (Pins 10 and 11) Connected to System Common			
		With Dual−Balanced Power Supply	Common of Dual Supply Connected to System Common			
Shutdown Input Mode						
Output Enabled Ve/s LOW		E/S Pin Open or Forced LOW	$V_{gµc}$ − 0.4		$V_{gµc}$ + 0.8	V
Output Shutdown Ve/s HIGH		E/S Pin Forced HIGH	$V_{gµc}$ + 2		V_µc	V
Output Enabled Ie/s LOW		E/S Pin LOW		0.1		µA
Output Shutdown Ie/s HIGH		E/S Pin HIGH		10		µA
Output Shutdown Time				60		ns
Output Enable Time (Note 2)				5	10	µs
All Flag Outputs						
HIGH State			$V_{gµc}$ + 2			V
LOW State					$V_{gµc}$ + 0.8	V

2. Guaranteed by characterization or design.
3. Formula accuracy requires a resistor with ±1% tolerance.

APPLICATIONS INFORMATION

Exposed Thermal Pad

The NCS5650 is capable of delivering 1.5 A, into a reactive load. Output signal swing should be kept as high as possible to minimize internal heat generation to keep the internal junction temperature as low as possible. The NCS5650 can swing to within 1 V of either rail without adding distortion. An exposed thermal pad is provided on the bottom of the device to facilitate heat dissipation. Application Note AND8402/D provides considerable details for optimizing the soldering down of the exposed pad. A very good example of the exposed pad implementation is provided in the layout information included with the NCS5650 Demo Board. The demo board implements 14 vias, each with an 18 mil diameter and 1.5 mils Copper walls.

Multi−Feedback Filter (MFB)

CENELEC EN 50065−1 is a European standard for signaling on low−voltage electrical installations in the frequency range 3 kHz to 148. 5kHz. More specifically Part 1 of that specification deals with frequency bands and electromagnetic disturbances introduced into the electrical mains. A practical solution to meet this requirement is to place a 4th−order filter between the output of the modem and the isolation transformer connected to the mains. In this datasheet a MFB filter topology is proposed to help meet the requirements of the CENELEC standard. Four (4) pole filters require two op amps for implementation. The NCS5650 has an input pre−amplifier and an output power amplifier. Therefore only passive components (R's and C's) need to be added. In addition the NCS5650 has a mid−supply virtual common at pin 2 (V_{com}) to facilitate implementation of the filter topology when powered from a single−sided power supply.

Figure 3 below shows the frequency response for each stage and the overall filter.

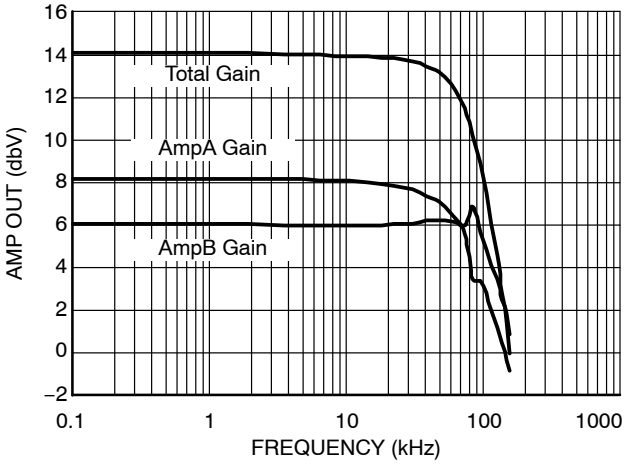


Figure 3. Amplifier Voltage vs. Frequency

Bypassing

Optimal stability and noise rejection will be implemented with power−supply bypassing placed as physically close to the device as possible. A parallel combination of 10 μF and 0.01 μF is recommended (ceramic and tantalum, respectively) for each sensitive point. For either single−supply operation or split supply operation, bypass should be placed directly across V_{CC} to V_{EE}. In addition add bypass from $V_{\mu C}$ to $GND_{\mu c}$. Reference Figure 4.

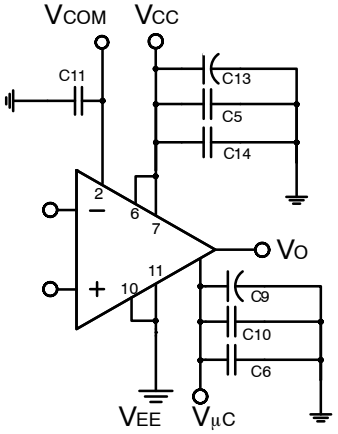


Figure 4.

Current Limit (R−Limit)

The 2 A output current of the NCS5650 can be programmed by the simple addition of a resistor (R_{Limit}) from pin 15 to V_{EE} (see Figure 5). If the load current tries to exceed the set current limit, the I_{LIM} flag will go logic High signaling the user to take any necessary action. When the current output recovers, the I_{LIM} flag will return to logic Low. The curve in Figure 5 is tolerance typically to ±50 mA. Unlike traditional power amplifiers the NCS5650 current limits functions both when sourcing and sinking current. To calculate the resistance required to program a desired current limit the following equation can be used:

$$I_{LIM} = \frac{1.215}{R_{CL}} \times 8197$$

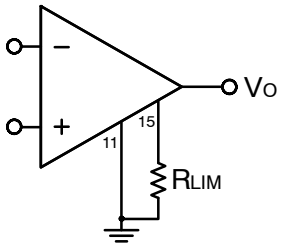


Figure 5.

Figure 6 graphically illustrates the required resistance in ohms to program the current limit.

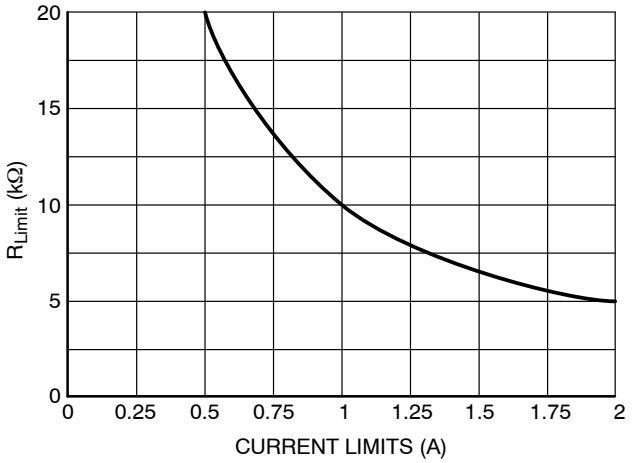


Figure 6.

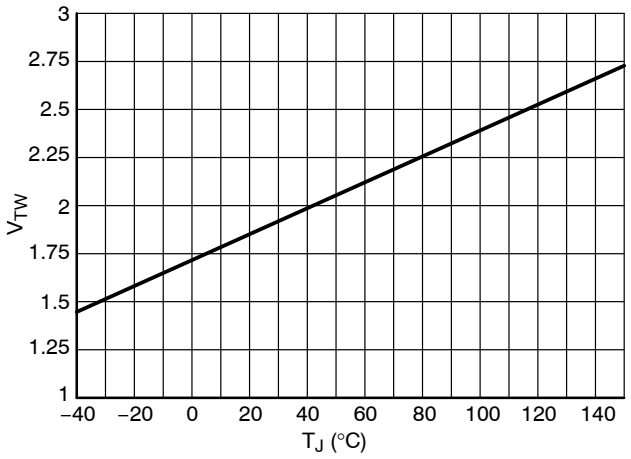


Figure 8.

Thermal Shutdown and Thermal Warning Flag

In the event load conditions cause internal over−heating the amplifier will go into shutdown to prevent damage. Under these conditions pin 17 the TSD flag (Thermal Shut Down) will go logic High. Thermal shutdown takes place at an internal junction temperature of approximately 160°C; the amplifier will recover to the Enabled mode when the junction temperature cools back down to approximately 145°C.

The user has the option to avoid entering into the TSD mode by monitoring the junction temperature via the Thermal Warning feature. Figure 8 shows how the user can select any junction temperature (T_{warn}) in the range 105°C to 145°C by applying the appropriate voltage to pin 14. A simple way to implement this feature is by setting the ratio of a voltage divider between V_{CC} (pins 6,7) and V_{EE} (the negative supply, pin 10 or 11). The voltage ratio required to program the thermal warning of the NCS5650 can be calculated using the following equation:

$$VTW = 6.665 \times 10^{-3} (T_J) + 1.72$$

Figure 8 illustrates the linearity of the internal junction temperature to the required voltage on pin 14 (T_{warn}).

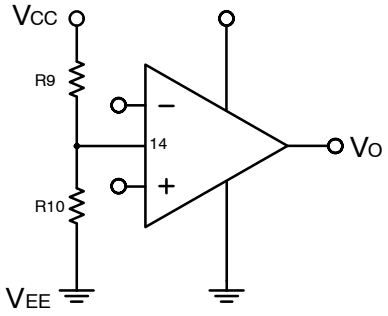


Figure 7.

Virtual Common (V_{com})

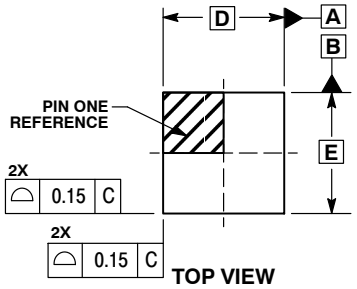
The principal purpose of V_{com} is to provide a convenient virtual common for implementing the 4th−order CENELEC filter when operating on single−sided power supply. When operating on balanced split supplies it is recommended to use the power supply common for the filter implementation and to leave V_{com} floating.

Digital Power Supply GND−Reference and Translators

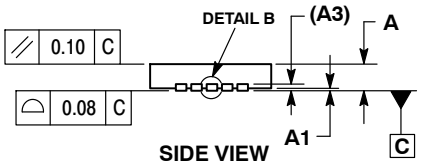
In many mixed signal applications analog GND and digital GND are not always at the same potential. To minimize GND loop issues, the NCS5650 has a separate GND pin (pin 20) which should be used to reference the digital supply and the warning flags (pins 16, 17, and 18). In most applications this would be the same GND reference used for the PLC modem. Please note that at some point in the application digital GND and analog GND must be tied together.

PACKAGE DIMENSIONS

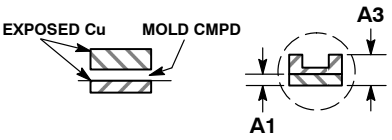
QFN20, 4x4, 0.5P
CASE 485E–01
ISSUE A



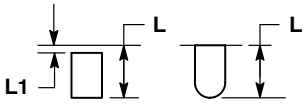
TOP VIEW



SIDE VIEW



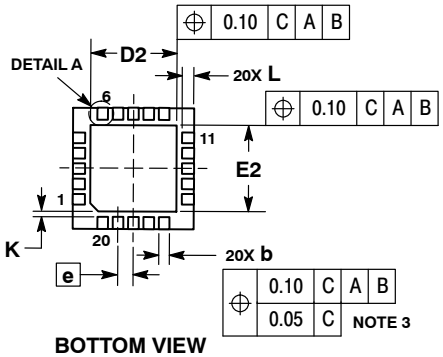
DETAIL B
OPTIONAL CONSTRUCTIONS



DETAIL A
OPTIONAL CONSTRUCTIONS

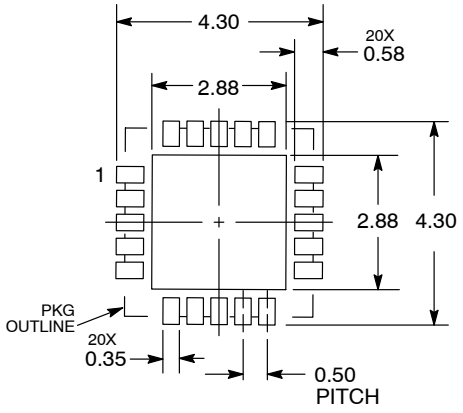
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15



BOTTOM VIEW

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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NCS5650/D