NBLVEP16VR

2.5V/3.3V/5V ECL Differential Receiver/Driver with Oscillator Gain Stage and Enabled High Gain Outputs

The NBLVEP16VR is an ECL/LVPECL oscillator gain stage with high−gain output buffers, selectable output enable and a feedback buffer. The NBLVEP16VR is a solution for crystal oscillators and SAW−based voltage−controlled oscillators.

- Q and $\overline{Q}$ Outputs have Selectable 4 mA or 8 mA, Self Bias Current Sources
- QHG and $\overline{QHG}$ have a Selectable 10 mA, Self Bias Current Sources
- Synchronous Output Enable of the High−Gain Outputs with Selectable Disabled State
- Selectable LVCMOS/LVTTL or LVPECL Level Input of the Output Enable Pin
- Maximum Frequency > 2.5 GHz Typical
- (LV)PECL Mode Operating Range: V_{CC} = 2.375 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −5.5 V
- Temperature Compensated Inputs and Outputs
- Excellent Clock Input Sensitivity
- V_{BB} Output Supports Current Source/Sink Capability up to a Robust 1.5 mA

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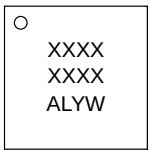
Bottom View

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM



XXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NBLVEP16VRMN	QFN−16	123 / Rail
NBLVEP16VRMNR2	QFN−16	3000/ Tape & Reel
NBWLVEP16VR	Wafer	Refer to Note 1.

1. Contact Sales Representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

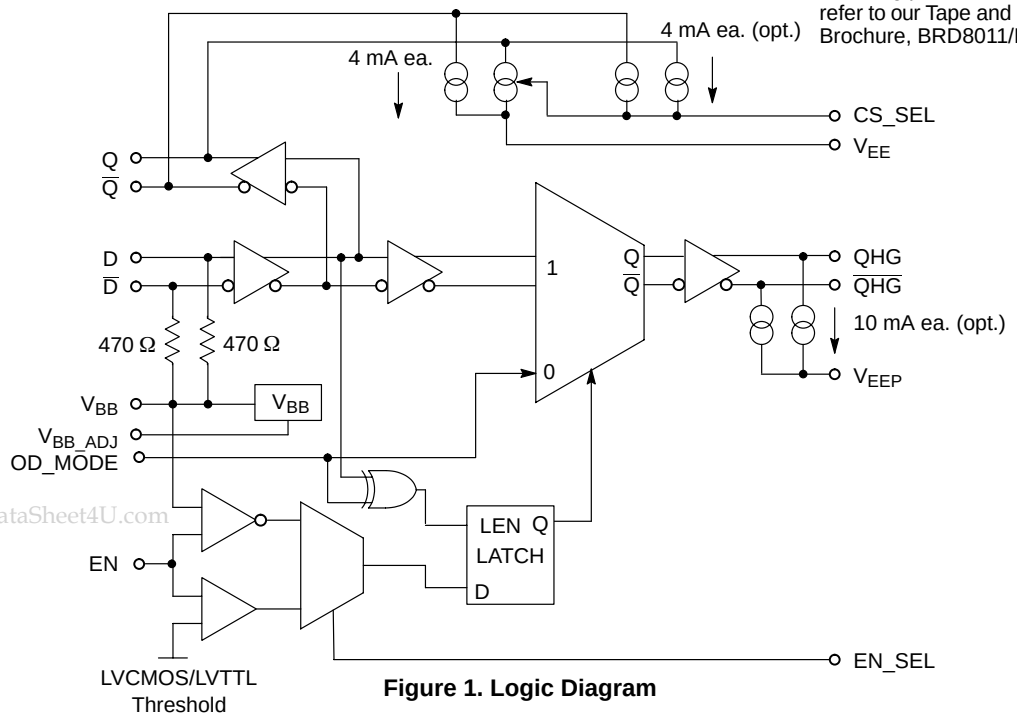


Figure 1. Logic Diagram

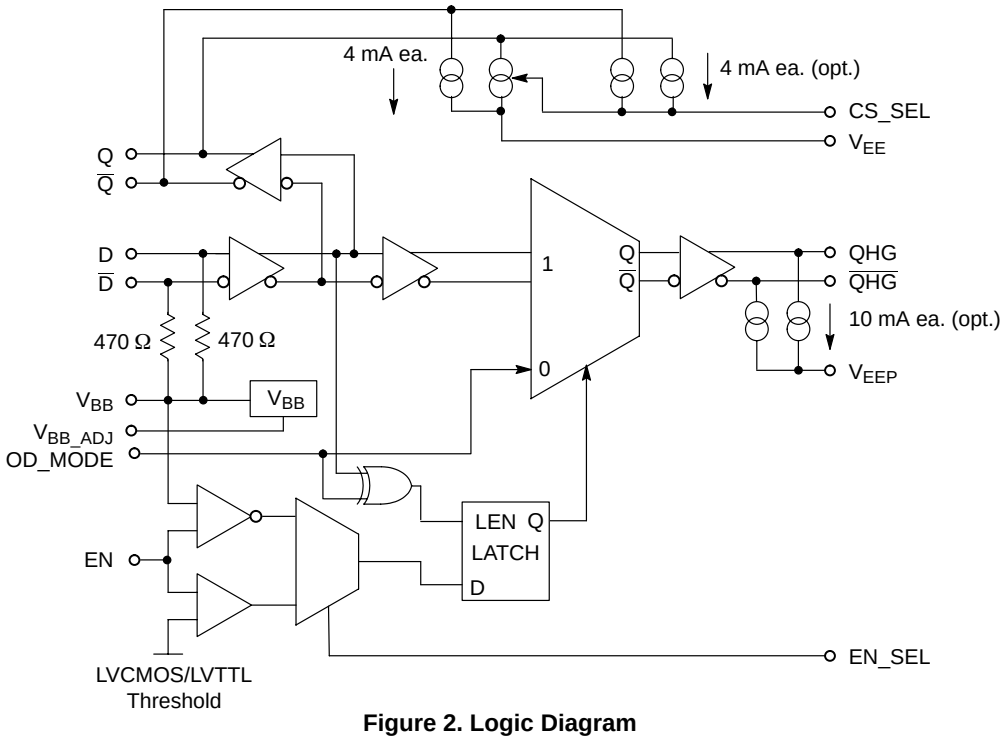


Figure 2. Logic Diagram

Table 1. Q AND $\overline{Q}$ INTERNAL CURRENT SOURCE SELECTOR

CS_SEL	Q	$\overline{Q}$	See Figure
OPEN	4 mA Typical	4 mA Typical	13, 13
V_{EE}	8 mA Typical	8 mA Typical	10, 13
V_{CC}	0 mA	4 mA Typical	13, 13

Table 2. QHG AND $\overline{QHG}$ INTERNAL CURRENT SOURCE SELECTOR

V_{EEP}	QHG	$\overline{QHG}$	See Figure
OPEN	0 mA	0 mA	8, 11
V_{EE}	10 mA Typical	10 mA Typical	9, 12

Table 3. OUTPUT ENABLE AND OUTPUT DISABLED STATE TRUTH TABLE

EN_SEL†	OD−MODE*	EN*	Q and $\overline{Q}$	QHG	$\overline{QHG}$
V_{CC} or OPEN	Low or OPEN	LVPECL Low, V_{EE} or OPEN	Data	Data	Data
V_{CC} or OPEN	Low or OPEN	LVPECL High or V_{CC}	Data	Low	High
V_{EE}	Low or OPEN	LVCMOS Low, V_{EE}, or OPEN	Data	Low	High
V_{EE}	Low or OPEN	LVCMOS High or V_{CC}	Data	Data	Data
V_{CC} or OPEN	High	LVPECL Low, V_{EE} or OPEN	Data	Data	Data
V_{CC} or OPEN	High	LVPECL High or V_{CC}	Data	High	Low
V_{EE}	High	LVCMOS Low, V_{EE}, or OPEN	Data	High	Low
V_{EE}	High	LVCMOS High or V_{CC}	Data	Data	Data

*Pins will default LOW when left open.
†Pin will default HIGH when left open.

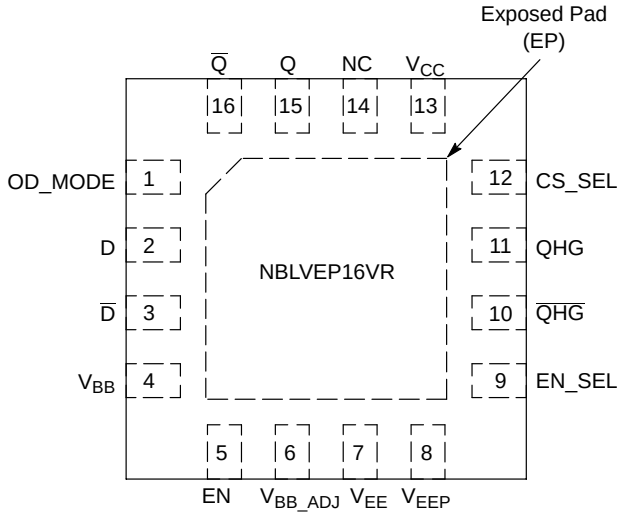


Figure 3. Pinout Diagram (Top View)

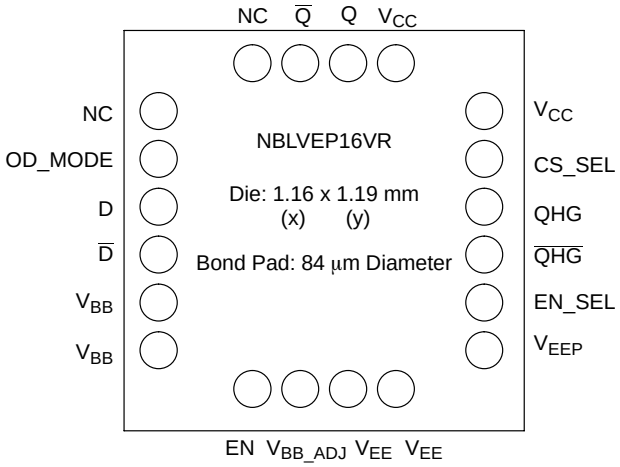


Figure 4. Die Map

Table 4. PIN DESCRIPTION

Pin No	Name	I/O	Description
1	OD_MODE*	LVCMOS/LVTTL Input (See Table 3)	Selectable Mode of Output Disabled Level
2	D	ECL / LVPECL Input	Clock / Data Input
3	$\overline{D}$	ECL / LVPECL Input	Inverted Clock / Data Input
4	V_{BB}	Reference Voltage Output	Reference Voltage Output
5	EN*	ECL / LVPECL or LVCMOS/LVTTL Input (see Table 3)	Output Enable Synchronous with D and $\overline{D}$
6	V_{BB_ADJ}		Adjust Standard V_{BB} Levels Upward When Tied to V_{CC} for 2.5 V Power Supply. Open for 3.3 V and 5 V Power Supply.
7	V_{EE}	Negative Power Supply	Negative Power Supply
8	V_{EEP}		Open or Tied to V_{EE} (See Table 1) Optional 10mA Current Source For QHG and $\overline{QHG}$
9	EN_SEL†	LVCMOS / LVTTL Input (See Table 3)	Input LVEL Selector Pin for EN
10	$\overline{QHG}$	ECL / LVPECL Output	Inverted High−Gain Output, Gain > 200
11	QHG	ECL / LVPECL Output	High−Gain Output, Gain > 200
12	CS_SEL		Selects Q and $\overline{Q}$ Current Source Magnitude (see Table 1), Open or Tied to V_{EE} or V_{CC}
13	V_{CC}	Positive Power Supply	Positive Power Supply
14	NC	No Connect	No Connect
15	Q	ECL / LVPECL Output	ECL/LVPECL Output for Feedback Loop
16	$\overline{Q}$	ECL / LVPECL Output	Inverted ECL/LVPECL Output for Feedback Loop
	EP	Power Supply (OPT)	Exposed Pad on Package Bottom Should Only Be Connected to V_{EE} or Left Open

*Pins will default LOW when left open.
†Pin will default HIGH when left open.

APPLICATIONS INFORMATION

The NBLVEP16VR is an ECL/LVPECL oscillator gain stage with high−gain output buffers, selectable output enable and a feedback buffer. The NBLVEP16VR is a solution for crystal oscillators and SAW−based voltage−controlled oscillators. Design versatility is enhanced with EN, a synchronous output enable pin to eliminate runt pulses; EN_SEL, an input state selector pin offering LVCMOS/LVTTL or ECL/LVPECL level control of EN; and OD_MODE, an output disable mode state pin which selects the polarity of the high−gain output's disabled state.

The NBLVEP16VR Q and $\overline{Q}$ outputs are ideal for feedback applications common in crystal oscillator gain blocks. They each have a selectable on−chip pull−down current source. External resistors may be used to increase the pull−down current to a maximum of 25 mA. The QHG and $\overline{QHG}$ outputs each have an optional on−chip pull−down current source of 10 mA. When V_{EEP} is left open, the 10 mA output current sources are disabled and the QHG and $\overline{QHG}$ outputs operate as standard ECL/LVPECL. When V_{EEP} is connected to V_{EE}, the 10 mA current sources are activated. The QHG and $\overline{QHG}$ pull−down current can be decreased by using a resistor connect from V_{EEP} to V_{EE}. See current source truth table for functions and options.

The output enable input pin, EN, is synchronized with the D and $\overline{D}$ data input signals in a way that furnishes glitchless gating of the QHG and $\overline{QHG}$ outputs and allows continuous oscillator operation. For applications that require output enable control, the NBLVEP16VR provides expanded output enable selectability. The logic level of the input state selector pin, EN_SEL, will determine whether the EN pin accepts ECL/LVPECL or LVCMOS/LVTTL logic levels.

The output disable mode state pin, OD_MODE, adds functional flexibility by giving the designer a choice of the QHG outputs' polarity when these high−gain outputs are disabled. For example, with OD_MODE LOW and EN LOW (LVPECL), the input is passed to the outputs and the data output equals the data input. If the D input is LOW when the EN goes HIGH, the next data transition to a HIGH is ignored and QHG remains LOW and $\overline{QHG}$ remains HIGH. The next positive transition of the data input is not passed on to the QHG outputs under these conditions. The QHG and $\overline{QHG}$ outputs remain in their disabled state as long as the EN input is held HIGH. The EN input has no influence on the Q or $\overline{Q}$ outputs and the data inputs are passed on to these outputs whether EN is HIGH or LOW. When the data input is HIGH and EN goes HIGH, it will force QHG LOW and $\overline{QHG}$ HIGH on the next negative transition of the D input. This configuration is ideal for crystal oscillator applications where the oscillator can be free−running and QHG/$\overline{QHG}$ gate on and off synchronously without adding extra counts to the output. See truth table and timing diagram for detailed ENable functions and options.

The NBLVEP16VR provides a V_{BB} and internal 470 Ω bias resistors from D to V_{BB} and $\overline{D}$ to V_{BB} for ac coupled single−ended or differential input signal(s). The V_{BB_ADJ} pin is used for 2.5 V single−ended operation when it is connected to V_{CC}. The V_{BB} output current source/sink capability can support a robust 1.5 mA.

For single−ended input conditions, the unused differential input is internally connected to V_{BB} as a switching reference voltage. Decouple V_{BB} and V_{CC} with a 0.01 μF capacitor. This internal V_{BB} will rebias AC coupled input(s). Inputs D or $\overline{D}$ must be signal driven or auto oscillation may result.

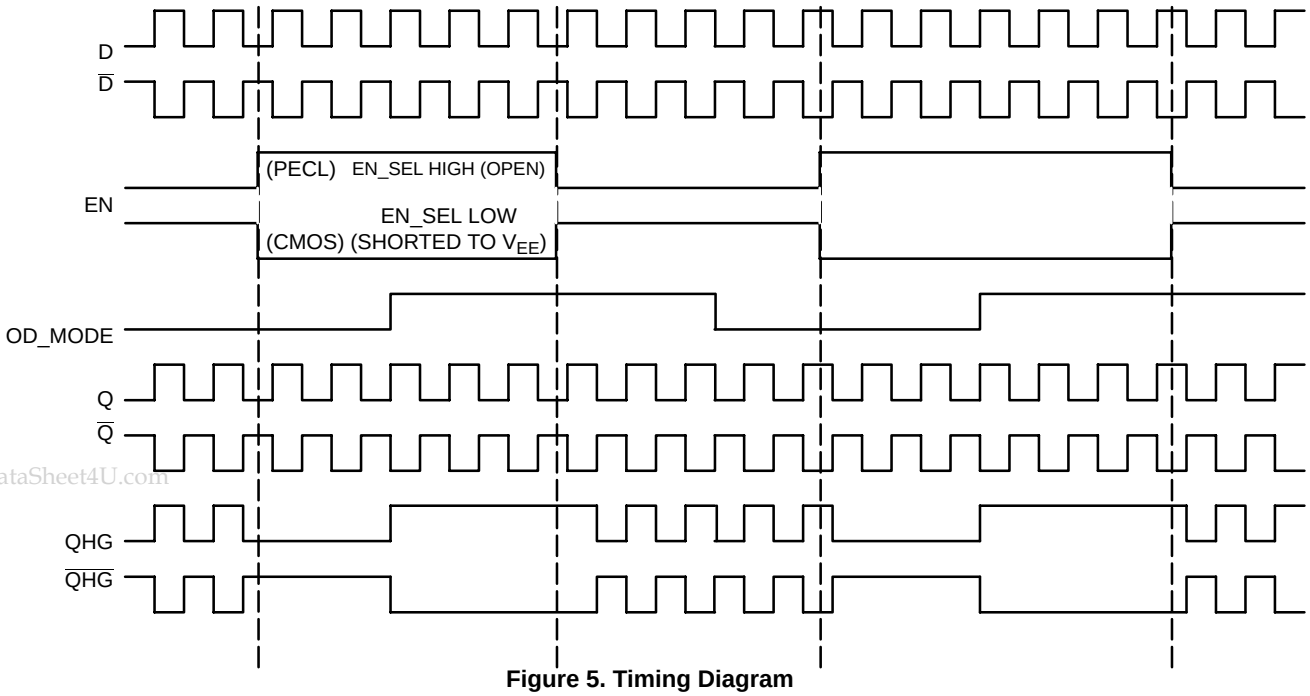


Figure 5. Timing Diagram

ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 1 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Rating	Unit
V_{CC}	LVPECL Mode Power Supply	V_{EE} = 0 V	6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V	−6	V
V_I	LVPECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	6 −6	V V
I_{BB}	V_{BB} Current Sink/Source		±1.5	mA
I_{IN}	Input Current (V_{IN} − V_{BB}) ÷ 470 Ω D, $\overline{D}$		±5	mA
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		−40 to +85	°C
T_{stg}	Storage Temperature Range		−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM 500 LFPM		°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board		°C/W

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

DC CHARACTERISTICS, LVPECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 2, 6)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 3)	30	35	48	30	38	48	35	40	54	mA
V_{OH}	Output HIGH Voltage (Note 4)	1340		1670	1340		1670	1340		1670	mV
V_{OL}	Output LOW Voltage (Note 4)	620		950	620		950	620		950	mV
V_{IH}	Input High Voltage (Single−Ended) (D, $\overline{D}$, EN) (Notes 5, 6)	1655		2000	1655		2000	1655		2000	mV
V_{IL}	Input Low Voltage (Single−Ended) (D, $\overline{D}$, EN) (Notes 5, 6)	1050		1395	1050		1395	1050		1395	mV
V_{BB}	Output Voltage Reference (Note 6)	1420	1525	1630	1420	1525	1630	1420	1525	1630	mV
V_{IHCMR}	Input High Voltage Common Mode Range (Differential Configuration)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current (Note 5) EN			150			150			150	μA
I_{IL}	Input LOW Current (Note 5) EN	0.5			0.5			0.5			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}.
3. V_{EEP} and CS_SEL open.
4. QHG/$\overline{\text{QHG}}$ outputs loaded with 50 Ω to V_{CC} − 2.0 V (V_{EEP} = OPEN) Figure 11 or with optional current source (V_{EEP} = V_{EE}) Figure 12. Q/$\overline{Q}$ outputs loaded with 8 mA current source (CS_SEL = V_{EE}).
5. EN_SEL Open.
6. V_{BB_ADJ} tied to V_{CC} for 2.5 V single−ended input operation.

DC CHARACTERISTICS, LVPECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 7)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 8)	30	38	48	30	40	48	35	42	54	mA
V_{OH}	Output High Voltage (Note 9)	2140		2470	2140		2470	2140		2470	mV
V_{OL}	Output Low Voltage (Note 9)	1420		1750	1420		1750	1420		1750	mV
V_{IH}	Input High Voltage (Single−Ended) (D, $\overline{D}$, EN) (Note 10)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input Low Voltage (Single−Ended) (D, $\overline{D}$, EN) (Note 10)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1790	1900	2030	1790	1900	2030	1790	1900	2030	mV
V_{IHCMR}	Input High Voltage Common Mode Range (Differential Configuration)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current (Note 10) EN			150			150			150	μA
I_{IL}	Input LOW Current (Note 10) EN	0.5			0.5			0.5			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

7. Input and output parameters vary 1:1 with V_{CC}.
8. V_{EEP} and CS_SEL open.
9. QHG/$\overline{\text{QHG}}$ outputs loaded with 50 Ω to V_{CC} − 2.0 V (V_{EEP} = OPEN) Figure 11 or with optional current source (V_{EEP} = V_{EE}) Figure 12. Q/$\overline{Q}$ outputs loaded with 8 mA current source (CS_SEL = V_{EE}).
10. EN_SEL Open.

DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 11)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 12)	30	41	48	30	43	48	35	45	54	mA
V_{OH}	Output High Voltage (Note 13)	3840		4170	3840		4170	3840		4170	mV
V_{OL}	Output Low Voltage (Note 13)	3120		3450	3120		3450	3120		3450	mV
V_{IH}	Input High Voltage (Single−Ended) (D, $\overline{D}$, EN) (Note 14)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input Low Voltage (Single−Ended) (D, $\overline{D}$, EN) (Note 14)	3055		3375	3055		3375	3055		3375	mV
V_{BB}	Output Voltage Reference	3490	3600	3730	3490	3600	3730	3490	3600	3730	mV
V_{IHCMR}	Input High Voltage Common Mode Range (Differential Configuration)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current (Note 14) EN			150			150			150	μA
I_{IL}	Input LOW Current (Note 14) EN	0.5			0.5			0.5			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}.
12. V_{EEP} and CS_SEL open.
13. QHG/$\overline{QHG}$ outputs loaded with 50 Ω to V_{CC} − 2.0 V (V_{EEP} = OPEN) Figure 11 or with optional current source (V_{EEP} = V_{EE}) Figure 12. Q/$\overline{Q}$ outputs loaded with 8 mA current source (CS_SEL = V_{EE}).
14. EN_SEL Open.

DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −5.5V to −2.375 V (Note 15)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current (Note 16)	30	38	48	30	40	48	35	42	54	mA
V_{OH}	Output High Voltage (Note 17)	−1160		−830	−1160		−830	−1160		−830	mV
V_{OL}	Output Low Voltage (Note 17)	−1880		−1550	−1880		−1550	−1880		−1550	mV
V_{IH}	Input High Voltage (Single−Ended) (D, $\overline{D}$, EN) (Notes 18, 19) −3.3 V V_{BB_ADJ} = OPEN −2.5 V V_{BB_ADJ} = V_{CC}	 −1225 −845		 −880 −500	 −1225 −845		 −880 −500	 −1225 −845		 −880 −500	mV
V_{IL}	Input Low Voltage (Single−Ended) (D, $\overline{D}$, EN) (Notes 18, 19) −3.3 V V_{BB_ADJ} = OPEN −2.5 V V_{BB_ADJ} = V_{CC}	 −1945 −1450		 −1625 −1105	 −1945 −1450		 −1625 −1105	 −1945 −1450		 −1625 −1105	mV
V_{BB}	Output Voltage Reference −3.3 V or −5.2 V V_{BB_ADJ} = OPEN −2.5 V (Note 19) V_{BB_ADJ} = V_{CC}	 −1510 −1080	 −1400 −975	 −1270 −870	 −1510 −1080	 −1400 −975	 −1270 −870	 −1510 −1080	 −1400 −975	 −1270 −870	mV
V_{IHCMR}	Input High Voltage Common Mode Range (Differential Configuration) $V_{EE} \le -5$ V	V_{EE}+1.2 V_{EE}+2.0		0	V_{EE}+1.2 V_{EE}+2.0		0	V_{EE}+1.2 V_{EE}+2.0		0	V V
I_{IH}	Input HIGH Current (Note 18) EN			150			150			150	μA
I_{IL}	Input LOW Current (Note 18) EN	0.5			0.5			0.5			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

15. Input and output parameters vary 1:1 with V_{CC}.
16. V_{EEP} and CS_SEL open.
17. QHG/$\overline{QHG}$ outputs loaded with 50 Ω to V_{CC} − 2.0 V (V_{EEP} = OPEN) Figure 11 or with optional current source (V_{EEP} = V_{EE}) Figure 12. Q/$\overline{Q}$ outputs loaded with 8 mA current source (CS_SEL = V_{EE}).
18. EN_SEL Open.
19. V_{BB_ADJ} tied to V_{CC} for −2.5 V single−ended operation.

(LVCMOS/LVTTL DC CHARACTERISTICS
V_{CC} = 2.375 V or 5.0 V, V_{EE} = 0 V or V_{CC} = 0 V, V_{EE} = −2.375 V to −5.5 V (Note 20)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input High Voltage	V_{EE}+2.0		V_{CC}	V_{EE}+ 2.0		V_{CC}	V_{EE}+2.0		V_{CC}	V
V_{IL}	Input Low Voltage	V_{EE}		V_{EE}+0.8	V_{EE}		V_{EE}+0.8	V_{EE}		V_{EE}+0.8	V
I_{IH}	Input HIGH Current	−150		150	−150		150	−150		150	μA
I_{IL}	Input LOW Current	−150		150	−150		150	−150		150	μA

20. EN_SEL = LOW When EN is Used as a LVCMOS/LVTTL Input.

AC CHARACTERISTICS V_{CC} = 2.375 V to 5.5 V; V_{EE} = 0 V or V_{CC} = 0 V V_{EE} = −2.375 V to −5.5 V (Note 21)

Symbol	Characteristic		−40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Differential Output (QHG) Voltage (Peak−to−Peak)	f_{out} < 1 GHz f_{out} < 2 GHz f_{out} < 2.5 GHz	500 260 210	660 500 400		500 310 210	700 500 380		500 280 190	700 450 330		mV mV
t_{PLH}, t_{PHL}	Propagation Delay (Differential) Figure 10 D to Q (CS_SEL = OPEN) Figure 10 D to Q (CS_SEL = V_{EE}) Figure 8 D to QHG (V_{EEP} Open) Figure 9 D to QHG (V_{EEP} = V_{EE})		 215 155 315 320	 290 270 390 400	 385 395 475 490	 215 165 335 335	 300 280 410 415	 385 405 495 505	 230 205 360 360	 315 300 440 450	 400 445 520 530	ps
t_S	Set−Up Time	EN to D	0.5			0.5			0.5			ns
t_H	Hold Time	EN to D	1.0			1.0			1.0			ns
t_{JITTER}	Random Clock Jitter (RMS)			0.5			0.5			0.5		ps
t_{SKEW}	Duty Cycle Skew (Note 23)			5	20		5	20		5	20	ps
V_{INPP}	Differential Input Voltage (Peak−to−Peak) (Note 22) Single−Ended Configuration	D to QHG D to Q D to QHG	25 50 50	800 800	1200 1200	25 50 50	800 800	1200 1200	25 50 50	800 800	1200 1200	mV mV mV
t_r t_f	Output Rise/Fall Times (20% − 80%) Q, $\overline{Q}$ (CS_SEL = V_{EE} or OPEN) QHG, $\overline{QHG}$ ($\overline{V}_{EEP}$ = V_{EE} or OPEN)		 70 90	 120 150	 300 210	 70 90	 120 150	 300 210	 70 90	 120 150	 300 210	ps
DC_O	Output Duty Cycle (Note 24) (QHG)		45	50	55	45	50	55	45	50	55	%

21. QHG/$\overline{QHG}$ and Q/$\overline{Q}$ outputs loaded with AC coupled 50 Ω loads. V_{EEP} and CS_SEL connected to V_{EE}.
22. V_{INPP} is the minimum differential Peak−to−Peak input swing for which AC parameters are guaranteed.
23. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs, ($t_{pLH} - t_{pHL}$).
24. Assumes 50% Input Duty Cycle, see Figures 11 or 12.

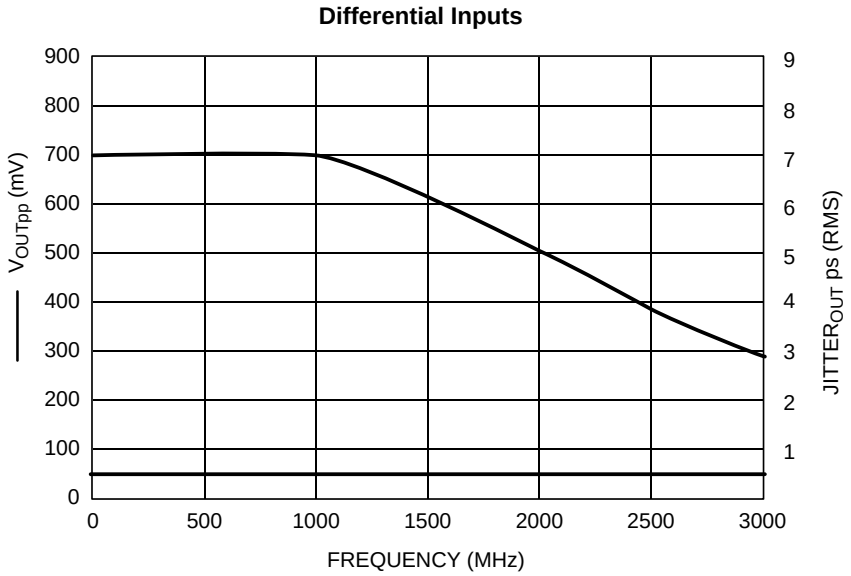


Figure 6. F_{max}/Jitter for QHG, $\overline{QHG}$ Output

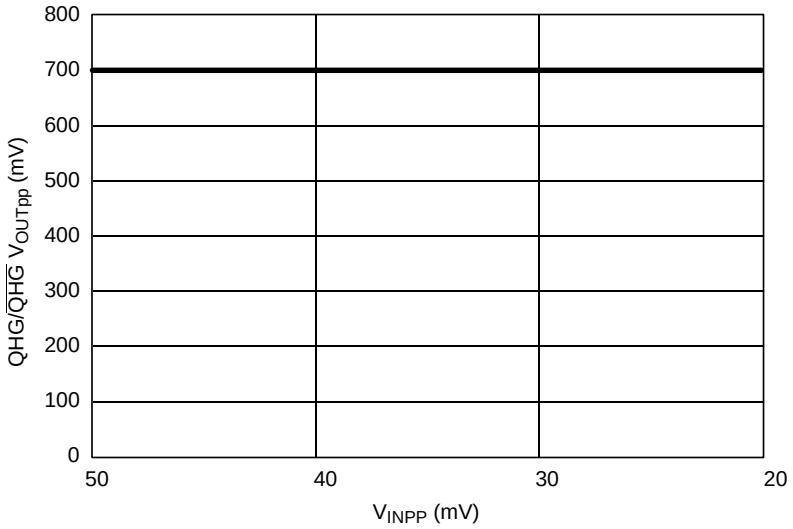


Figure 7. Differential Gain vs. Input Voltage (100 MHz)

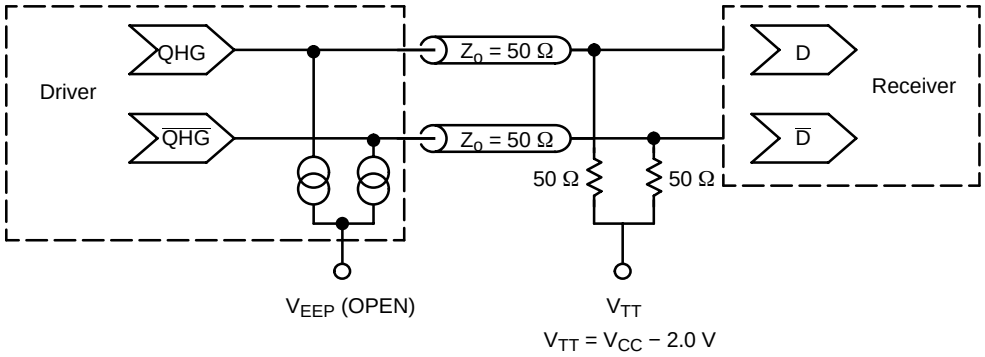


Figure 8. Typical Termination for Output Driver
V_{EEP} Open (See Application Note AND8020 − Termination of ECL Logic Devices.)

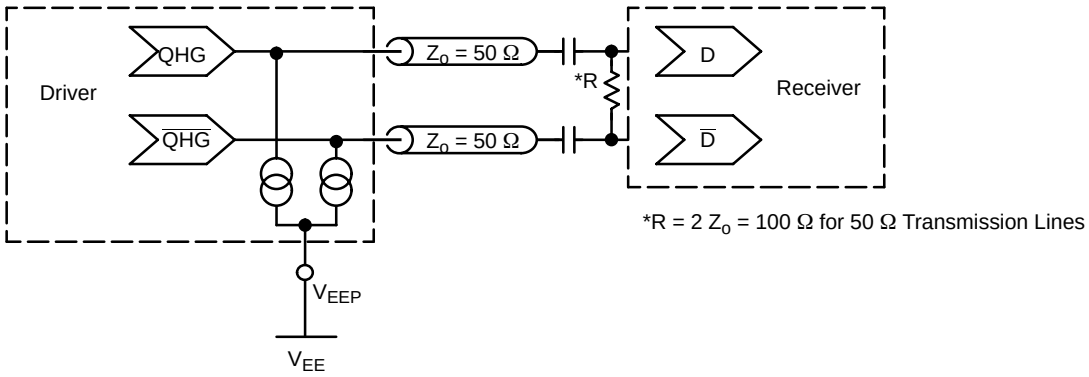


Figure 9. QHG/$\overline{QHG}$ Output Loading and Termination, $V_{EEP} = V_{EE}$.

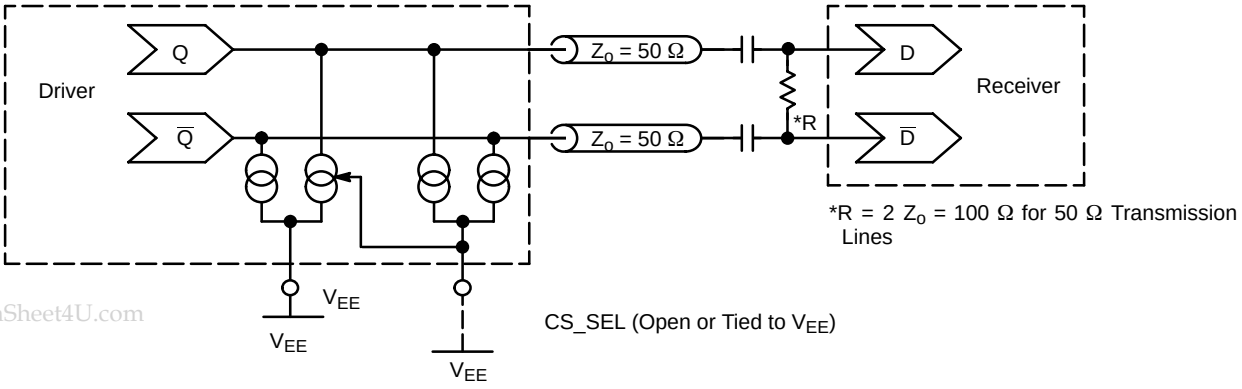


Figure 10. Q/$\overline{Q}$ Output Loading and Termination, CS_SEL Open or Tied to V_{EE} or V_{CC}

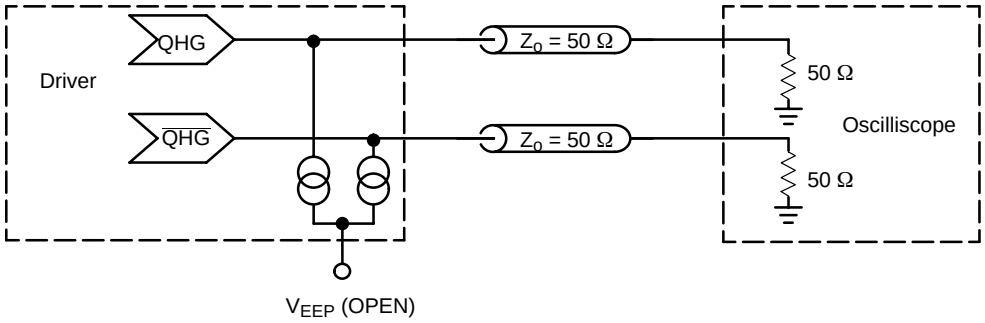


Figure 11. QHG/$\overline{QHG}$ Device Evaluation Set−up; V_{EEP} = OPEN

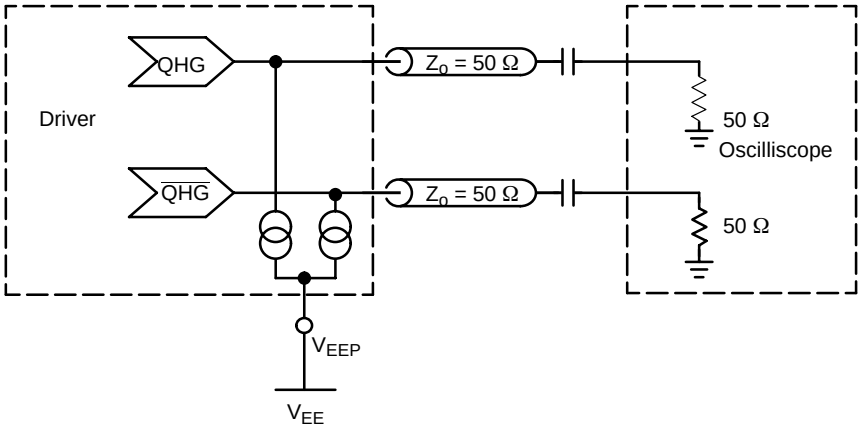


Figure 12. QHG/$\overline{QHG}$ Device Evaluation Set−up; V_{EEP} = V_{EE}

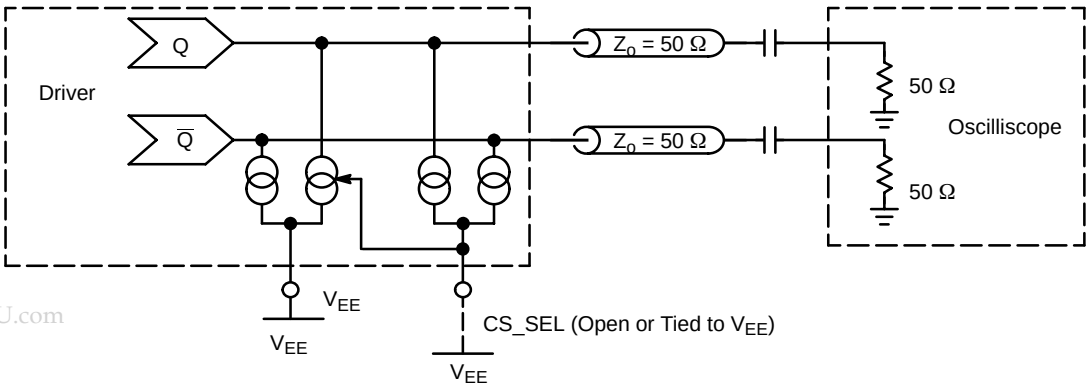


Figure 13. Q/$\overline{Q}$ Device Evaluation Set−up; CS_SEL = V_{EE} or OPEN

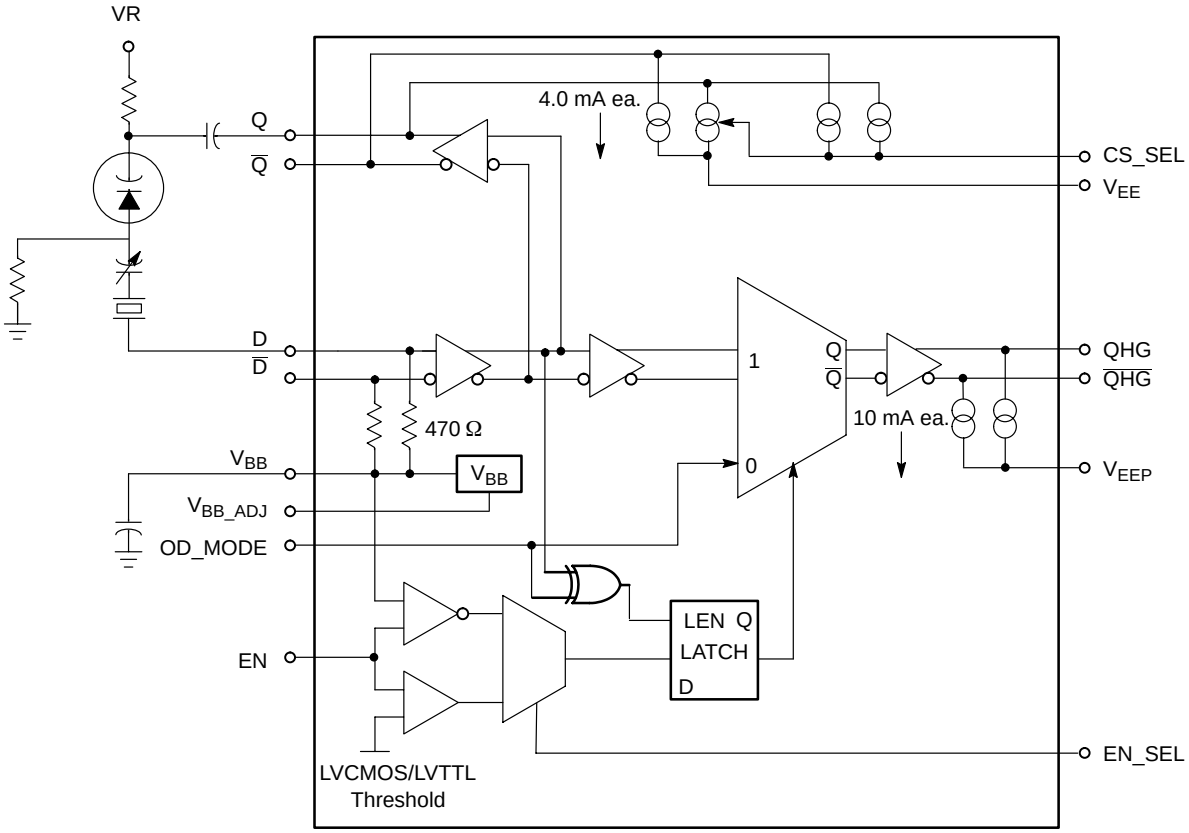


Figure 14. Typical Application

The VCXO, or voltage controlled crystal oscillator, is an oscillator where the output frequency is controlled by the crystal and an external control voltage. The VCXO can have the output frequency change with a change in voltage at a control pin of the oscillator. Most, if not all, VCXO's use varactor diodes to vary the frequency. A varactor diode is a semiconductor device that behaves as a variable capacitor when a voltage is applied to it. Thus, when a change in the control voltage is applied to the control pin of the oscillator, it causes a change in the capacitance seen by the crystal internal to the oscillator. These changes in the circuit load capacitance cause changes in the oscillator output frequency due to crystal loading.

Resource Reference of Application Notes

AN1404 − ECLinPS Circuit Performance at Non−Standard V_{IH} Levels

AN1406 − Designing with LVPECL (ECL at +5.0 V)

AND8002 − Marking and Date Codes

AND8009 − ECLinPS Plus Spice I/O Model Kit

AND8020 − Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

PACKAGE DIMENSIONS

QFN−16
CASE 485G−01
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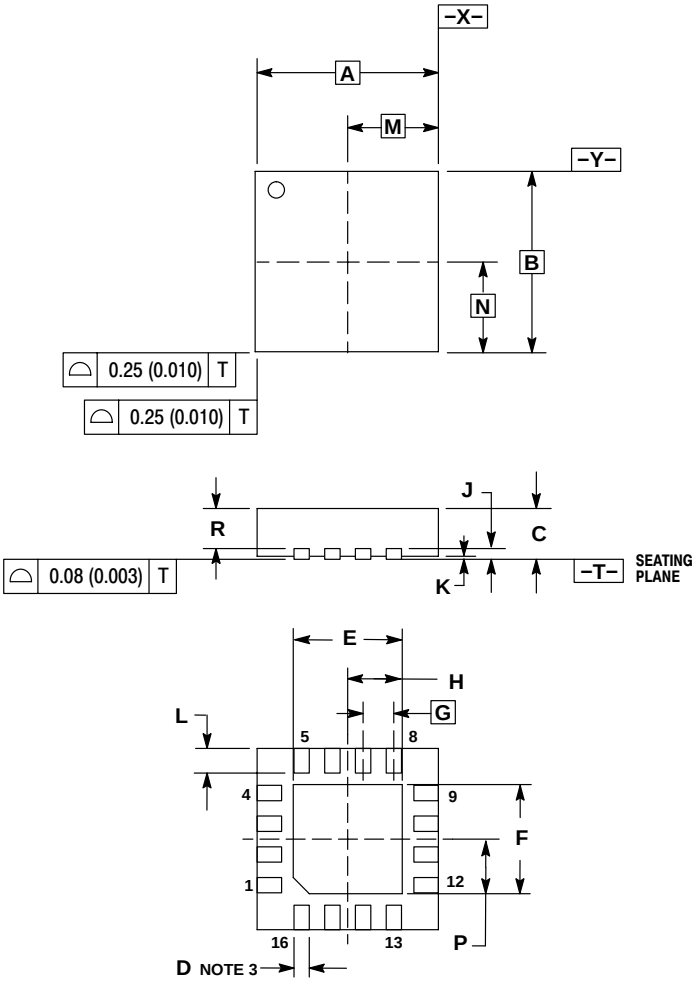

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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