N- and P-Channel 12-V (D-S) MOSFET

CHARACTERISTICS

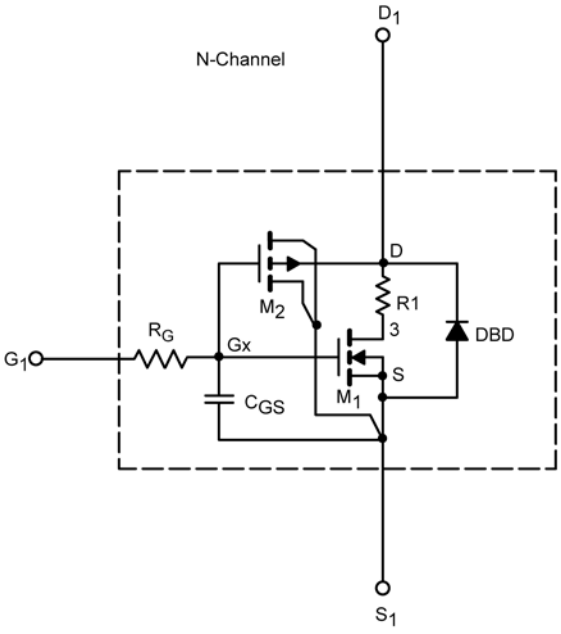
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

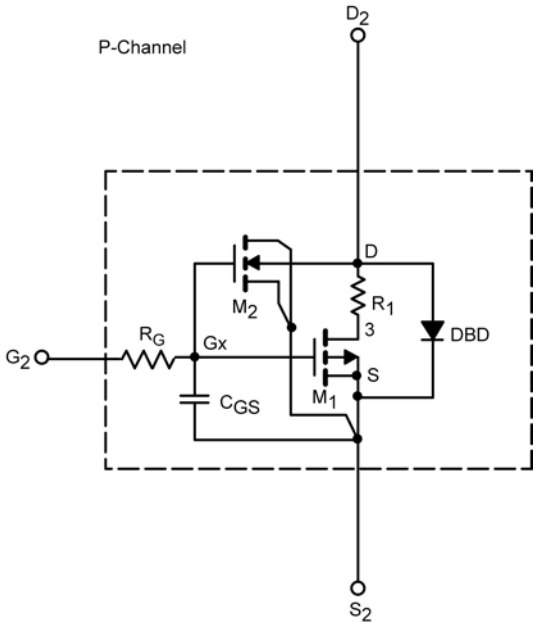
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 4.5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





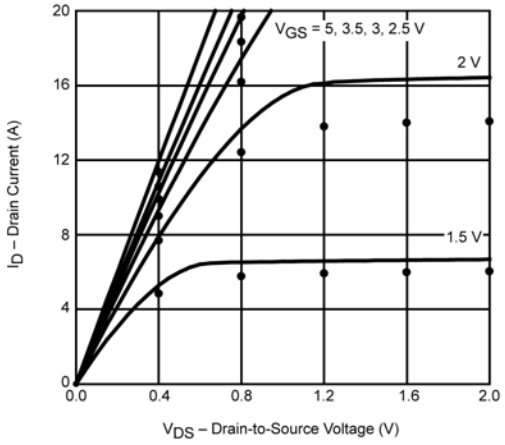
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

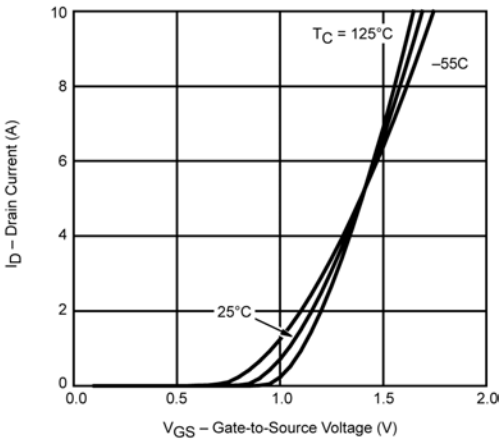
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.55		
		V_{DS} = V_{GS}, I_D = –250 µA	P-Ch	0.84		
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.2 A	N-Ch	0.034	0.033	Ω
		V_{GS} = –4.5 V, I_D = – 3.3 A	P-Ch	0.058	0.058	
		V_{GS} = 2.5 V, I_D = 3.8 A	N-Ch	0.041	0.039	
		V_{GS} = –2.5 V, I_D = – 2.8 A	P-Ch	0.085	0.082	
		V_{GS} = 1.8 V, I_D = 1.6 A	N-Ch	0.051	0.051	
		V_{GS} = –1.8 V, I_D = – 0.70 A	P-Ch	0.121	0.111	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.2 A	N-Ch	14	13	S
		V_{DS} = –10 V, I_D = –3.3 A	P-Ch	15	9	
Diode Forward Voltage[a]	V_{SD}	I_S = 4.4 A, V_{GS} = 0 V	N-Ch	0.95	0.80	V
		I_S = –3.4 A, V_{GS} = 0 V	P-Ch	0.70	–0.80	
Dynamic[b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = –6 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	448	400	pF
			P-Ch	429	400	
Output Capacitance	C_{oss}		N-Ch	117	120	
			P-Ch	142	140	
Reverse Transfer Capacitance	C_{rss}		N-Ch	57	70	
			P-Ch	101	100	
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 8 V, I_D = 5.5 A	N-Ch	6.5	7.5	nC
		V_{DS} = –6 V, V_{GS} = –8 V, I_D = –4.3 A	P-Ch	5.6	8	
		N-Channel V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 5.5 A P-Channel V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –4.3 A	N-Ch	3.9	4.5	
			P-Ch	3.5	5	
Gate-Source Charge	Q_{gs}		N-Ch	0.60	0.60	
			P-Ch	0.80	0.80	
Gate-Source Charge	Q_{gs}		N-Ch	0.80	0.80	
			P-Ch	1.4	1.4	

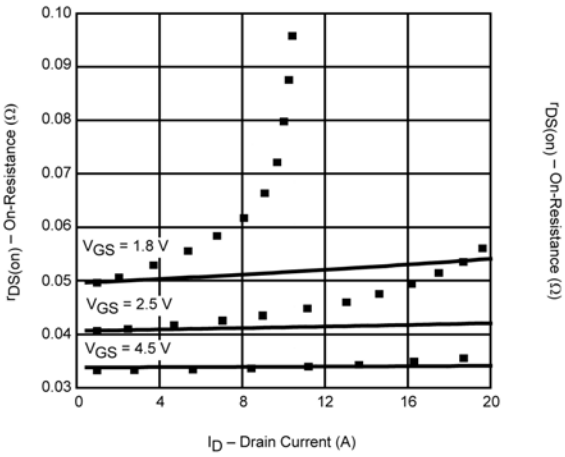
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

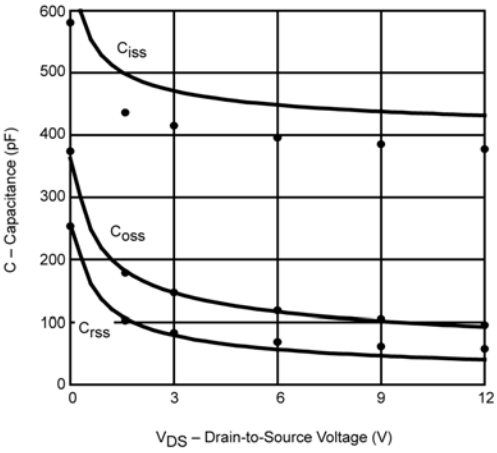
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

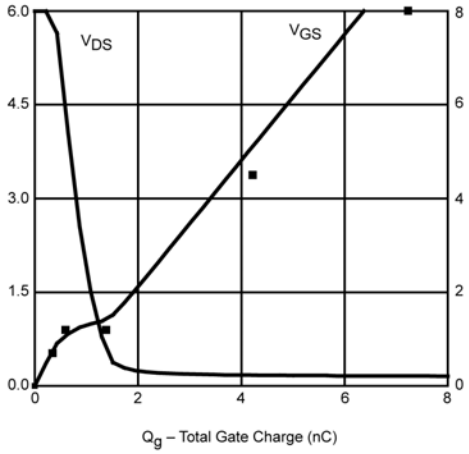
N-Channel MOSFET

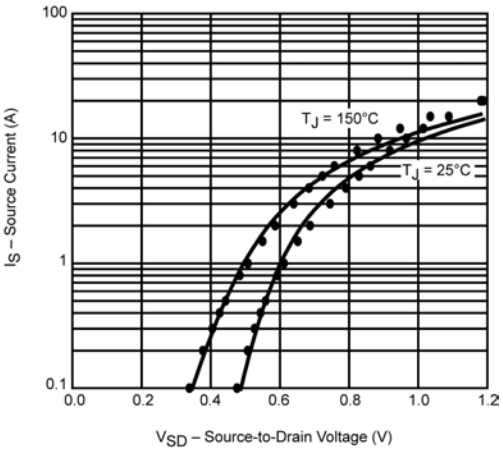






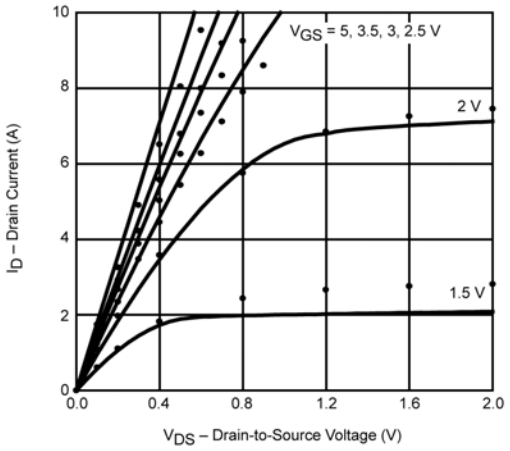


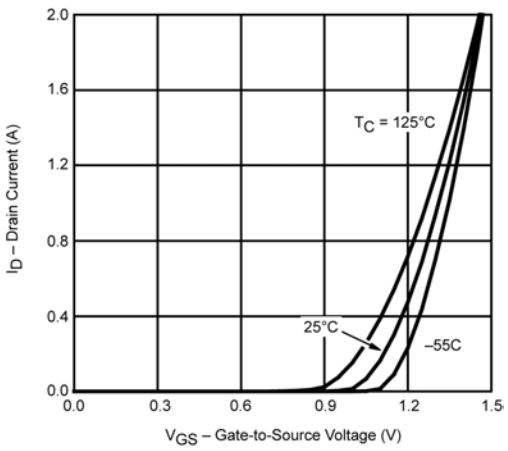


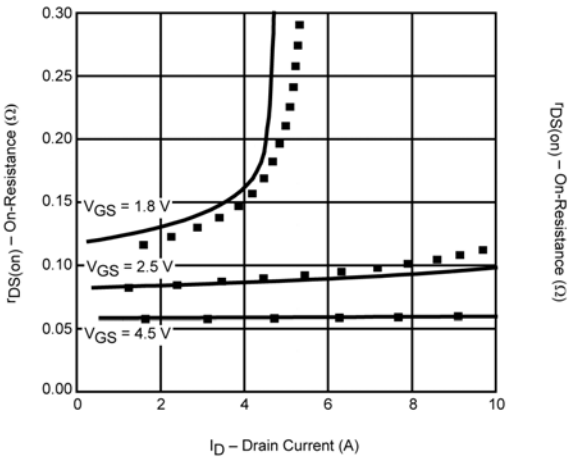


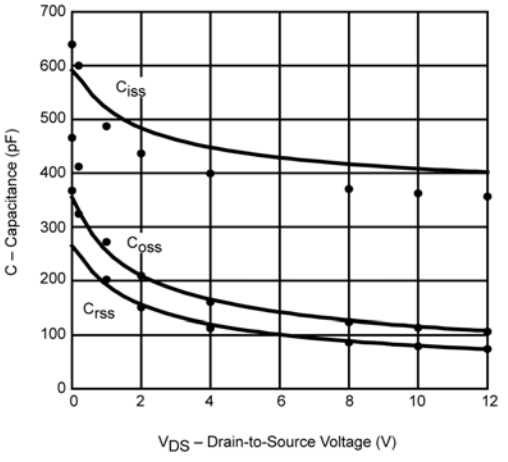
Note: Dots and squares represent measured data.

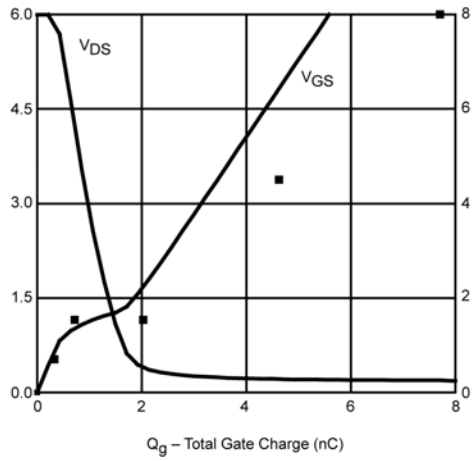
P-Channel MOSFET

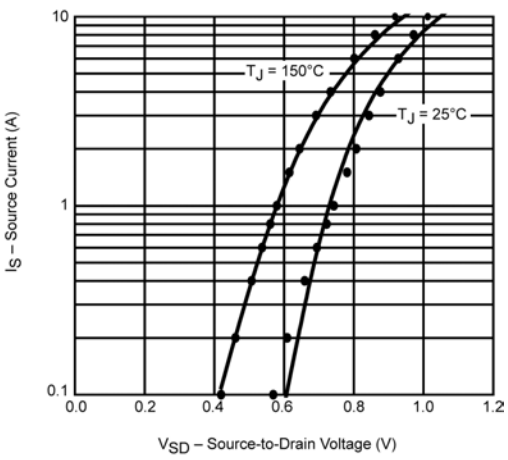












Note: Dots and squares represent measured data.

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