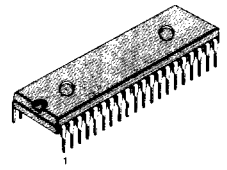
HIGH-SPEED A/D-D/A CONVERTER (20MHz 8-bit A/D + 10-bit D/A)

40 DIP



The KSV3110 consists of high speed low glitch 10-bit DAC and high speed flash 8-bit ADC with the various auxiliary circuits (reference voltage source, pre buffer amp, input clamp circuit and feed-in output amp).

The KSV3110 is suitable for video application, capable of converting an analog signal with full power frequency components up to 6MHz into 8-bit digital signals.

All digital inputs and outputs are TTL compatible.

FEATURES

- **8-bit A/D + 10 bit D/A resolution**
- **TTL digital interface**
- **Internal input buffer amp**
- **Internal clamp circuit (Peak, Keyed)**
- **20MSPS conversion rate**
- **Internal reference voltage (2V)**
- **Internal feed-in amp**
- **Few external components for application**
- **Easy and simple video application**

APPLICATIONS

- Medical image processor
- Data acquisition systems
- Radar data conversion
- Video data conversion

BLOCK DIAGRAM

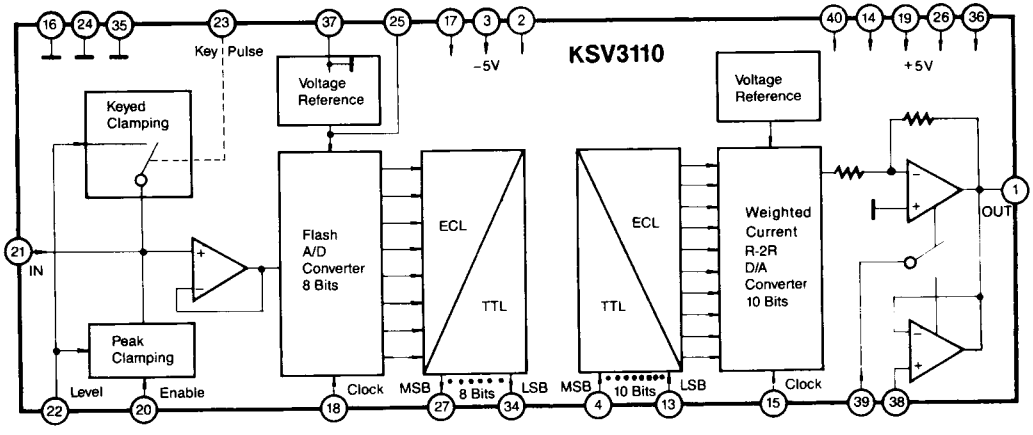


Fig. 1

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	Analog Output D/A Converter	21	Analog Input A/D Converter
2	−5V Supply D/A-Analog	22	Clamping Level Input
3	−5V Supply D/A Converter-Digital	23	Clamping Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5V Supply A/D Converter-Digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5V Supply D/A Converter-Analog-Digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter-Analog	35	Digital Ground A/D Converter
16	GND D/A Conv. & Clock A/D Converter	36	+5V Supply A/D Converter-Analog
17	−5V Supply A/D Converter-Analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter-Analog	38	External Analog Input
19	+5V Supply A/D Converter	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	+5V Supply D/A-Analog

EVALUATION CIRCUIT

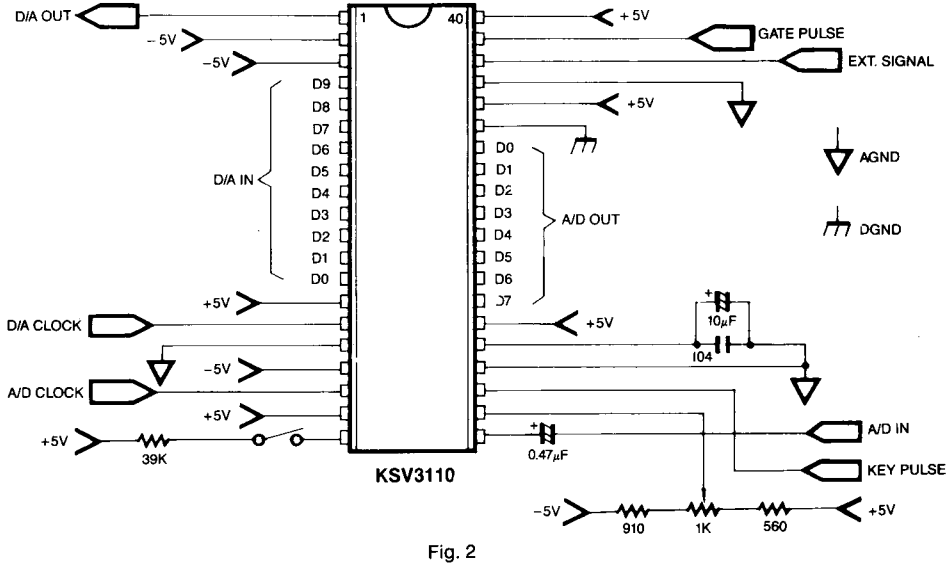


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	−0.5 to +6	V
Negative Supply Voltage	V_{EE}	+0.5 to −6	V
Input Voltages (digital)	V_{DI}	−0.5 to +5.5	V
Input Voltages (analog)	V_{AI}	−0.5 to +5.5	V
Digital Output Applied Voltage	V_{DO}	−0.5 to +5.5	V
Digital Output Forced Current	I_{DO}	−2.0 to +6.0	mA
Digital Output Short Time	t_{SHORT}	1	sec
Analog Output Applied Voltage	V_{AO}	−0.5 to +5.5	V
Analog Output Forced Current	I_{AO}	−10 to +0.5	mA
Ambient Operating Temperature	T_A	−25 to +85	degree
Storage Temperature Range	T_{stg}	−40 to +125	degree

NOTE: 1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.
3. Applied voltage must be current limited to specified range.
4. Current is specified as positive when flowing into the device.

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5.0	−5.25	V
A/D Converter					
Clock High Time (1)	t_{CKH1}	15			ns
Clock Low Time (1)	t_{CKL1}	25			ns
Clamping Pulse High Time	t_{CLPH}	1			μs
Clamping Pulse Low Time	t_{CLPL}	1			μs
Digital Input High Voltage (1)	V_{DIH1}	2.0			V
Digital Input Low Voltage (1)	V_{DIL1}			0.8	V
Digital Output High Current	I_{DOH}			−400	μA
Digital Output Low Current	I_{DOL}			2.4	mA
Peak Clamping Resistance	R_{20}	20	39	60	Kohm
Analog Input Voltage	V_{AI}	0		V_{ref}	V
Clamping Level	V_{22}	−1		2	V
D/A Converter					
Clock High Time (2)	t_{CKH2}	20			ns
Clock Low Time (2)	t_{CKL2}	20			ns

(Continue)

OPERATING CONDITIONS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Switch Over Pulse High Time	t_{39H}	1			μs
Switch Over Pulse Low Time	t_{39L}	1			μs
Digital Input High Voltage (2)	V_{DIH2}	2.0			V
Digital Input Low Voltage (2)	V_{DIL2}			0.8	V
Digital Input Set-up Time	t_{SET}	15			ns
Digital Input Hold Time	t_{HOLD}	12			ns
External Analog Input Voltage	V_{38}	−1		3	V
Ambient Temperature	T_A	0		70	degree

2

ELECTRICAL CHARACTERISTICS (within specified operation condition)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Positive Supply Current	I_{CC}	V_{CC} = Max		105	140	mA
Negative Supply Current	I_{EE}	V_{EE} = Max		−95	−130	mA
A/D Converter						
Analog Input Bias Current	I_{AIN}	V_{AI} = 2.0V, V_{EE} = Max			5	μA
Analog Input Capacitance	C_{AIN}			5		pF
Analog Input Resistance	R_{AIN}	F_{AIN} = 100KHz		100		Kohm
Total String Resistance	R_{STRING}	$R_{(pin\ 25-pin\ 37)}$	350	450	550	ohm
Reference Voltage	V_{REF}	$V_{pin\ 25}$	1.8		2.2	V
Clock High Current	I_{CKH1}	V_{CK} = 2.4V, V_{CC} = Max			50	μA
Clock Low Current	I_{CKL1}	V_{CK} = 0.4V, V_{CC} = Max			−800	μA
Clamping Pulse High Current	I_{CLPH}	V_{CLP} = 2.4V, V_{CC} = Max		8	50	μA
Clamping Pulse Low Current	I_{CLPL}	V_{CLP} = 0.4V, V_{CC} = Max			−500	μA
Digital Output High Voltage	V_{DOH}	I_{DOH} = 0.4mA V_{CC} = Min	2.4			V
Digital Output Low Voltage (1)	V_{DOL1}	I_{DOL} = 1.6mA V_{CC} = Min			0.5	V
Digital Output Low Voltage (2)	V_{DOL2}	I_{DOL} = 2.4mA V_{CC} = Min			0.7	V
Maximum Conversion Rate	F_{AS}	V_{CC}, V_{EE} = Min	20			MSPS
Aperture Delay Time	t_{AP}	V_{CC}, V_{EE} = Min	−10		0	ns
Digital Output Delay	t_D	V_{CC}, V_{EE} = Min		15	20	ns
Clamp Level Sink Current	I_{22}	Peak: off, Keyed: off	0		150	μA
Peak Clamp Level Difference	$\triangle V_{PEAK}$	V_{22} V_{21}	−250	−100	0	mV
Keyed Clamp Level Difference	$\triangle V_{KEY}$	V_{22} V_{21}	−60			mV
Peak Clamp Charge Resistance	R_{PEAK}	$\triangle V_{21}/\triangle I_{22}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Charge Resistance	R_{KEY}	$\triangle V_{21}/\triangle I_{22}$, $V_{21} < V_{22}$		150		ohm
Keyed Clamp Discharge Current	I_{KEY}	$V_{21} > V_{22}$		100		μA
Static Diff. Nonlinearity	SDNL1	F_{IN} = 1KHz CK = 1MHz		0.2		%

ELECTRICAL CHARACTERISTICS (Continued)

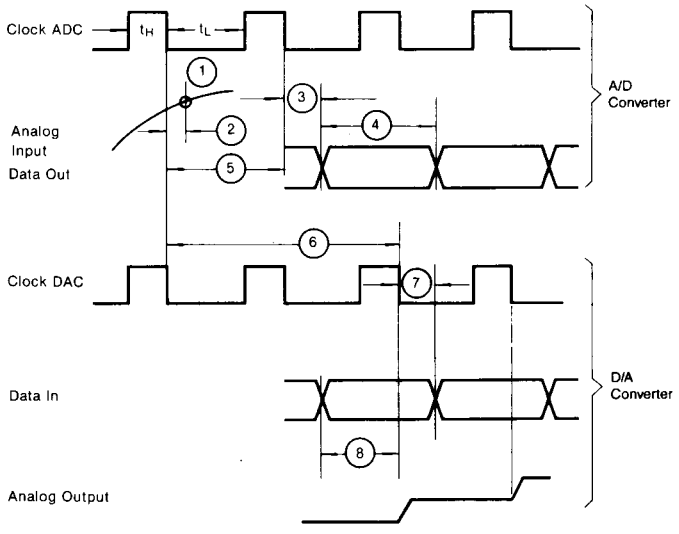
Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Dynamic Diff. Nonlinearity	DDNL	A_{IN} = 1.02MHz CK = 10MHz		0.3		%
		A_{IN} = 6.0018MHz CK = 25MHz (37.5% DUTY)			0.6	%
Dynamic Integral Nonlinearity	DINL	A_{IN} = 1.02MHz CK = 10MHz		0.8		%
Full Power Input Band Width	BW		6			MHz
Full Code Offset Error	E_{FULL}	(Full Code Input) – V_{REF}	0	+100	+200	mV
Zero Code Offset Error	E_{ZERO}	(Zero Code Input) – V_{REF}	–100	+40	+100	mV
Signal to Noise Ratio	SNR	A_{IN} = 1.02MHz CK = 10MHz		42		dB
(RMS Signal/RMS Noise)		A_{IN} = 1.02MHz CK = 20MHz		35		dB
		A_{IN} = 3.601MHz CK = 25MHz (37.5% DUTY)	30	34		dB
Differential Gain Error	DG	A_{IN} = 3.579545MHz CK = 14.318MHz	–1		3	%
Differential Phase Error	DP	A_{IN} = 3.579545MHz CK = 14.318MHz	–2		2	degree
D/A Converter						
Digital Input High Current	I_{DIH2}	V_{CC} = Max, V_{DIH2} = 2.4V			50	μA
Digital Input Low Current	I_{DIH2}	V_{CC} = Max, V_{DIL2} = 0.4V			–500	μA
External Input Bias Current	I_{38}	V_{CC} = Max, V_{38} = 3V			10	μA
External Input Capacitance	C_{38}			5		pF
External Input Equ. Resistance	R_{38}	F_{38} = 10KHz		1		Mohm
External Amp. Offset Error	E_{OFFSET}	V_{38} = –1V	–100		100	mV
External Amp. Gain Error	E_{GAIN}	{(V1/V38) – 1}*100	–5		5	%
Max. Data Conversion Rate	F_{DC}		20			MSPS
Analog Output Delay	t_D				25	ns
Settling Time	t_{SET}	settle to 0.2%			40	ns
Rising Time	t_R	10% to 90%			50	ns
Falling Time	t_F	90% to 10%			35	ns
Glitch Amplitude	G_A				80	mV
Glitch Duration	G_D				7	ns
Glitch Energy	G_E				250	pV-sec
Static Diff. Nonlinearity	SDNL2	KSV3110-10			0.05	%
		KSV3110-9			0.1	%
		KSV3110-8			0.2	%
Static Integral Nonlinearity	SINL				1	%
Full Scale Output Voltage	V_{FULL}	V_{CC} = typ, V_{EE} = typ	1.8		2.2	V
Zero Scale Output Voltage	V_{ZERO}	V_{CC} = typ, V_{EE} = typ	–60		+60	mV

MARKING SPECIFICATIONS (Ordering Information)

The KSV3110 has three versions according to the accuracy bit (so-called 'precision') of the D/A Converter, and their marking specifications are as follows:

Marking Spec.	D/A Converter		A/D Converter	Package	Temp. Range
	Accuracy Bit	Diff. Nonlinearity	Diff. Nonlinearity		
KSV3110-10	10-bit	0.05%	0.2%	40 DIP	0 ~ +70°C
KSV3110-9	9-bit	0.1%			
KSV3110-8	8-bit	0.2%			

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D
⑥ Total Transfer Time A/D-D/A with Common Clock
⑦ Input Register Hold Time
⑧ Input Register Setup Time

Fig. 3

PACKAGE LAYOUT

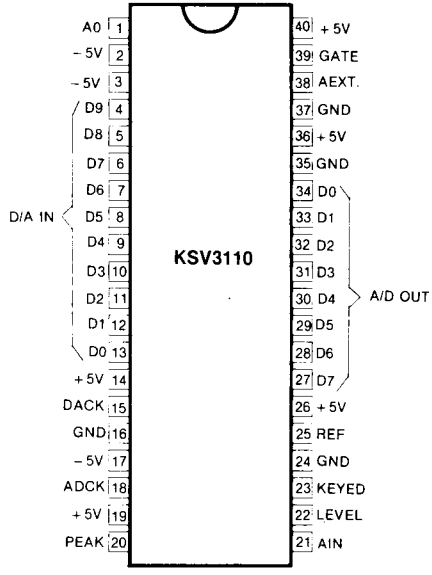


Fig. 4

DESCRIPTION OF THE CONNECTION AND THE SIGNALS

Pin No.	Description
Pin 1	Analog Output D/A Converter This pin, whose diagram is shown in Fig. 7, is the output for the processed analog signal either originating from the D/A converter or from the external analog input Pin 38.
Pin 2	−5-volt Supply D/A Converter, Analog This pin gets the negative supply for the analog part of the D/A converter
Pin 3	−5-volt Supply D/A Converter, Digital This pin gets the negative supply for the digital part of the D/A converter.
Pin 4 to 13	Digital Inputs Bit 9 to Bit 0 This diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter and not-used inputs should be connected to the ground.
Pin 14	+5-volt Supply D/A Converter, Digital This pin gets the positive supply for the digital part of the D/A converter.
Pin 15	Clock Input D/A Converter This pin, whose diagram is shown in Fig. 5, must be supplied with the clock signal for the D/A converter.
Pin 16	Ground D/A Converter and Clock A/D Converter This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.

DESCRIPTION OF THE CONNECTION AND THE SIGNALS (Continued)

Pin No.	Description
Pin 17	– 5-volt Supply A/D Converter, Analog This pin is the negative supply pin for the analog part of the A/D Converter.
Pin 18	Clock Input A/D Converter The diagram of this pin is shown in Fig. 5. Pin 18 is supplied with the clock of the A/D converter.
Pin 19	+ 5-volt Supply A/D Converter Via this pin the A/D converter gets its positive supply.
Pin 20	Peak Clamping Enable Input Via Pin 20, whose diagram is shown in Fig. 6, the peak clamping facility can be enabled.
Pin 21	Analog Input A/D Converter Fig. 7 is the diagram of this input. To Pin 21 is applied the analog signal to be converted into digital.
Pin 22	Clamping Level Input Via this pin, whose diagram is shown in Fig. 6, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Clamping Pulse Input Pin 23 must be supplied with the key pulse if keyed clamping is required.
Pin 24	Analog Ground A/D Converter This pin serves as the ground pin for the analog part of the A/D converter.
Pin 25	Reference-voltage A/D Converter This pin, whose diagram is shown in Fig. 8, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to Pin 37.
Pin 26	+ 5-volt Supply A/D Converter, Digital This pin is the positive supply pin for the digital part of the A/D converter.
Pin 27 to 34	Digital Outputs Bit 7 to Bit 0 Fig. 11 shows the diagram of these outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 35	Digital Ground A/D Converter This pin is the ground connection for the digital part of the A/D converter.
Pin 36	+ 5-volt Supply A/D Converter, Analog This pin is the positive supply pin for the analog part of the A/D converter.
Pin 37	Ground of Reference-voltage A/D Converter To this pin must be connected the ground end of the decoupling which is at Pin 25.
Pin 38	External Analog Input The diagram of this input is shown in Fig. 10. Pin 38 serves for feeding an external analog signal into the output amplifier of the KSV3110 instead of the D/A-converted signal originating from Pins 4 to 13.
Pin 39	Output Signal Switchover Input This pin, whose diagram is shown in Fig. 5, is intended for enabling the external analog signal fed to Pin 38.
Pin 40	+ 5-volt Supply Converter, Analog This pin is the negative supply pin for the analog parts of the D/A converter.

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

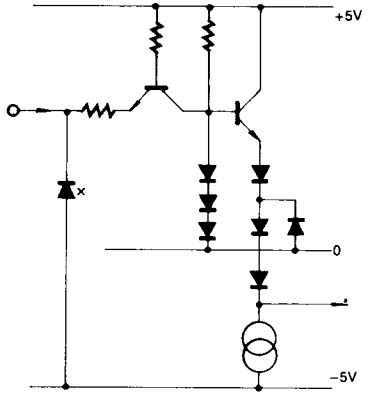


Fig. 5: Pins 4 to 13, 15, 18, 23 and 39, Inputs

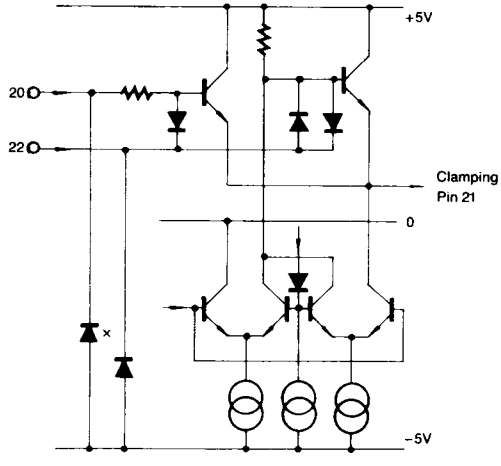


Fig. 6: Pins 20 and 22, Inputs

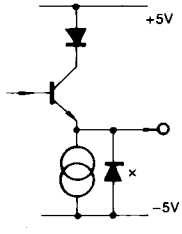


Fig. 7: Pin 1, Output

x = protection diode

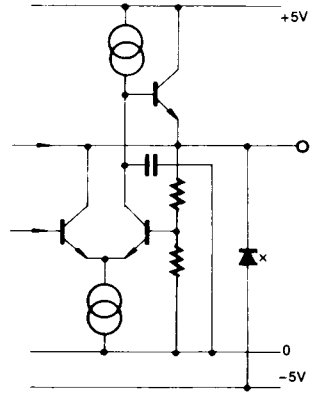


Fig. 8: Pin 25, Reference Voltage Pin

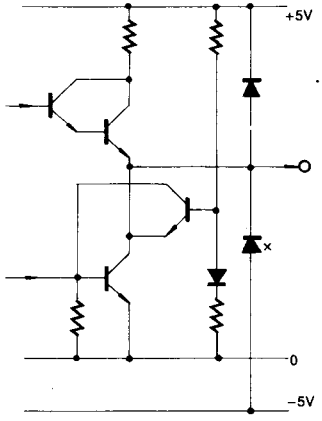


Fig. 9: Pins 27 to 34, Outputs

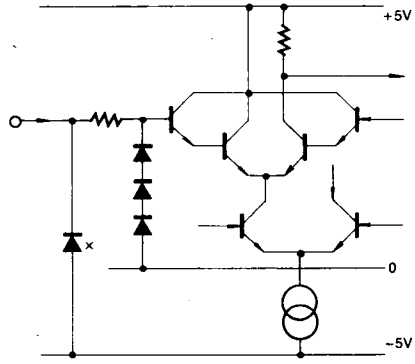


Fig. 10: Pin 38, Input
x = protection diode

RECOMMENDED APPLICATION CIRCUIT

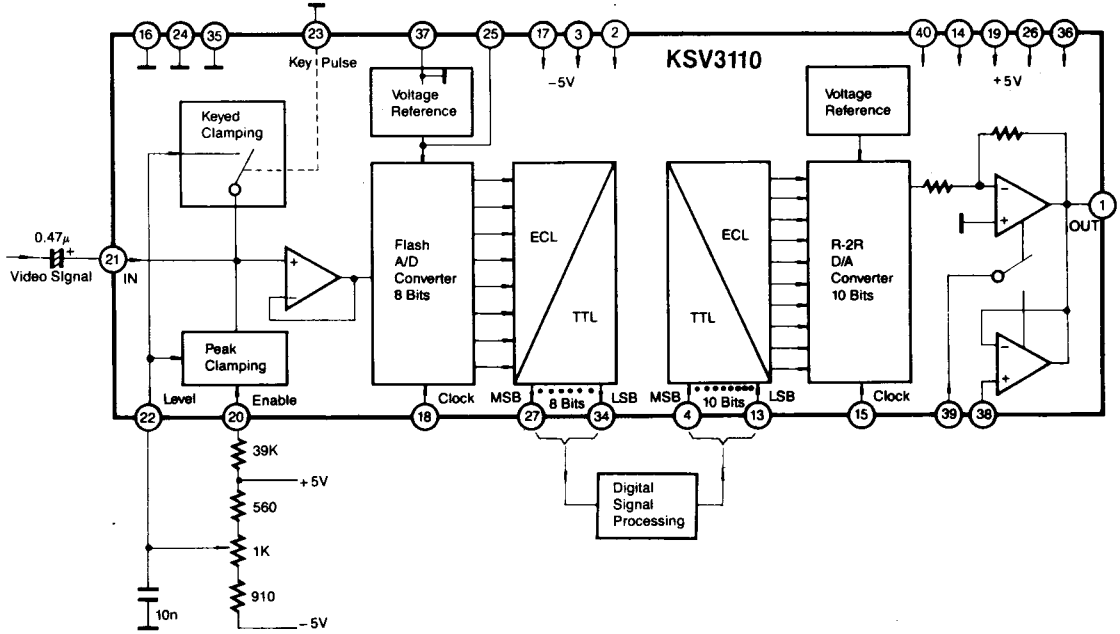


Fig. 11: Operation with peak clamping
The input signal is clamped automatically to the negative peak value. Pin 20 is connected to +5V via a 39KΩ resistor, and Pin 22 (clamping level input) is connected, as desired, to zero or a voltage between −1 and +2V. The input signal is fed to Pin 21 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

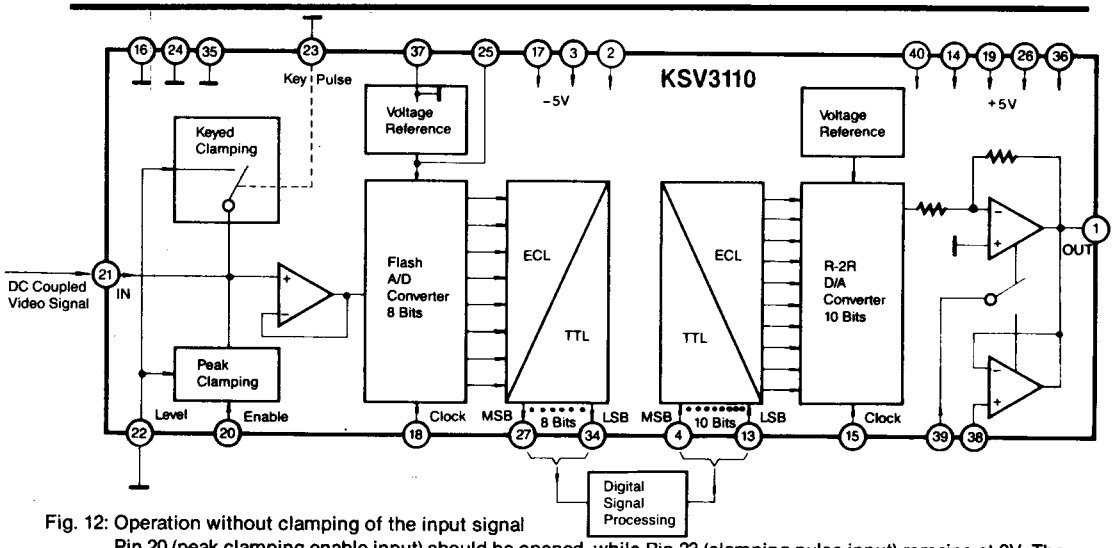


Fig. 12: Operation without clamping of the input signal
Pin 20 (peak clamping enable input) should be opened, while Pin 23 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, Pin 21, without a coupling capacitor such that it lies between 0 and + 2V.

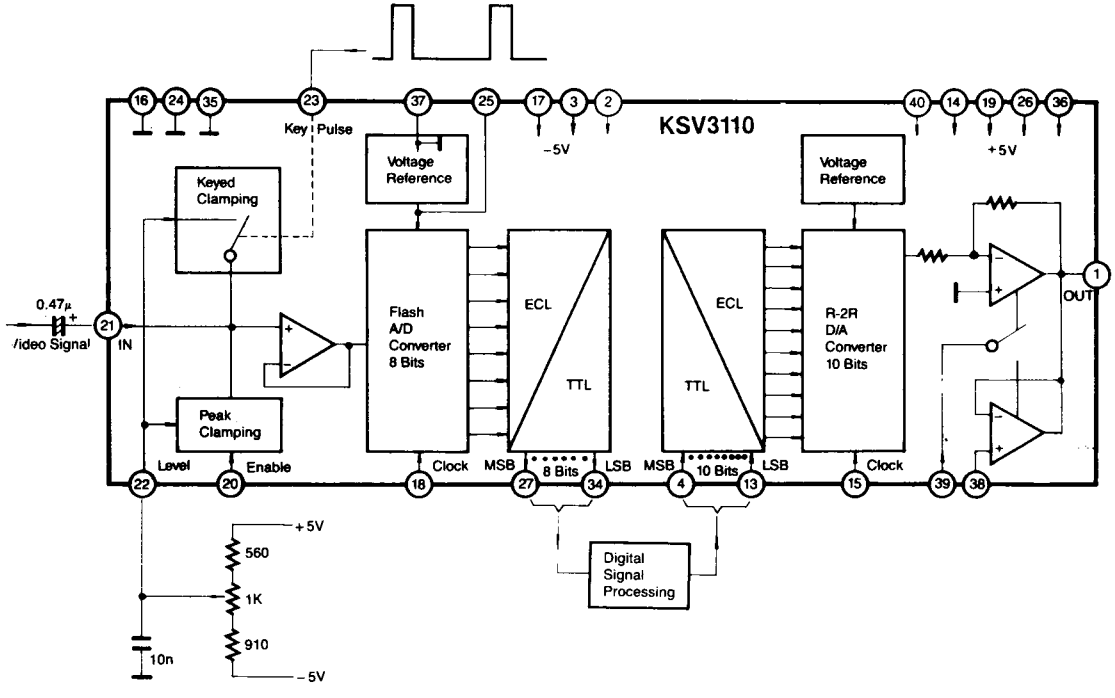


Fig. 13: Operation with keyed clamping
The input signal is applied to Pin 21 through a coupling capacitor. Pin 20 must not be connected. While the input signal is at the desired clamping level, a high-level is applied at the clamping pulse input, Pin 23. By this means the clamping switch in the KSV3110 connects the input with the clamping level at Pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between – 1 and + 2V.