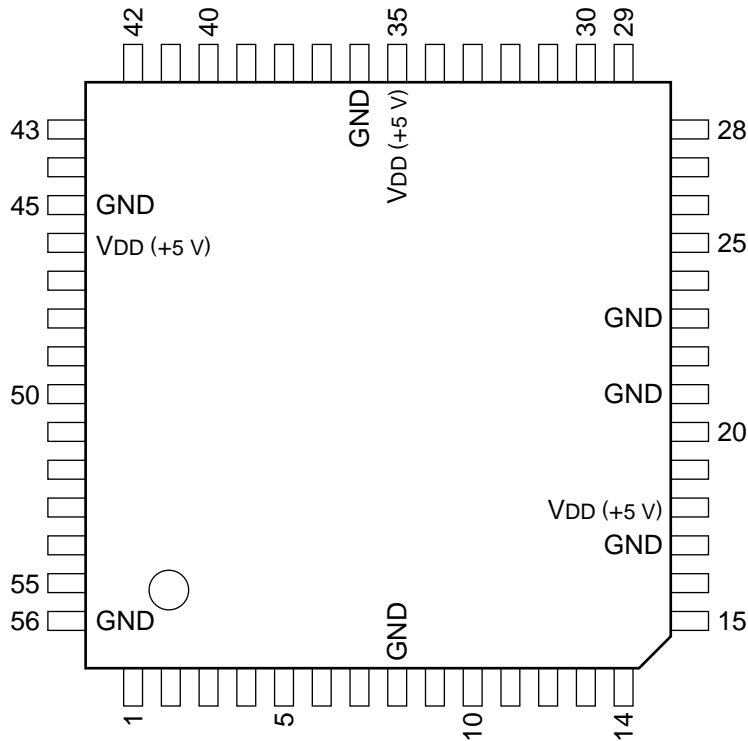


## C-MOS IEEE 1284 PERIPHERAL CONTROLLER

—TOP VIEW—

(V<sub>DD</sub> = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	B <i>Po</i> INT2	15	I/O	bD1	29	I	B <i>Pi</i> DEND1	43	I/O	B <i>Pb</i> D1
2	O	B <i>Po</i> INT1	16	I/O	bD0	30	I	B <i>Pi</i> DAK0	44	I/O	B <i>Pb</i> D0
3	O	B <i>Po</i> INT0	17	—	GND	31	O	B <i>Po</i>	45	—	GND
4	I	iA3	18	—	V <sub>DD</sub>	32	O	B <i>Po</i> DEND0	46	—	V <sub>DD</sub>
5	I	iA2	19	I	iRD/RW	33	I	B <i>Pi</i> CLS	47	I	B <i>Pi</i> SEI
6	I	iA1	20	I	iWR/EN	34	O	B <i>Po</i> RT	48	I	B <i>Pi</i> AF
7	I	iA0	21	—	GND	35	—	V <sub>DD</sub>	49	I	B <i>Pi</i> INI
8	—	GND	22	I	B <i>Pi</i> CLK	36	—	GND	50	I	B <i>Pi</i> STB
9	I/O	bD7	23	—	GND	37	I/O	B <i>Pb</i> D7	51	O	B <i>Po</i> PE
10	I/O	bD6	24	I	iRST	38	I/O	B <i>Pb</i> D6	52	O	B <i>Po</i> ACK
11	I/O	bD5	25	I	iCIS	39	I/O	B <i>Pb</i> D5	53	O	B <i>Po</i> BY
12	I/O	bD4	26	I	iCS	40	I/O	B <i>Pb</i> D4	54	O	B <i>Po</i> FT
13	I/O	bD3	27	I	B <i>Pi</i> DAK1	41	I/O	B <i>Pb</i> D3	55	O	B <i>Po</i> SE
14	I/O	bD2	28	O	B <i>Po</i> DRQ1	42	I/O	B <i>Pb</i> D2	56	—	GND

**INPUT**

$\overline{\text{BPiAF}}$	: COMPATIBILITY = n AUTO Fd
$\text{BPiCLK}$	: CLOCK
$\text{BPiCLS}$	: COMPATIBILITY MODE LEVEL SELECT
$\overline{\text{BPiDAK0}}$	: DMA ACKNOWLEDGE0
$\overline{\text{BPiDAK1}}$	: DMA ACKNOWLEDGE1
$\overline{\text{BPiDEND1}}$	: DMA END1
$\overline{\text{BPiINI}}$	: COMPATIBILITY = n INITIAL
$\overline{\text{BPiSEI}}$	: COMPATIBILITY = n SELECT IN
$\overline{\text{BPiSTB}}$	: COMPATIBILITY = n STROBE
iA0 - iA3	: ADDRESS
iCIS	: CPU INTERFACE SELECT
$\overline{\text{iCS}}$	: CHIP SELECT
$\overline{\text{iRD}}/\overline{\text{WR}}$	: READ/READ WRITE SELECT
$\overline{\text{iRST}}$	: RESET
$\overline{\text{iWR}}/\overline{\text{EN}}$	: WRITE/ENABLE

**OUTPUT**

$\text{BPoACK}$	: COMPATIBILITY = n ACK
$\text{BPoBY}$	: COMPATIBILITY = BUSY
$\overline{\text{BPoDEND0}}$	: DMA END0
$\overline{\text{BPoDRQ0}}$	: DMA REQUEST0
$\overline{\text{BPoDRQ1}}$	: DMA REQUEST1
$\overline{\text{BPoFT}}$	: COMPATIBILITY = n FAULT
$\overline{\text{BPoINT0}}$	: INTERRUPT REQUEST0
$\overline{\text{BPoINT1}}$	: INTERRUPT REQUEST1
$\overline{\text{BPoINT2}}$	: INTERRUPT REQUEST2
$\text{BPoPE}$	: COMPATIBILITY = P ERROR
$\text{BPoRT}$	: INDICATE REVERSE TRANSFER
$\text{BPoSE}$	: COMPATIBILITY = SELECT

**INPUT/OUTPUT**

bD0 - bD7	: DATA BUS
BPbD0 - BPbD7	: COMPATIBILITY = DATA

