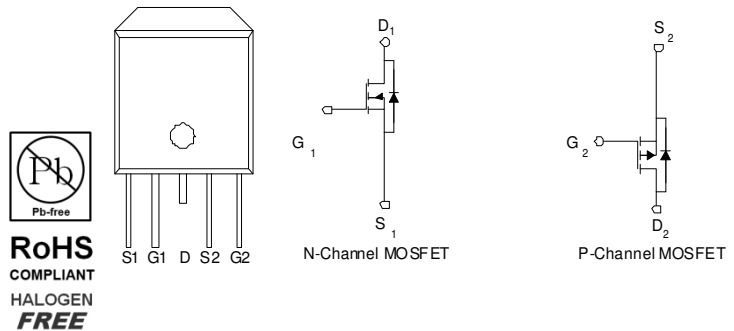


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	39 @ $V_{GS} = 4.5V$	30
	29 @ $V_{GS} = 10V$	36
-30	29 @ $V_{GS} = -4.5V$	-36
	22 @ $V_{GS} = -10V$	39



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	36	-39	A
	$T_A = 70^\circ C$		30	-32	
Pulsed Drain Current ^b		I_{DM}	40	-40	
Continuous Source Current (Diode Conduction) ^a		I_S	30	-30	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	50	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175		$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

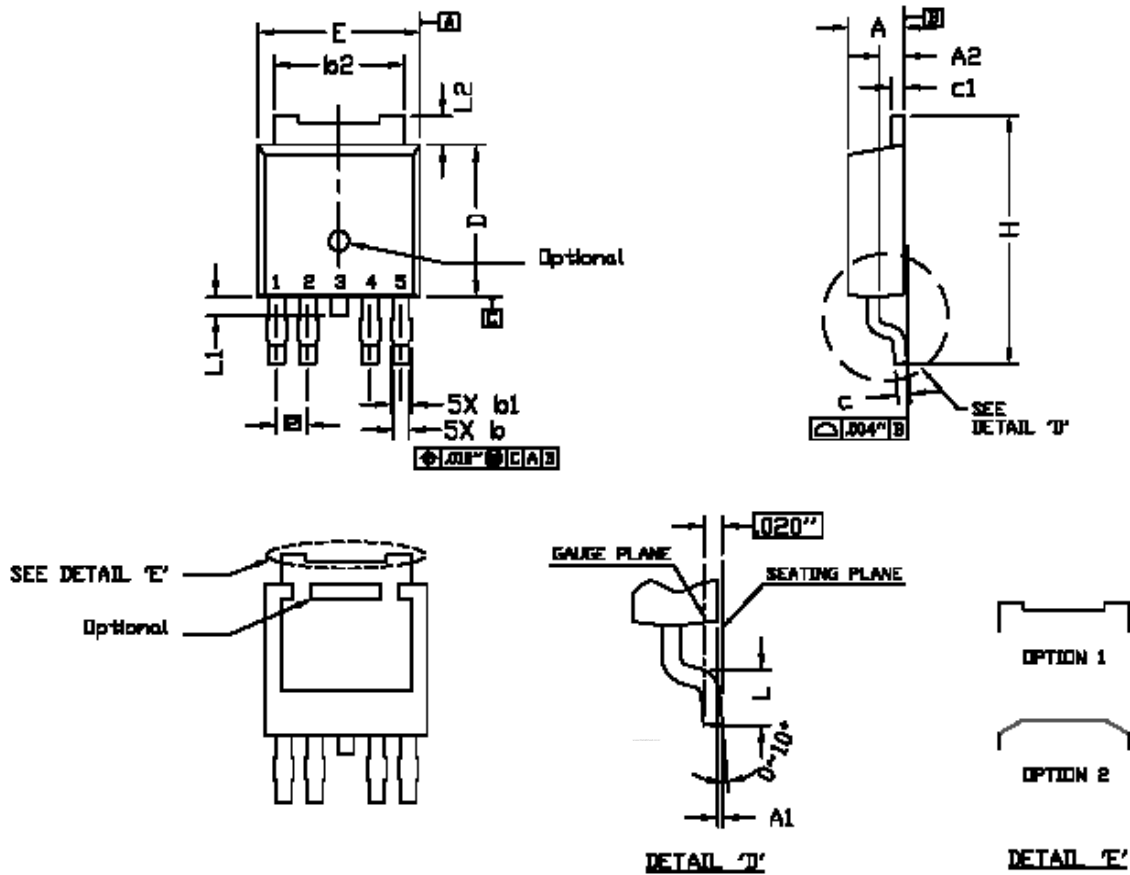
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	0.6			V
		V _{GS} = V _{DS} , I _D = -250 uA	P	-0.6			
Gate-Body Leakage	I _{CSS}	V _{GS} = -20 V, V _{DS} = 0 V	P			±100	nA
		V _{GS} = 20 V, V _{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V	P			-1	uA
		V _{DS} = 24 V, V _{GS} = 0 V	N			1	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	20			A
		V _{DS} = -5 V, V _{GS} = -10 V	P	-20			
Drain-Source On-Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 6.9 A	N			29	mΩ
		V _{GS} = 4.5 V, I _D = 6 A				39	
		V _{GS} = -10 V, I _D = -5.2 A	P			22	
		V _{GS} = -4.5 V, I _D = -4.2 A				29	
Forward Transconductance ^a	g _s	V _{DS} = 15 V, I _D = 6.9 A	N		25		S
		V _{DS} = -15 V, I _D = -5.2 A	P		10		
Dynamic							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =10V, I _D =6.9A P-Channel V _{DS} =-15V, V _{GS} =-10V, I _D =-5.2A	N		6.0		nC
			P		10		
Gate-Source Charge	Q _{gs}		N		1.0		
			P		2.4		
Gate-Drain Charge	Q _{gd}		N		1.5		
			P		3.9		
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DS} =15V, V _{GS} =10V, I _D =1A , R _{GEN} =6Ω, P-Channel V _{DD} =-15V, V _{GS} =-10V, I _D =-1A R _{GEN} =6Ω	N		7.4		nS
			P		7.6		
Rise Time	t _r		N		4		
			P		6.8		
Turn-Off Delay Time	t _{d(off)}		N		22.2		
			P		33.6		
Fall-Time	t _f		N		3.6		
			P		23.2		

Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

TO252_4L PACKAGE OUTLINE



- NOTE**
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
 2. DIMENSION L IS MEASURED IN GAUGE PLANE.
 3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED.
 4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
 5. REFER TO JEDEC TO-252 (AD).

SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.288	2.388	0.086	0.090	0.094
A1	0.000	—	0.127	0.000	—	0.005
A2	0.889	—	1.143	0.035	—	0.045
b	0.508	—	0.711	0.020	—	0.028
b1	0.584	—	0.787	0.023	—	0.031
b2	4.953	—	5.461	0.195	—	0.215
c	0.457	0.508	0.610	0.018	0.020	0.024
c1	0.457	—	0.610	0.018	—	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
E	6.350	6.604	6.731	0.250	0.260	0.265
e	1.270 BSC.			0.050 BSC.		
H	9.398	—	10.414	0.370	—	0.410
L	1.270	—	2.032	0.050	—	0.080
L1	—	—	1.018	—	—	0.040
L2	0.889	—	1.270	0.035	—	0.050