SONY

High Power DPDT Switch with Logic Control

CXG1188UR

Description

The CXG1188UR can be used in wireless communication systems, for example, CDMA handsets with GPS.
The IC has on-chip logic for operation with 1 CMOS control input.
The Sony J-FET process is used for low insertion loss and on-chip logic circuit.
(Applications: Dual-band cellular handsets, CDMA with GPS, dual-band CDMA)

Features

- ◆ Low insertion loss: 0.30dB@900MHz, 0.45dB@1900MHz
- ◆ High linearity: IIP3 = 65dBm (Typ.)
- ◆ 1 CMOS compatible control line

Package

Small package size: 12-pin UQFN

Structure

GaAs J-FET MMIC

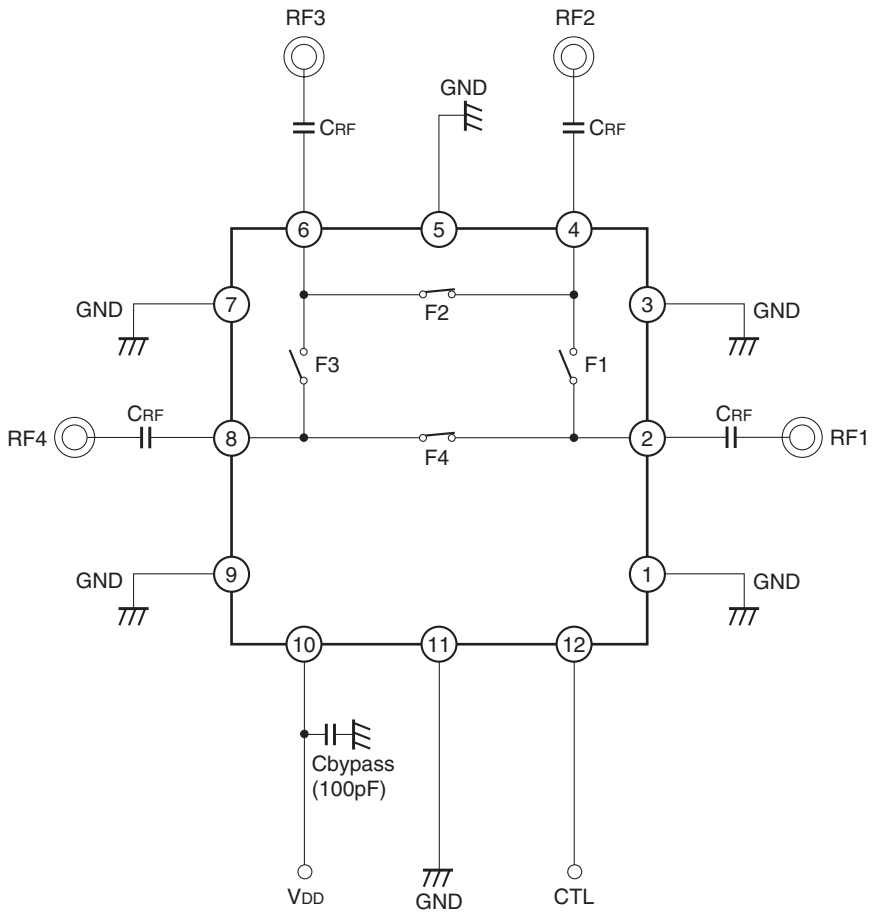
Absolute Maximum Ratings

(Ta = 25˚C)

◆ Bias voltage	V_{DD}	7	V
◆ Control voltage	Vctl	5	V
◆ Operation temperature	Topr	–35 to +85	˚C
◆ Storage temperature	Tstg	–65 to +150	˚C

This IC is ESD sensitive device. Special handling precautions are required.

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

C_{RF}: This capacitor is used for RF decoupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

CTL	ON state	OFF state	F1	F2	F3	F4
L	RF1 – RF2, RF3 – RF4	RF2 – RF3, RF4 – RF1	ON	OFF	ON	OFF
H	RF2 – RF3, RF4 – RF1	RF1 – RF2, RF3 – RF4	OFF	ON	OFF	ON

DC Bias Conditions

(Ta = 25℃)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	3.0	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.7	3.0	3.6	V

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	900MHz		0.30	0.55	dB
		1.9GHz		0.45	0.70	dB
Isolation	ISO.	900MHz	18	21		dB
		1.9GHz	14	16		dB
VSWR	VSWR	50Ω		1.2		—
Harmonics	2fo	*1		–75	–60	dBc
		*3		–75	–60	dBc
	3fo	*1		–75	–60	dBc
		*3		–75	–60	dBc
Input IP3	IIP3	*2	55	65		dBm
		*4	55	65		dBm
1dB compression input power	P1dB	V_{DD} = 2.8V	32	35		dBm
Switching speed	TSW			1	5	μs
Bias current	I_{DD}	V_{DD} = 3.0V		55	130	μA
Control current	Ictl	Vctl (H) = 3.0V		40	100	μA

*1 Pin = 25dBm, 0/3V control, V_{DD} = 3.0V, 900MHz

*2 Pin = 25dBm (900MHz) + 25dBm (901MHz), 0/3V control, V_{DD} = 3.0V

*3 Pin = 25dBm, 0/3V control, V_{DD} = 3.0V, 1.9GHz

*4 Pin = 25dBm (1.9GHz) + 25dBm (1.901GHz), 0/3V control, V_{DD} = 3.0V

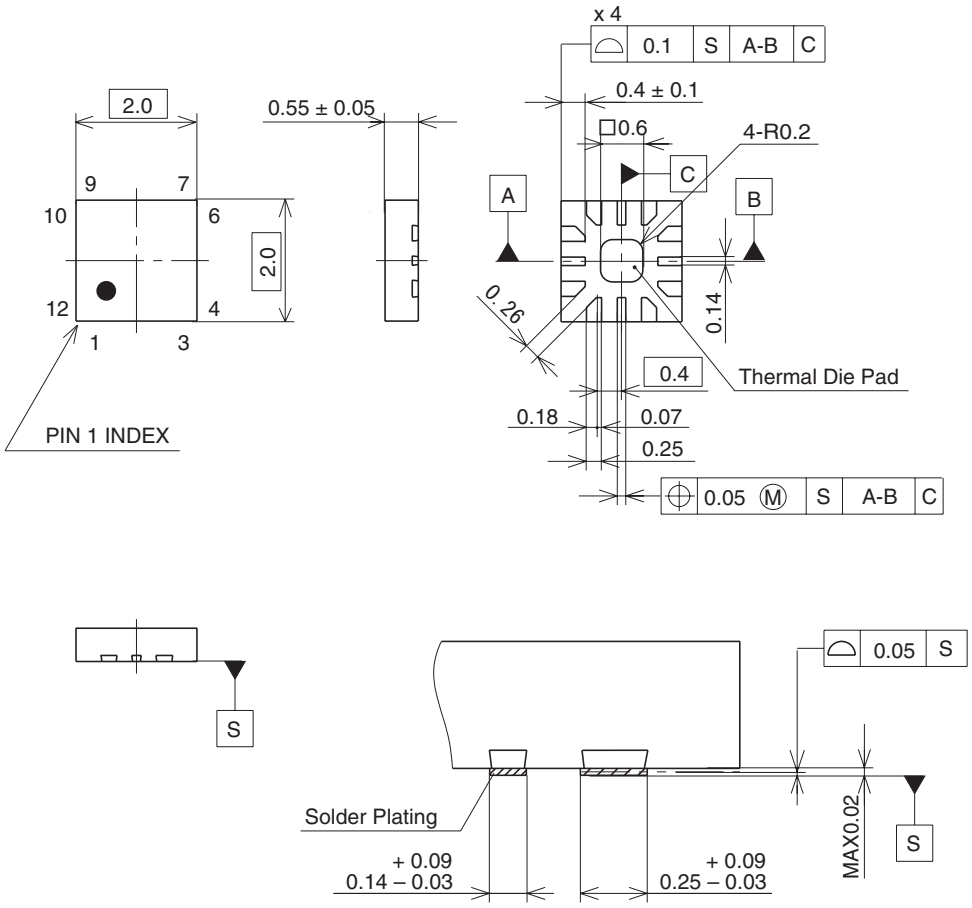
Pin Description

Pin No.	Symbol	Description
1	GND	Control signal input
2	RF1	RF signal input
3	GND	GND
4	RF2	RF signal output
5	GND	GND
6	RF3	RF signal input
7	GND	GND
8	RF4	RF signal output
9	GND	GND
10	V_{DD}	Power supply input
11	GND	GND
12	CTL	Control signal input

Package Outline

(Unit: mm)

12PIN UQFN（PLASTIC）



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-12P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm