

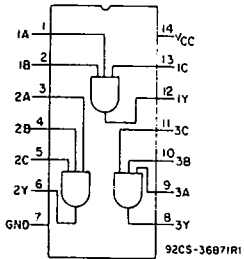
CD54/74HC11
CD54/74HCT11

File Number 1475

HARRIS SEMICONDUCTOR

27E D ■ 430227J 0017479 2 ■ HAS

High-Speed CMOS Logic



Triple 3-Input AND Gate

Type Features:

- Buffered inputs
- Typical propagation delay = 8 ns @ $V_{CC} = 5 V$, $C_L = 15 pF$, $T_A = 25^\circ C$

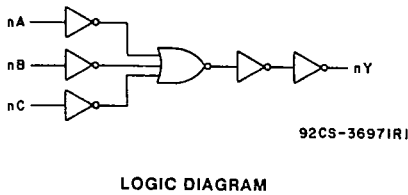
FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

The RCA-CD54/74HC11 and CD54/74HCT11 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC11 and CD54HCT11 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC11 and CD74HCT11 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Phillips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL}=30\%$, $N_{IH}=30\%$ of V_{CC}
@ $V_{CC}=5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL}=0.8 V$ Max., $V_{IH}=2 V$ Min.
CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}



LOGIC DIAGRAM

TRUTH TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{cc}):
(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5V$ OR $V_i > V_{cc} + 0.5V$) ± 20 mA

DC OUTPUT CURRENT, I_{OK} (FOR $V_o < -0.5V$ OR $V_o > V_{cc} + 0.5V$) ± 20 mA

DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR $-0.5V < V_o < V_{cc} + 0.5V$) ± 25 mA

DC V_{cc} OR GROUND CURRENT, (I_{cc}): ± 50 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ C$ (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ C$ (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ C$ to 300 mW

For $T_A = -55$ to $+100^\circ C$ (PACKAGE TYPE F, H) 500 mW

For $T_A = +100$ to $+125^\circ C$ (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ C$ to 300 mW

For $T_A = -40$ to $+70^\circ C$ (PACKAGE TYPE M) 400 mW

For $T_A = +70$ to $+125^\circ C$ (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ C$ to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to $+125^\circ C$

PACKAGE TYPE E, M -40 to $+85^\circ C$

STORAGE TEMPERATURE (T_{stg}) -65 to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ C$

Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only $+300^\circ C$

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package Temperature Range) V_{cc} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{cc}	V
Operating Temperature T_A :			
CD74 Types	-40	+85	$^\circ C$
CD54 Types	-55	+125	$^\circ C$
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC11
CD54/74HCT11

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC11/CD54HC11										CD74HCT11/CD54HCT11										UNITS			
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES			54HC TYPES			TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES				54HCT TYPES		
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C			-55/ +125°C			V _i V	V _{cc} V	+25°C			-40/ +85°C				-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max				
High-Level Input Voltage V _{ih}			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5	to	2	—	—	2	—	2	—	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	—	5.5											
			6	4.2	—	—	4.2	—	4.2	—	—	—												
Low-Level Input Voltage V _{il}			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5	to	—	—	0.8	—	0.8	—	0.8	—	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	5.5											
			6	—	—	1.8	—	1.8	—	1.8	—	—												
High-Level Output Voltage V _{oh}	V _{ih}	-0.02	2	1.9	—	—	1.9	—	1.9	—	—	V _{ih}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V	
or			4.5	4.4	—	—	4.4	—	4.4	—	—	or	5.5											
CMOS Loads	V _{ih}		6	5.9	—	—	5.9	—	5.9	—	—	V _{ih}												
TTL Loads	V _{ih}										V _{ih}													
	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	—	—	V		
	V _{ih}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V _{ih}													
Low-Level Output Voltage V _{ol}	V _{ih}	0.02	2	—	—	0.1	—	0.1	—	0.1	—	V _{ih}	4.5	—	—	0.1	—	0.1	—	0.1	—	V		
or			4.5	—	—	0.1	—	0.1	—	0.1	—	or	5.5											
CMOS Loads	V _{ih}		6	—	—	0.1	—	0.1	—	0.1	—	V _{ih}												
TTL Loads	V _{ih}										V _{ih}													
	or	4	4.5	—	—	0.26	—	0.33	—	0.4	—	or	4.5	—	—	0.26	—	0.33	—	0.4	—	V		
	V _{ih}	5.2	6	—	—	0.26	—	0.33	—	0.4	—	V _{ih}												
Input Leakage Current I _i	V _{cc}		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	μA		
or	Gnd																							
Quiescent Device Current I _{cc}	V _{cc}	0	6	—	—	2	—	20	—	40	—	V _{cc}	5.5	—	—	2	—	20	—	40	—	μA		
or	Gnd											or												
Additional Quiescent Device Current per input pin, 1 unit load ΔI _{cc}												V _{cc} -2.1	4.5	to	—	100	360	—	450	—	490	μA		
													5.5											

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ALL	0.50

*Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC11 CD54/74HCT11

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r, t_f = 6 \text{ ns}$)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Input to Output (Fig. 1)	t_{PLH}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
	t_{PHL}	4.5	—	20	—	28	—	25	—	35	—	30	—	42	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Transition Times (Fig. 1)	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_i		—	10	—	10	—	10	—	10	—	10	—	10	pF

SWITCHING CHARACTERISTICS ($V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$, Input $t_r, t_f = 6 \text{ ns}$)

CHARACTERISTIC	SYMBOL	Typical		Units
		HC	HCT	
Propagation Delay, Data Input to Output Y (Fig. 1) ($C_L = 15 \text{ pF}$)	t_{PLH} t_{PHL}	8	11	ns
Power Dissipation Capacitance*	C_{PD}	26	28	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.
 $PD = V_{CC}^2 f (C_{PD} + C_L)$ where f = input frequency

C_L = output load capacitance
 V_{CC} = supply voltage

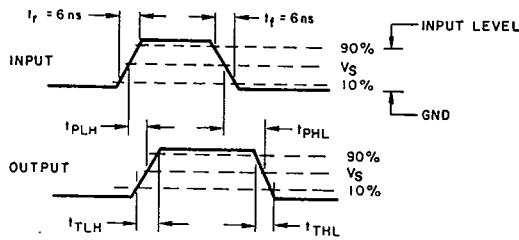


Fig. 1 — Transition times and propagation delay times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

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