FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC21 OR DATA SHEET

1. FEATURES

- CHMOS technology
- 32-bit internal structure
- Maximum internal clock frequency: 15 MHz
- 8 programmable interrupt inputs
- Choice of on-chip memory (RAM, ROM and EPROM)
- Built-in clock generators - maximum 30 MHz crystal
- Reset control circuitry
- On-chip address decoder
- 16-bit input/output General Purpose Port
- 8-bit input/output Auxiliary Port
- 16-bit input/output Secondary Port
- I²C serial bus interface
- UART serial interface
- 16-bit timer/counter
- Two 16-bit match/count/capture registers
- Full 68000 software compatibility
- 68000-compatible bus interface
- 56 powerful instruction types
- 5 basic data types
- 2 M byte addressing range
- 14 addressing modes
- Memory-mapped I/O
- Auto-vectored interrupts
- 7 interrupt levels
- Reduced power modes
- 80C51 bus interface compatible
- 84-pin PLCC or 80-pin QFP package
- Supply voltage of 3.3 to 6.0 V (9xC101 only)

2. GENERAL DESCRIPTION

This document gives an overview of the basic functions, internal structure and electrical characteristics of the P9xC1xx family of microcontrollers. The family comprises the 90C100, 93C100, 97C100; 90C101 and the 93C101 in this data sheet the term 90C100 refers to any one of the family members. The 90C100 is a highly integrated 16/32-bit microcontroller for use in a large variety of applications and is fully software compatible with the 68000. By integrating standard as well as advanced peripheral functions on the 90C100, system costs are dramatically reduced.

The internal architecture of the 90C100 is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The 90C100 has powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a 15 MHz clock signal for CPU and peripheral interfaces.

The I²C-bus interface allows easy and low-cost addition of peripherals (master and slave devices). The 90C100 also includes a UART interface. Expansion of memory (up to 2 M bytes) and catering for additional peripherals is possible using dedicated 8051 and 68000 compatible buses. A built-in timer/counter with two independently programmable match/count/capture registers means that the 90C100 can be programmed with any two of the following options simultaneously:

- pulse generator
- external event counter
- reference timer

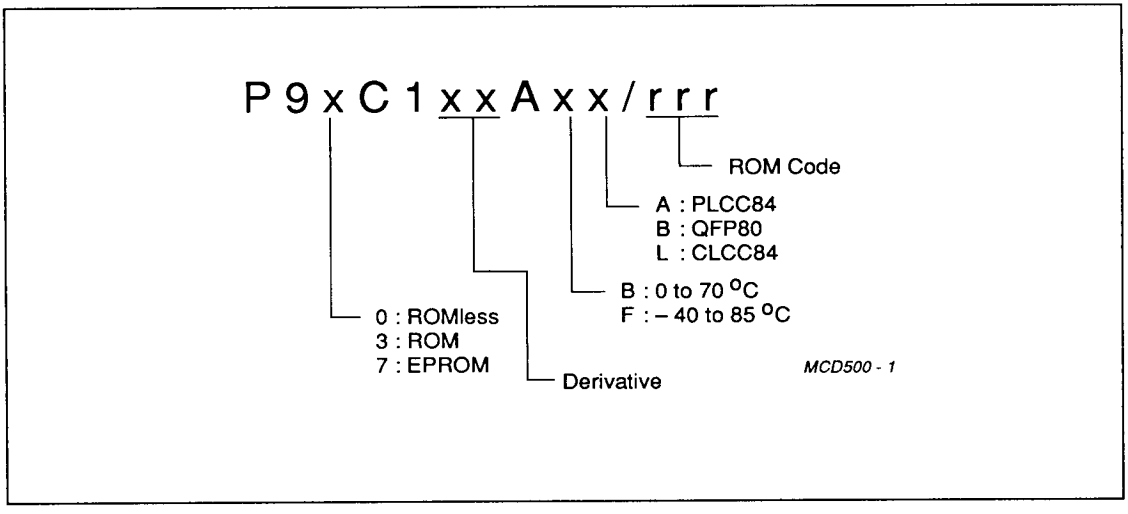
A choice of memory configurations is possible with this family of microcontrollers; these are shown in Table 1. A total of 40 input/output pins are available having standard or quasi-bidirectional features.

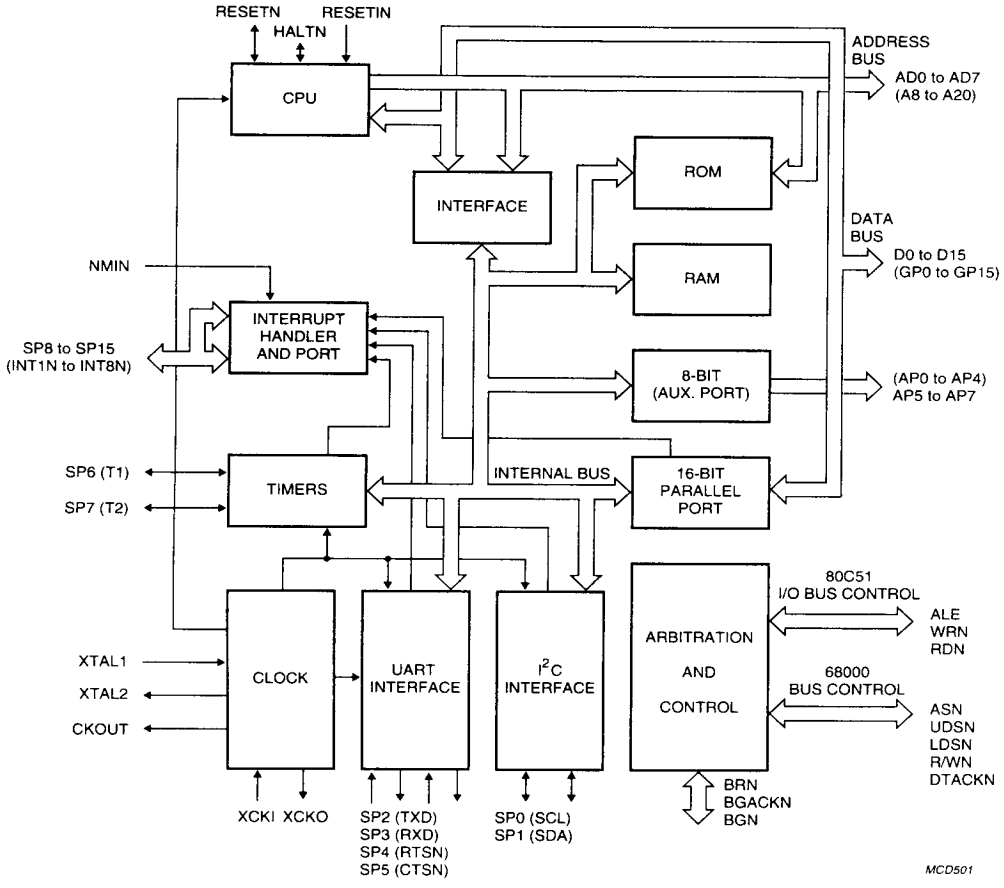
Table 1 Memory configurations

DEVICE	RAM	ROM	EPROM
90C100	512 bytes	–	–
93C100	512 bytes	34 K bytes	–
97C100	512 bytes	–	32 K bytes
90C101	512 bytes	–	–
93C101	512 bytes	34 K bytes	–

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	MATERIAL	CODE	
P90C100ABA	84	PLCC	plastic	SOT189	0 to 70
P90C100ABB	80	QFP	plastic	SOT318	0 to 70
P90C100AFA	84	PLCC	plastic	SOT189	–40 to 85
P90C100AFB	80	QFP	plastic	SOT318	–40 to 85
P93C100ABA	84	PLCC	plastic	SOT189	0 to 70
P93C100ABB	80	QFP	plastic	SOT318	0 to 70
P93C100AFA	84	PLCC	plastic	SOT189	–40 to 85
P93C100AFB	80	QFP	plastic	SOT318	–40 to 85
P97C100ABA	84	PLCC	plastic	SOT189	0 to 70
P97C100AFA	84	PLCC	plastic	SOT189	–40 to 85
P97C100ABL	84	CLCC	ceramic	NO331B	0 to 70
P97C100AFL	84	CLCC	ceramic	NO331B	–40 to 85
P90C101ABA	84	PLCC	plastic	SOT189	0 to 70
P90C101ABB	80	QFP	plastic	SOT318	0 to 70
P90C101AFA	84	PLCC	plastic	SOT189	–40 to 85
P90C101AFB	80	QFP	plastic	SOT318	–40 to 85
P93C101ABA	84	PLCC	plastic	SOT189	0 to 70
P93C101ABB	80	QFP	plastic	SOT318	0 to 70
P93C101AFA	84	PLCC	plastic	SOT189	–40 to 85
P93C101AFB	80	QFP	plastic	SOT318	–40 to 85





1. AP7, BGACKN, BRN and BGN not available with the QFP80 package.

Fig.1 Block diagram.

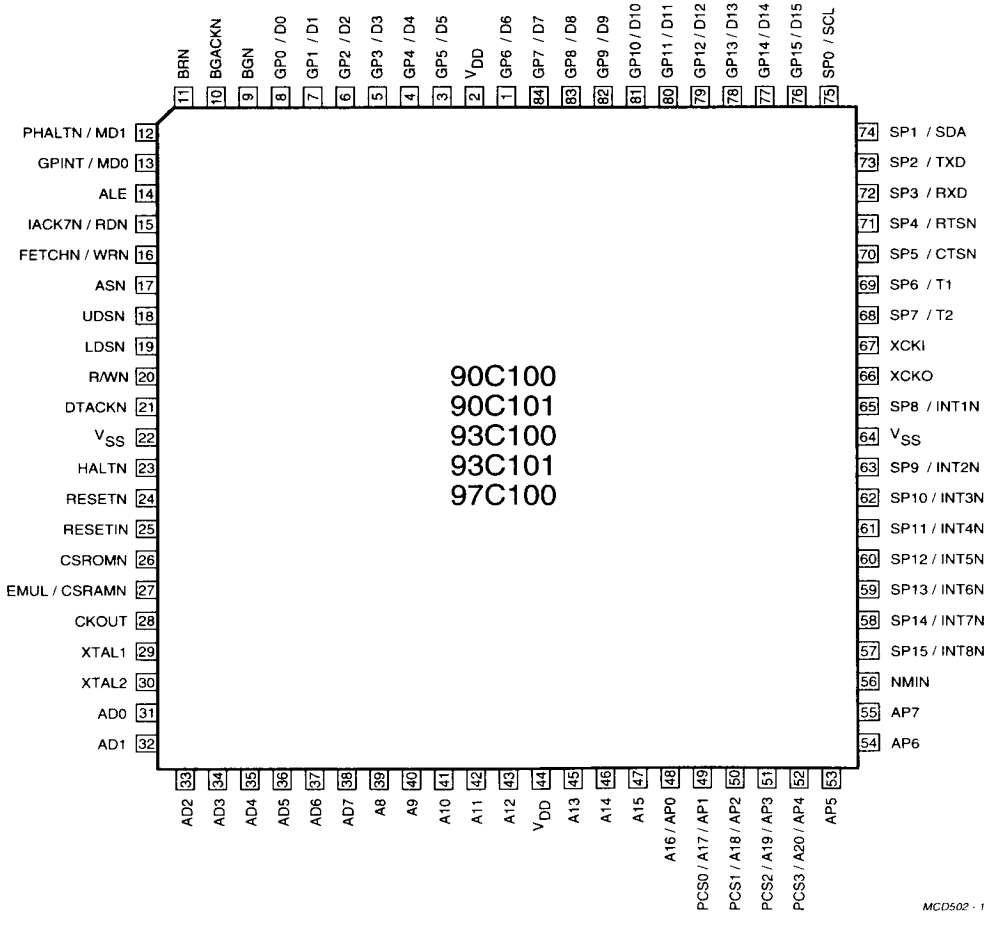


Fig.2 Pinning diagram for PLCC84.

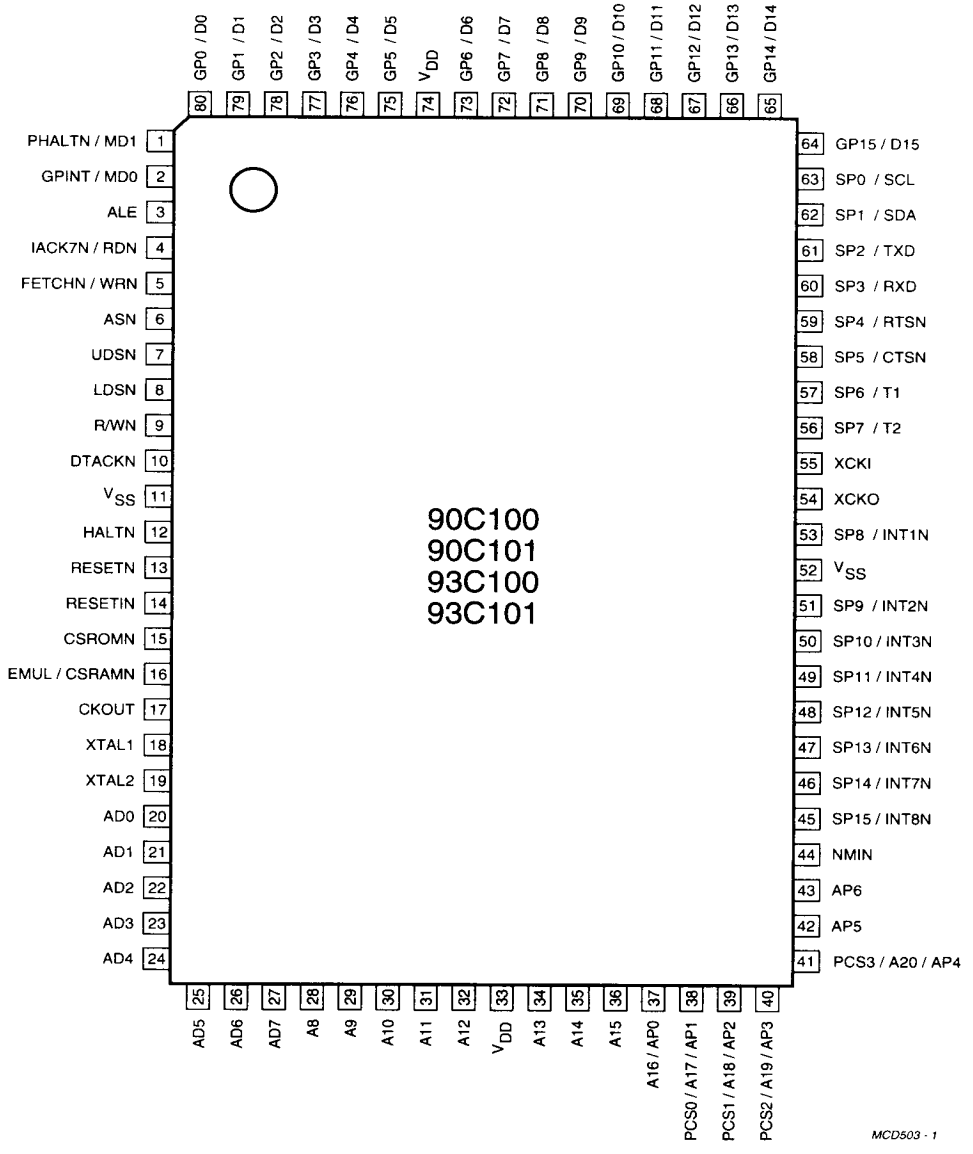


Fig.3 Pinning diagram for QFP80.

4. SIGNAL DESCRIPTION

MNEMONIC	TYPE	PLCC84	QFP80	FUNCTION
AD0 to AD7	I/O	31-38	20–27	**Address/Data bus** (active HIGH, 3-state). Multiplexed bus for peripheral extension (8051), these are the LSBs for the address bus during memory extension cycles (68000).
A8 to A15	O	39-43, 45-47	28–32, 34–36	**Address lines** (active HIGH, 3-state). Used as the MSBs for peripheral extension cycles and as the middle part of address bus for memory extension cycles.
AP0 to AP4 (A16 to A20) (PCS0 to PCS3)	I/O	48-52	37–41	**Auxiliary I/O port**. Either the MSBs of the address in Memory extension cycles or Chip selects.
GP0 to GP15 (D0 to D15)	I/O	8-3 1, 84-76	80–75, 73–64	**General Purpose port** (active HIGH, 3-state). Alternative function 16-bit bidirectional Data bus for the 68000 memory.
ASN	O	17	6	**Address Strobe** (active LOW, 3-state). Indicates a valid address on the bus.
LDSN	O	19	8	**Lower Data Strobe** (active LOW, 3-state). For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
UDSN	O	18	7	**Upper Data Strobe** (active LOW, 3-state). For a WRITE cycle, the data is valid on the upper half of the data bus (D8 to D15). For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
R/WN	O	20	9	**Read** (active HIGH)/**Write** (active LOW, 3-state). Controls the direction of the data flow of the memory bus cycle.
DTACKN	I	21	10	**Data Transfer Acknowledge** (active LOW). Asserted by the peripheral during CPU bus cycles when data is either received from or placed on the bus. If not asserted punctually it causes the CPU to insert wait states.
BRN	I	11	n.a.	**Bus Request** (active LOW). Asserted by wire-ORed external DMA devices that request bus ownership. (PLCC package only). See note 1.
BGN	O	9	n.a.	**Bus Grant** (active LOW). A daisy chain output which is asserted by the 90C100 when the bus is granted by the CPU. (PLCC package only).
BGACKN	I/O	10	n.a.	**Bus Grant Acknowledge** (active LOW, open drain). Asserted by any external DMA device that has control of the bus or by the internal 80C51 bus controller. As long as this line is held LOW externally, the 90C100 will hold the bus signals in the high impedance state. When BGACKN is released, the 90C100 will have access to the bus. (PLCC package only). See note 1.
RESETN	I/O	24	13	**Reset** (active LOW, open drain, bidirectional). If asserted externally together with the HALTN line, it will cause the processor to enter the Reset state. It is driven LOW by the processor when the Reset instruction resets external hardware or on-chip peripherals. See note 1.

MNEMONIC	TYPE	PLCC84	QFP80	FUNCTION
HALTN	I/O	23	12	**Halt** (active LOW, open drain, bidirectional). If asserted externally together with RESETN, it causes the 90C100 to enter the Reset state. If asserted alone, it will cause the CPU to stop after completion of the current bus cycle. As long as HALTN is held LOW, all control signals are inactive (except BGACKN) and all 3-state lines are placed in the high-impedance state. When the processor has stopped executing instructions (e.g. after a double bus fault), the processor drives this line LOW. See note 1.
NMIN	I	56	44	**Non-Maskable Interrupt (level 7)** (active LOW). While the other interrupts may be masked (disabled), this interrupt is always enabled. The LOW level must be maintained until the interrupt acknowledge cycle is performed.
SP8 to SP15 (INT1N to INT8N)	I/O	65, 63-57	53, 51–45	**Latched Interrupt Inputs** (active LOW). A LOW level for ≥ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable. These 8-bits may also be used as an Input/Output port. See note 1.
RESETIN	I	25	14	**Reset Input Line** (active HIGH). Connected to an external capacitor in order to provide the correct reset sequence at power-up.
V_{DD}	-	44, 2	33, 74	**Supply voltage** + 5 V nominal.
V_{SS}	-	22, 64	11, 52	**Ground.**
XTAL1, XTAL2	I	29, 30	18, 19	**External Crystal Inputs**. XTAL1 can be used as a clock-input if an external clock generator is used. The crystal or external clock frequency is divided by 2 to obtain the internal clock and CKOUT signals.
CKOUT	O	28	17	**Clock Out**. This is the reference from the internal system clock.
MD0/GPINT MD1/PHALTN	I	13, 12	2, 1	**Input lines**. These signals define the memory map to be used and the activation of the 16-bit parallel port or the 16-bit data bus. These pins are combined with signals used in emulator mode: GPINT is the Interrupt coming from the external logic used to emulate the GP port. PHALTN is used to freeze the state of the on chip peripherals.
ALE	O	14	3	**Address Latch Enable**. Used to latch the low byte of address (AD0-AD7) during access to external 8051 bus compatible peripheral circuits.
WRN/FETCHN	O	16	5	**External Peripheral Write Strobe** (active LOW). In emulator mode, this pin serves also as the FETCHN output.
RDN/IACK7N	O	15	4	**External Peripheral Read Strobe** (active LOW). In emulator mode, this pin serves also as IACK7N output.

MNEMONIC	TYPE	PLCC84	QFP80	FUNCTION
CSROMN	O	26	15	**ROM Chip Select** (active LOW). Decodes a size of 512 K bytes mapped from 0 to 512 K bytes (available in the Modes 1 to 3). CSROMN is asserted during the read cycles of the Reset Vector.
CSRAMN/EMUL	O	27	16	**RAM Chip Select** (active LOW). Decodes a size of 512 K bytes mapped from 512 K bytes to 1 M bytes (available in the Modes 1 to 3). This pin is also used during Reset, to enter Emulator mode. See notes 1 and 2.
AP5 to AP7	I/O	53–55	42, 43, n.a.	**Auxiliary I/O Port** (always available). AP7 is not available in the QFP package.
SCL (SP0)	I/O	75	63	**Serial Clock** (open drain). SCL is the clock signal for the I²C-bus operation. It is driven either by the 90C100 when the I²C interface is in the master mode, or it becomes the clock input when I²C interface is in the slave mode.
SDA (SP1)	I/O	74	62	**Serial Data** (open drain). SDA is the data signal for the I²C-bus.
T1 (SP6), T2 (SP7)	I/O	69, 68	57, 56	**Timers 1 and 2** (3-state). These are I/O signals for the capture timers of Channels 1 and 2 respectively. They can be programmed as either outputs for pulses or inputs for count cycles and events.
RXD (SP3)	I/O	72	60	**Receive Data.** RXD is the data input for the UART serial interface.
TXD (SP2)	I/O	73	61	**Transmit Data.** TXD is data output for the UART serial interface.
RTSN (SP4)	I/O	71	59	**Request To Send** (active LOW). This output of the UART serial interface indicates that the receiver is ready to accept data on the RXD line.
CTSN (SP5)	I/O	70	58	**Clear To Send** (active LOW). This input to the UART serial interface indicates that the remote receiving device is ready. RTSN and CTSN can be connected to each other if no control lines are required.
XCKI	I	67	55	**External Clock.** When selected, XCKI is the clock input for the UART serial interface. This signal can be used to either: - generate special baud rates. - or when a crystal frequency other than 29.491 MHz is used by the 90C100, an external clock of 9.8304 MHz may be connected to this input to generate the standard baud rates.
XCKO	O	66	54	**Auxiliary Oscillator Output.** To be connected along with XCKI, to a crystal in order to generate the auxiliary clock for the UART or the CPU. Can be used as a low-cost RC oscillator for stand-by function.
SP0 to SP7	I/O	75-68	63–56	**Input/Output** port if the alternate function is not used.

Notes

1. Pin with high impedance pull-up resistor
2. The pull-up on CSRAMN/EMUL is activated during the RESET to avoid floating level at power-on.