

# NP180N055TUJ

R07DS0181EJ0100

Rev.1.00

Dec 22, 2010

## MOS FIELD EFFECT TRANSISTOR

### Description

The NP180N055TUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

### Features

- Low on-state resistance  
—  $R_{DS(on)} = 2.3 \text{ m}\Omega \text{ MAX.}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 90 \text{ A}$ )
- Low Ciss:  $C_{iss} = 9500 \text{ pF TYP.}$  ( $V_{DS} = 25 \text{ V}$ )
- Designed for automotive application and AEC-Q101 qualified

### Ordering Information

Part No.	Lead Plating	Packing	Package
NP180N055TUJ-E1-AY <sup>*1</sup>	Pure Sn (Tin)	Tape 800 p/reel	TO-263-7pin, Taping (E1 type)
NP180N055TUJ-E2-AY <sup>*1</sup>			TO-263-7pin, Taping (E2 type)

Note: <sup>\*1</sup>. Pb-free (This product does not contain Pb in the external electrode.)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	55	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 180$	A
Drain Current (pulse) <sup>*1</sup>	$I_{D(pulse)}$	$\pm 720$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	348	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>*2</sup>	$P_{T2}$	1.8	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current <sup>*3</sup>	$I_{AR}$	66	A
Repetitive Avalanche Energy <sup>*3</sup>	$E_{AR}$	435	mJ

### Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.43	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance <sup>*2</sup>	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

Notes: <sup>\*1</sup>.  $T_C = 25^\circ\text{C}$ ,  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

<sup>\*2</sup>. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mm

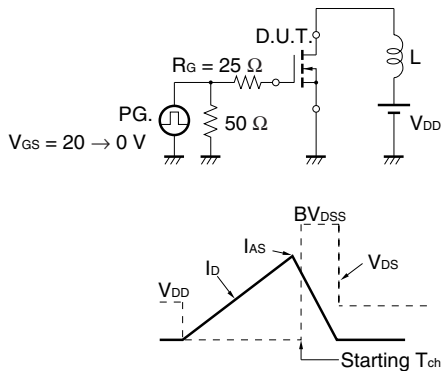
<sup>\*3</sup>.  $T_{ch(peak)} \leq 150^\circ\text{C}$ ,  $R_G = 25 \Omega$

**Electrical Characteristics (T<sub>A</sub> = 25°C)**

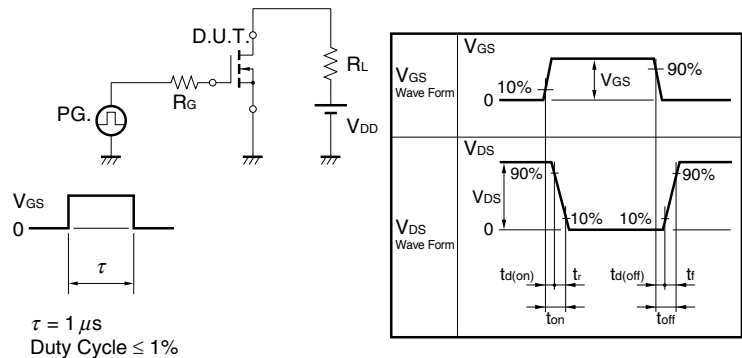
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 55 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	2.0	3.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	65	130		S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 90 A
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>		1.7	2.3	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 90 A
Input Capacitance	C <sub>iss</sub>		9500	14250	pF	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz
Output Capacitance	C <sub>oss</sub>		1060	1590	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		320	580	pF	
Turn-on Delay Time	t <sub>d(on)</sub>		45	100	ns	V <sub>DD</sub> = 28 V, I <sub>D</sub> = 90 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 0 Ω
Rise Time	t <sub>r</sub>		20	50	ns	
Turn-off Delay Time	t <sub>d(off)</sub>		100	200	ns	
Fall Time	t <sub>f</sub>		10	30	ns	
Total Gate Charge	Q <sub>G</sub>		150	230	nC	V <sub>DD</sub> = 44 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 180 A
Gate to Source Charge	Q <sub>GS</sub>		35		nC	
Gate to Drain Charge	Q <sub>GD</sub>		45		nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.9	1.5	V	I <sub>F</sub> = 180 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		64		ns	I <sub>F</sub> = 180 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Q <sub>rr</sub>		138		nC	di/dt = 100 A/μs

Note: \*1. Pulsed

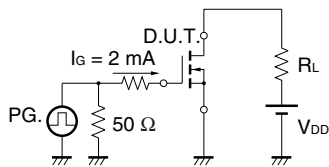
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

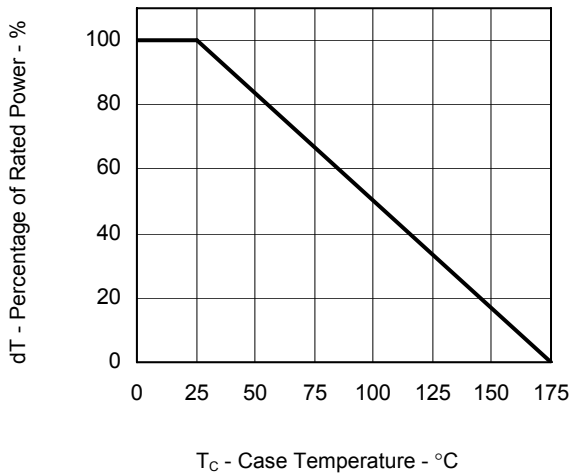


**TEST CIRCUIT 3 GATE CHARGE**

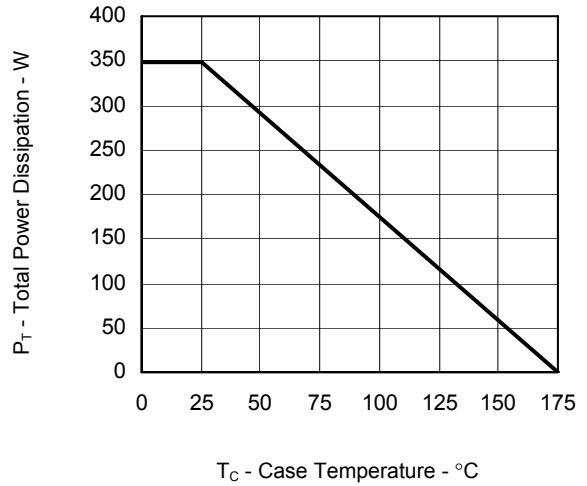


Typical Characteristics (T<sub>A</sub> = 25°C)

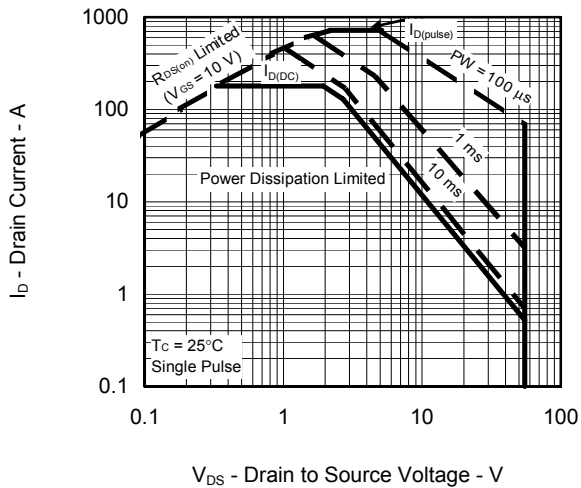
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



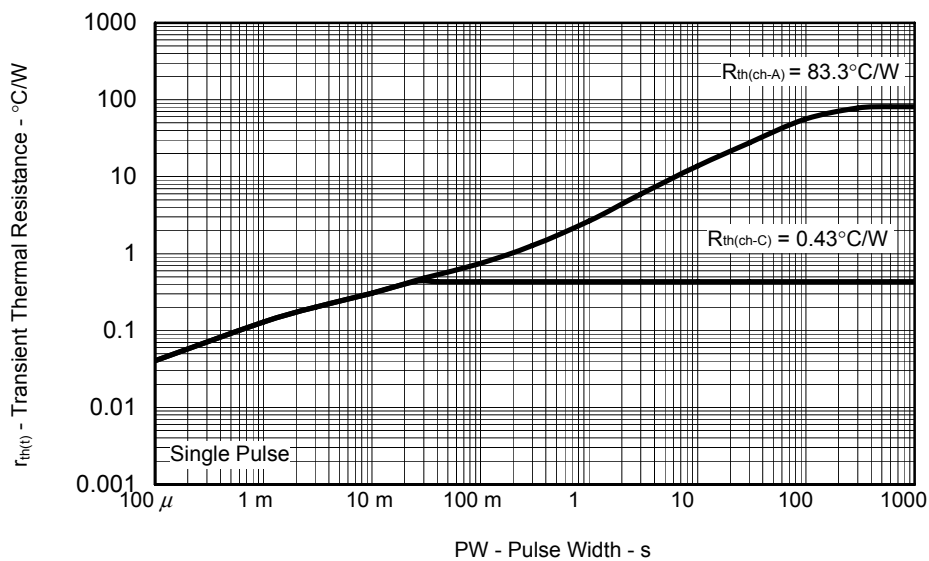
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



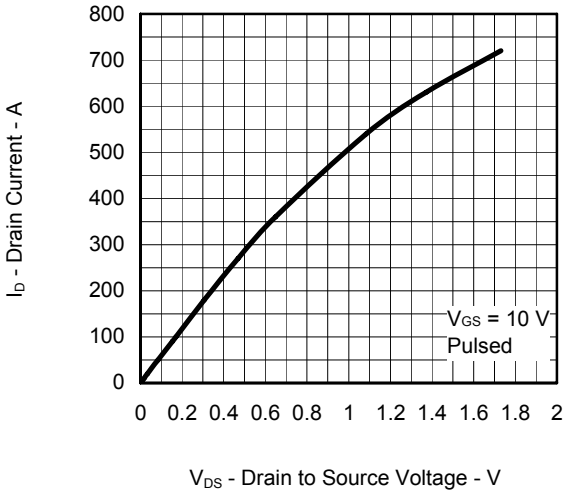
FORWARD BIAS SAFE OPERATING AREA



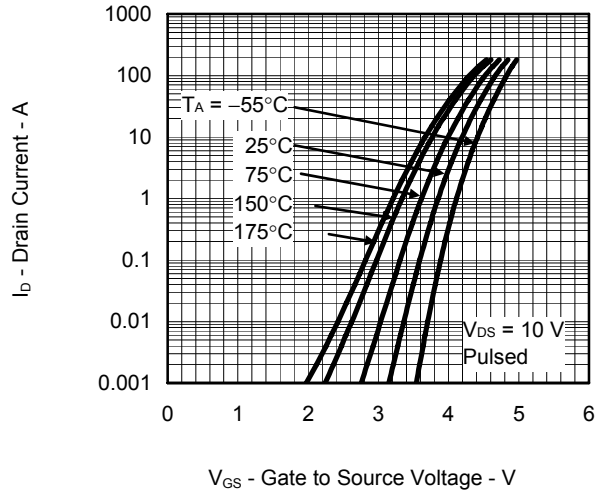
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



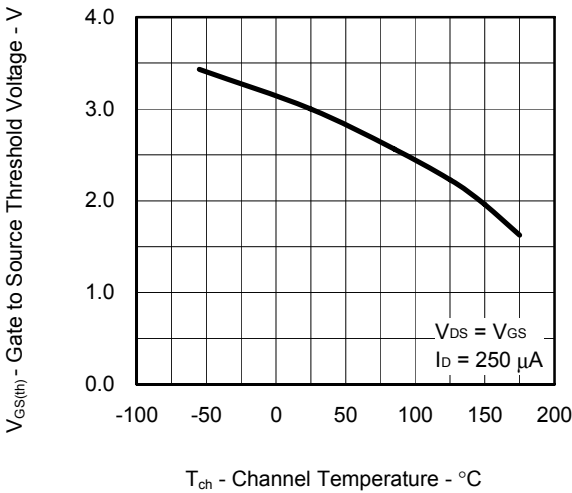
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



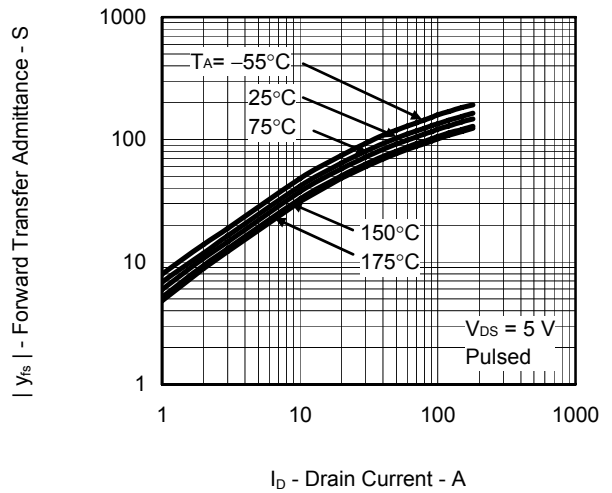
FORWARD TRANSFER CHARACTERISTICS



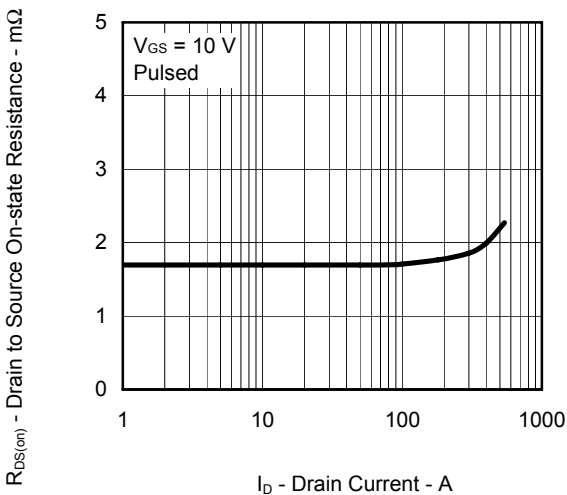
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



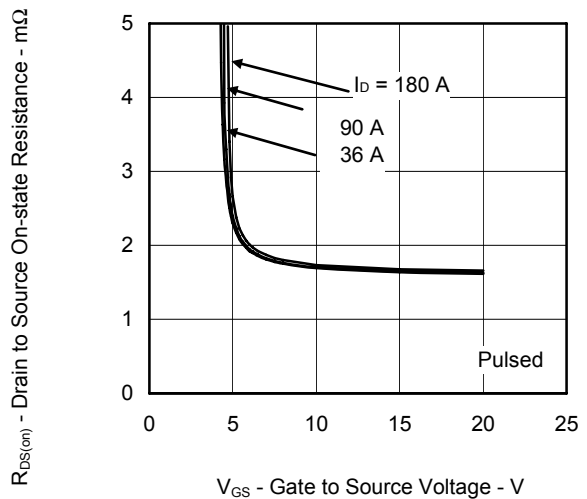
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



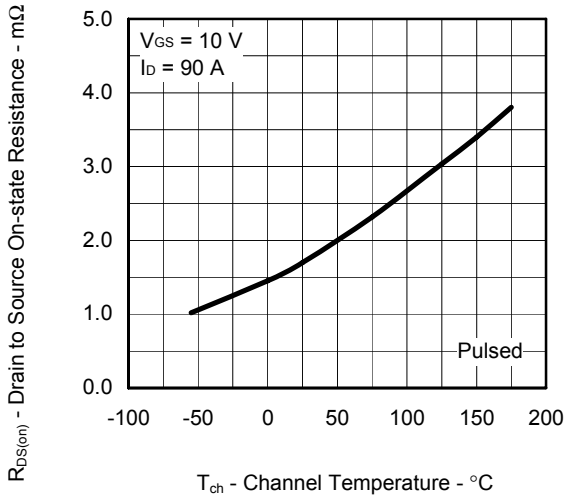
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



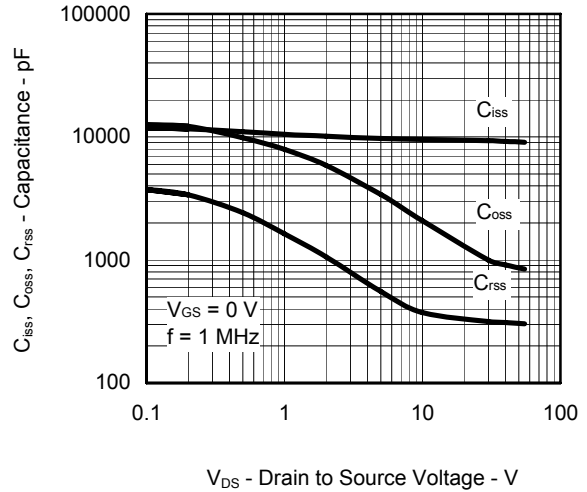
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



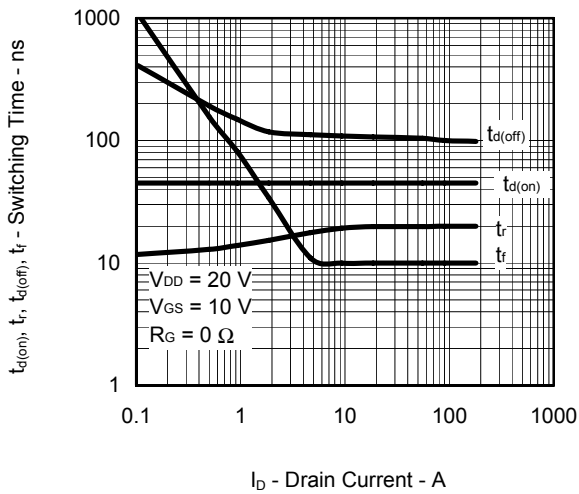
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



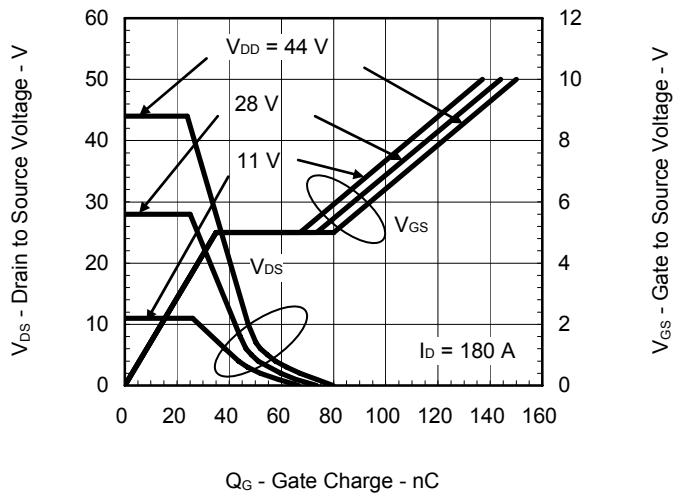
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



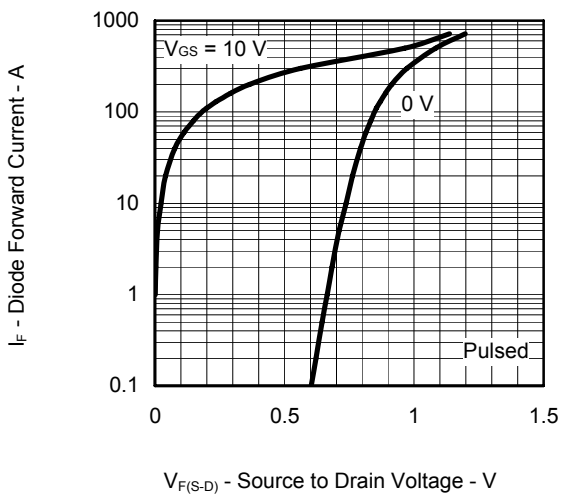
SWITCHING CHARACTERISTICS



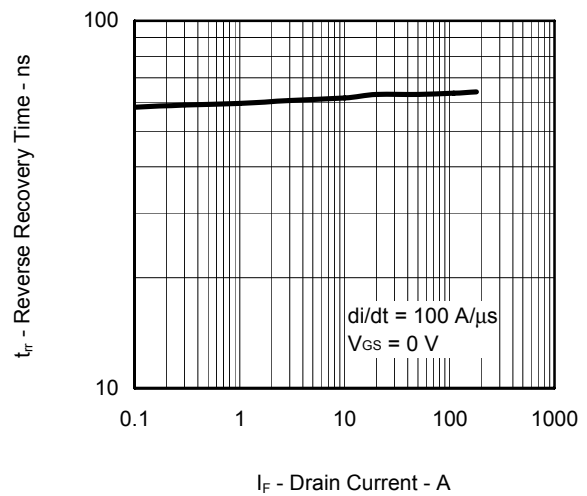
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

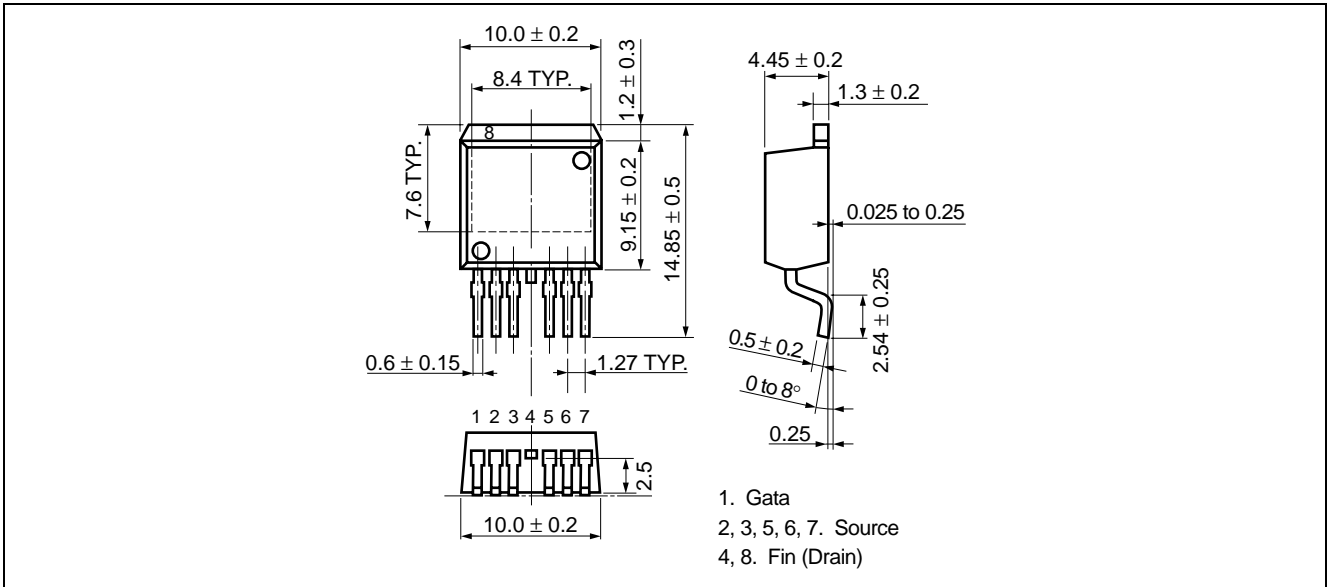


REVERSE RECOVERY TIME vs. DRAIN CURRENT

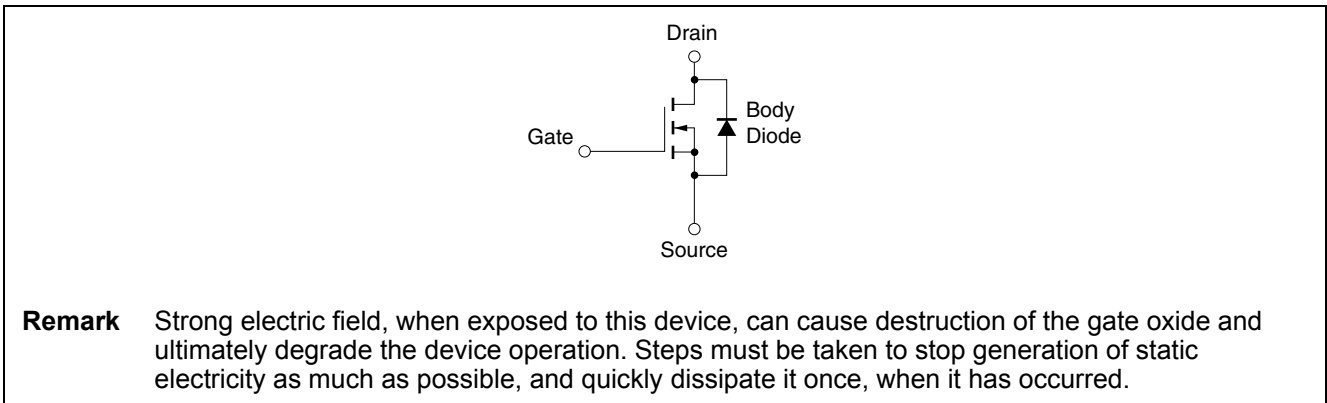


Package Drawings (Unit: mm)

TO-263-7pin (MP-25ZT) (Mass: 1.5 g TYP.)



Equivalent Circuit



<b>Revision History</b>	<b>NP180N055TUJ Data Sheet</b>
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<b>Rev.</b>	<b>Date</b>	<b>Description</b>	
		<b>Page</b>	<b>Summary</b>
1.00	Dec 22, 2010	-	First Edition Issued

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