NP160N04TUK

MOS FIELD EFFECT TRANSISTOR

R07DS0543EJ0100
Rev.1.00
Sep 23, 2011

Description

The NP160N04TUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
  $R_{DS(on)}$ = 1.5 mΩ MAX. (V_{GS} = 10 V, I_D = 80 A)
- Low C_{iss}: C_{iss} = 7200 pF TYP. (V_{DS} = 25 V)
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP160N04TUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263-7pin (MP-25ZT)
NP160N04TUK-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±160	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±640	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	250	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *2	I_{AR}	56	A
Repetitive Avalanche Energy *2	E_{AR}	313	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.60	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	°C/W

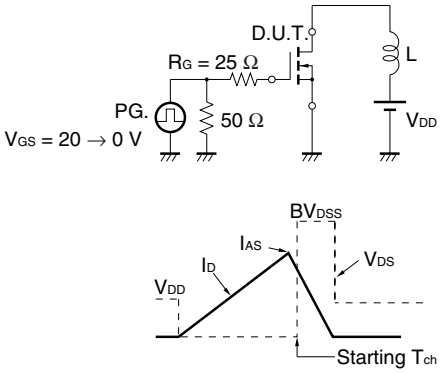
Notes: *1. T_C = 25°C, P_W ≤ 10 μs, Duty Cycle ≤ 1%
*2. R_G = 25 Ω, V_{GS} = 20 → 0 V

Electrical Characteristics (T_A = 25°C)

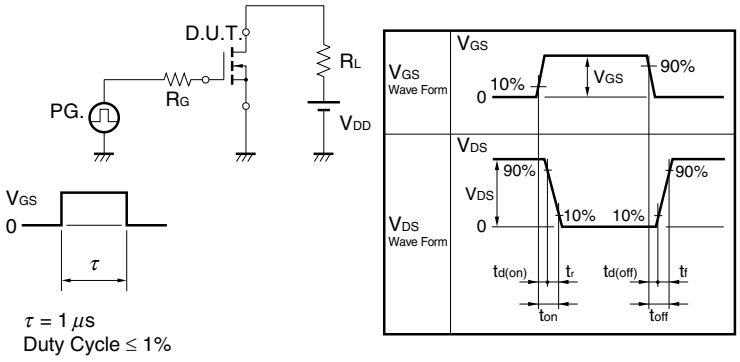
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	$\|y_{fs}\|$	60	120		S	V_{DS} = 5 V, I_D = 80 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$		1.25	1.50	mΩ	V_{GS} = 10 V, I_D = 80 A
Input Capacitance	C_{iss}		7200	10800	pF	V_{DS} = 25 V,
Output Capacitance	C_{oss}		1040	1560	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		390	710	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		30	70	ns	V_{DD} = 20 V, I_D = 80 A,
Rise Time	t_r		16	40	ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		100	200	ns	R_G = 0 Ω
Fall Time	t_f		13	40	ns	
Total Gate Charge	Q_G		126	189	nC	V_{DD} = 32 V,
Gate to Source Charge	Q_{GS}		32		nC	V_{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		31		nC	I_D = 160 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I_F = 160 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		62		ns	I_F = 160 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		110		nC	di/dt = 100 A/μs

Note: *1. Pulsed test

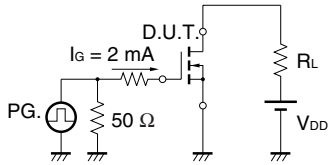
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

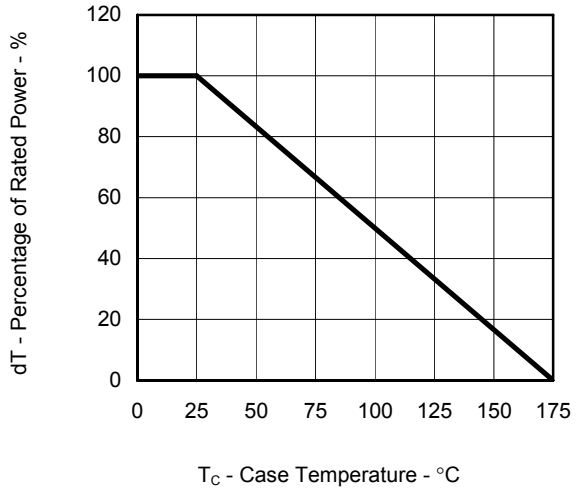


TEST CIRCUIT 3 GATE CHARGE

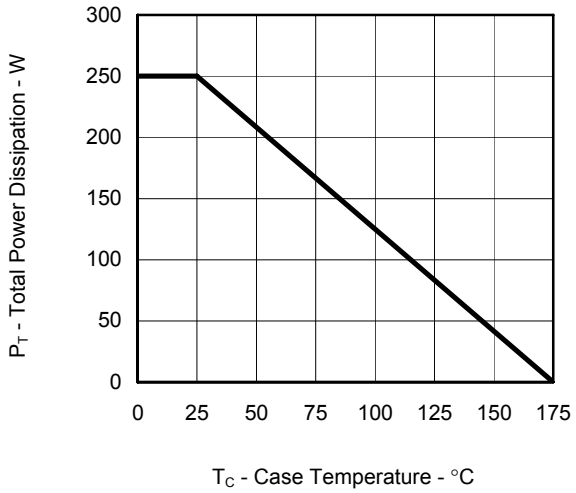


Typical Characteristics (T_A = 25°C)

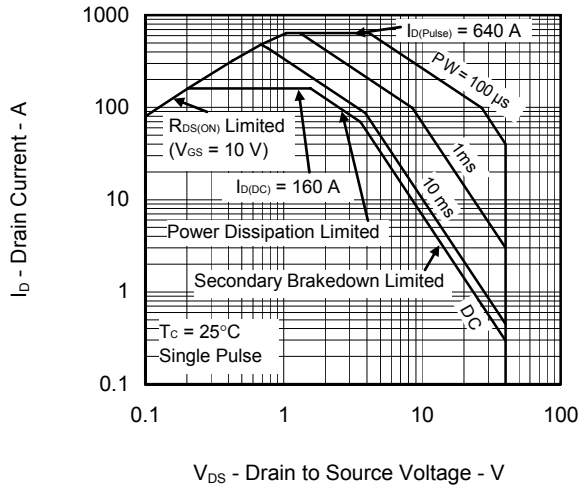
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



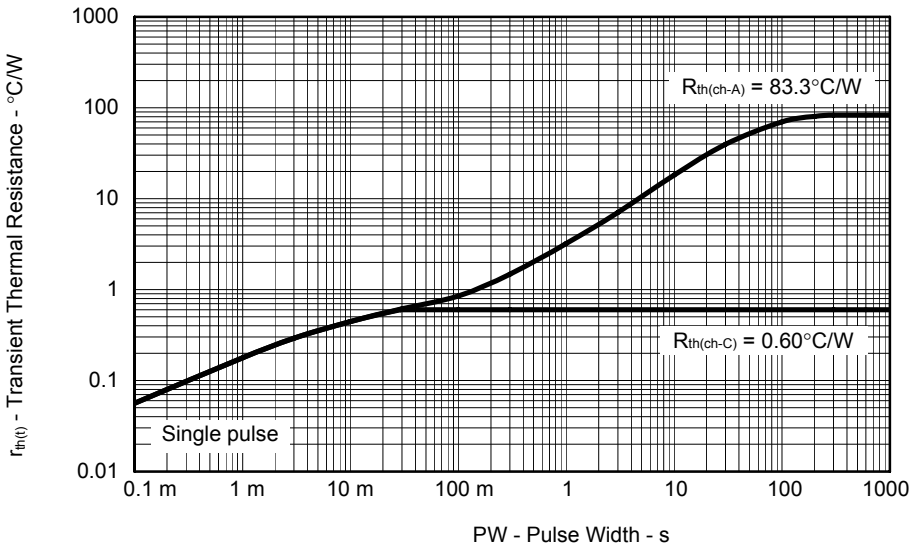
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



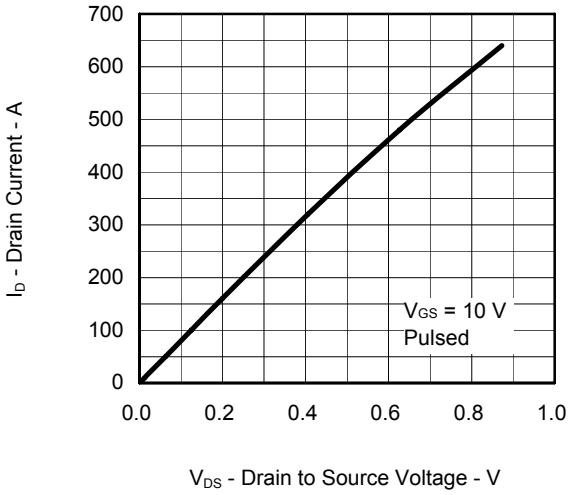
FORWARD BIAS SAFE OPERATING AREA



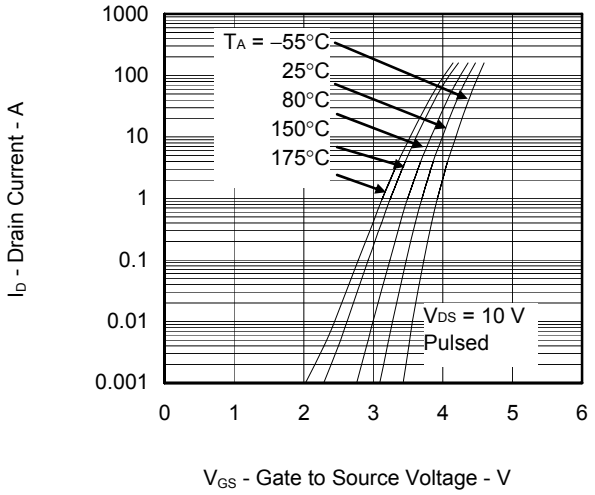
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



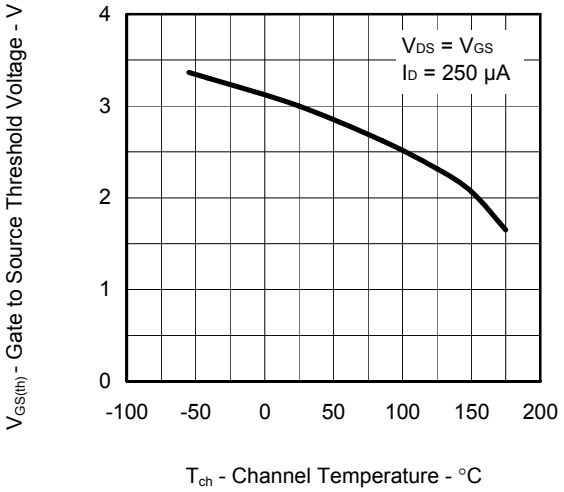
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



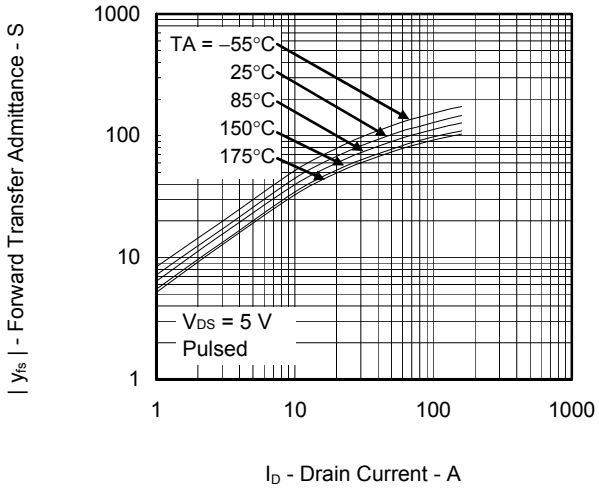
FORWARD TRANSFER CHARACTERISTICS



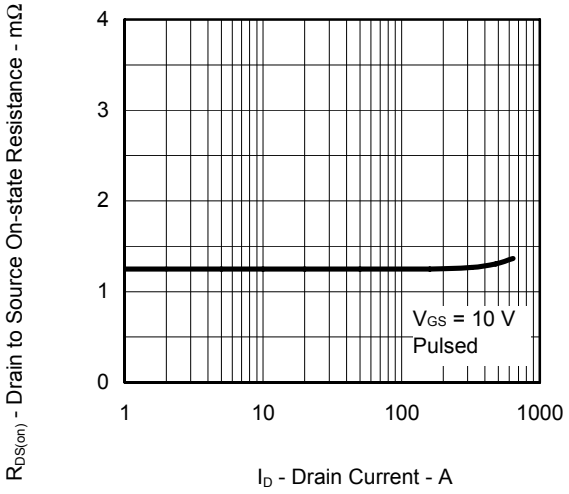
GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATURE



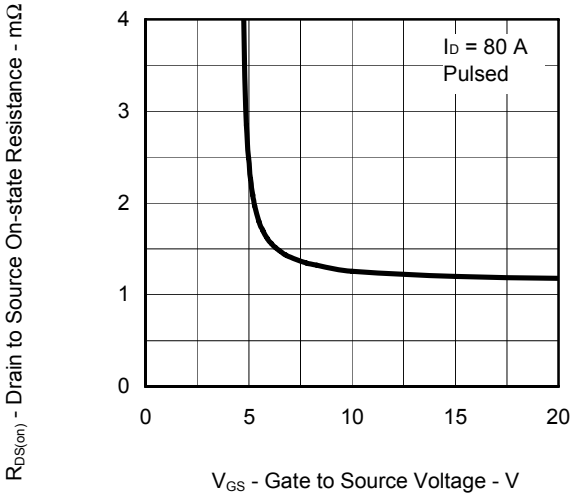
FORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENT



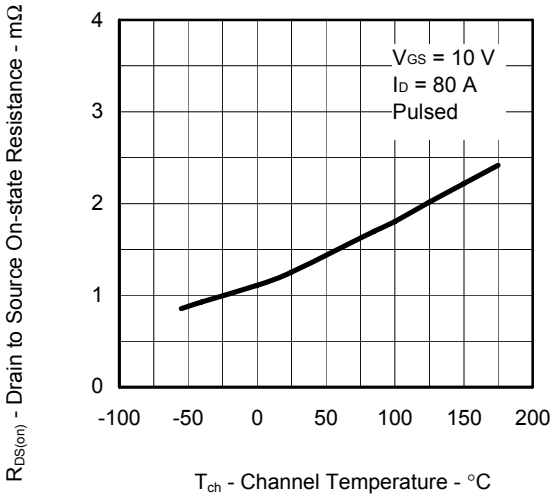
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



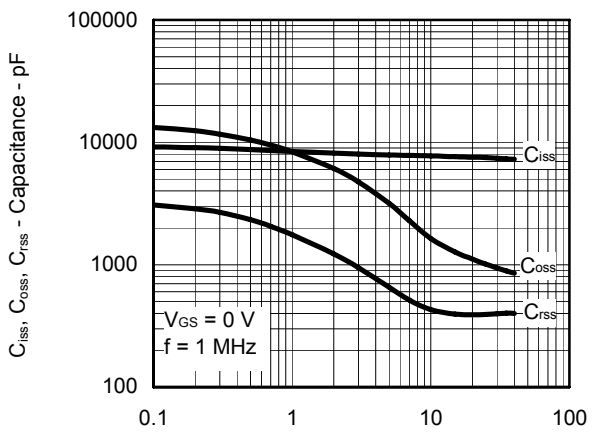
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



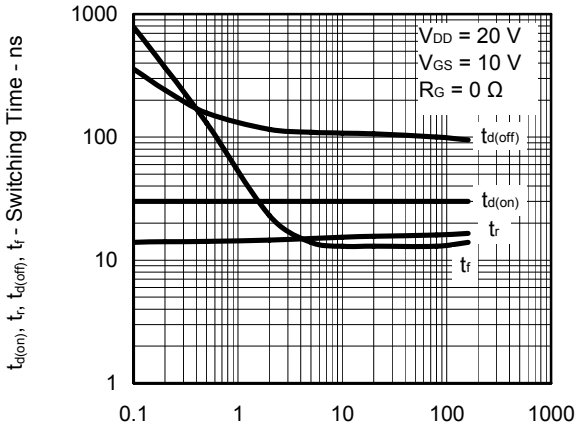
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



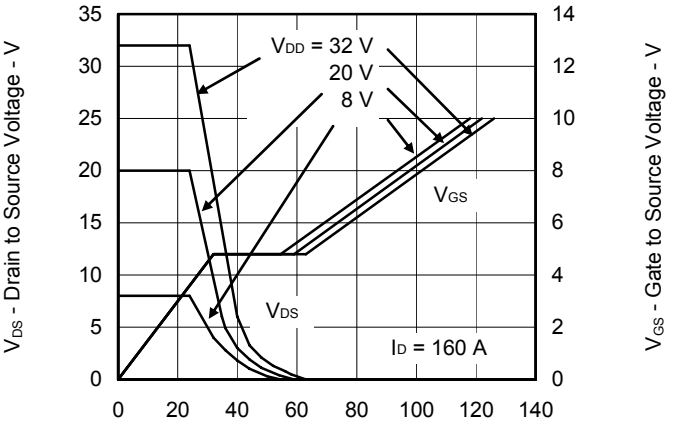
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



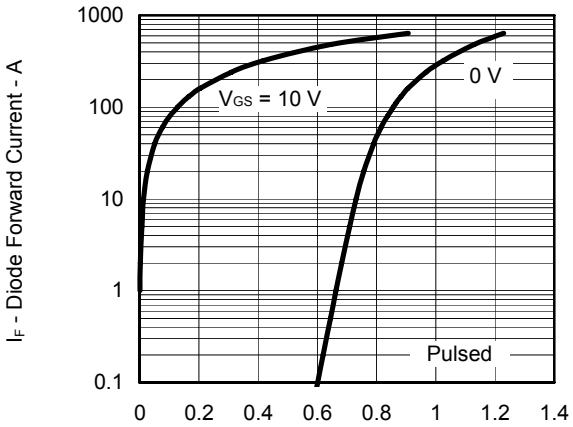
SWITCHING CHARACTERISTICS



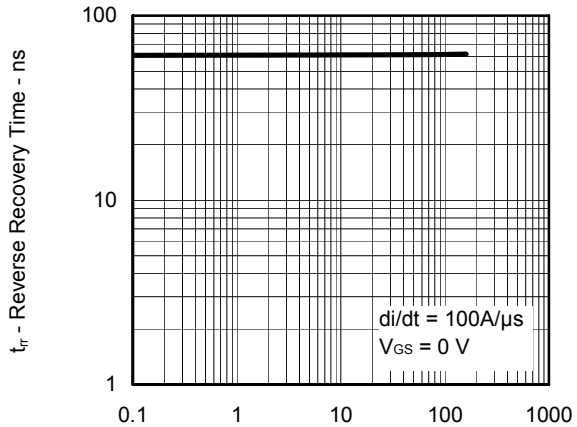
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

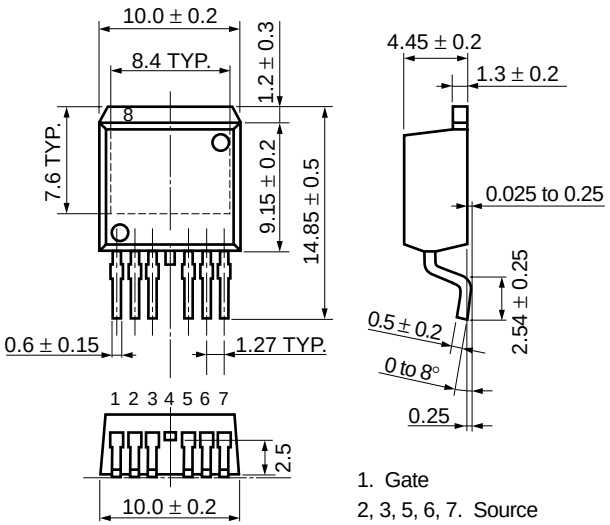


REVERSE RECOVERY TIME vs. DRAIN CURRENT



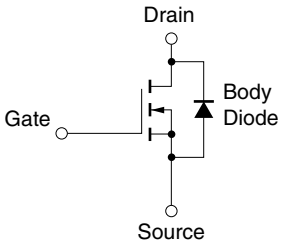
Package Drawing (Unit: mm)

TO-263-7pin (MP-25ZT) (Mass: 1.5 g TYP.)



1. Gate
2, 3, 5, 6, 7. Source
4, 8. Fin (Drain)

Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP160N04TUK Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep 23, 2011	–	First Edition Issued

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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