HYB25DC512800C[E/F]
HYB25DC512160C[E/F]

512-Mbit Double-Data-Rate SDRAM

DDR SDRAM

RoHS Compliant Products

Memory Products

Infineon technologies

N e v e r   s t o p   t h i n k i n g .

HYB25DC512800C[E/F], HYB25DC512160C[E/F]

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Page	Subjects (major changes since last revision)
9	added product types HYB25DC512800C[E/F]-6 and HYB25DC512160C[E/F]-6
65	addded AC Timing Diagrams
69	added I_{DD} currents DDR333

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1 Overview

This chapter gives an overview of the 512-Mbit Double-Data-Rate SDRAM product family and describes its main characteristics.

1.1 Features

- Double data rate architecture: two data transfers per clock cycle
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Burst Lengths: 2, 4, or 8
- CAS Latency: 2, 2.5, 3
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- RAS-lockout supported $t_{RAP} = t_{RCD}$
- 7.8 µs Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL_2 compatible) I/O
- $V_{DDQ} = 2.5 \text{ V} \pm 0.2 \text{ V}$
- $V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$
- P-TFBGA-60 package
- PG-TSOPII-66 package
- RoHS Compliant Products[1]

Table 1 Performance

Part Number Speed Code			–5	–6	Unit
Speed Grade	Component		DDR400B	DDR333	—
max. Clock Frequency	@CL3	f_{CK3}	200	166	MHz
	@CL2.5	$f_{CK2.5}$	166	333	MHz
	@CL2	f_{CK2}	133	266	MHz

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[1]

RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The 512-Mbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512-Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a *2n* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512-Mbit Double-Data-Rate SDRAM effectively consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 512-Mbit Double-Data-Rate SDRAM operates from a differential clock (CK and $\overline{\text{CK}}$; the crossing of CK going HIGH and $\overline{\text{CK}}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Table 2 Ordering Information for Lead-Free(RoHS Compliant Products)

Part Number[1]	Org.	CAS-RCD-RP Latencies	Clock (MHz)	CAS-RCD-RP Latencies	Clock (MHz)	Speed	Package
HYB25DC512800CE–5	×8	3-3-3	200	2.5-3-3	166	DDR400B	PG-TSOPII-66
HYB25DC512800CF–5							PG-TFBGA-60
HYB25DC512160CE–5	×16						PG-TSOPII-66
HYB25DC512160CF–5							PG-TFBGA-60
HYB25DC512800CE–6	×8	2.5-3-3	166	2-3-3	133	DDR333	PG-TSOPII-66
HYB25DC512800CF–6							PG-TFBGA-60
HYB25DC512160CE–6	×16						PG-TSOPII-66
HYB25DC512160CF–6							PG-TFBGA-60

1) HYB: designator for memory components
   25DC: DDR SDRAMs at V_{DDQ} = 2.5 V
   512: 512-Mbit density
   800/160: Product variations x8 and x16
   E/F: Package type FBGA and TSOP

1 Pin Configuration

The pin configuration of a DDR SDRAM is listed by function in **Table 1** (60 pins). The abbreviations used in the Pin#/Buffer# column are explained in **Table 2** and **Table 3** respectively. The pin numbering for FBGA is depicted in Figure 1 and that of the TSOP package in Figure 2.

Table 1   Pin Configuration of DDR SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
G2, 45	CK1	I	SSTL	**Clock Signal** Note: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
G3, 46	$\overline{CK1}$	I	SSTL	**Complementary Clock Signal**
H3, 44	CKE	I	SSTL	**Clock Enable Rank** Note: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after V_{DD} is applied on first power up. After V_{REF} has become stable during the power on and initialization sequence, it must be mantained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be mantained to this input.
Control Signals				
H7, 23	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
G8, 22	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
G7, 21	$\overline{WE}$	I	SSTL	**Write Enable**
H8, 24	$\overline{CS}$	I	SSTL	**Chip Select** Note: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin.
Address Signals				
J8, 26	BA0	I	SSTL	**Bank Address Bus 2:0**
J7, 27	BA1	I	SSTL	Note: BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.

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512-Mbit Double-Data-Rate SDRAM

Pin Configuration

Table 1   Pin Configuration of DDR SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
K7, 29	A0	I	SSTL	**Address Bus 11:0**
L8, 30	A1	I	SSTL	Note: Provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a Mode Register Set command.
L7, 31	A2	I	SSTL	
M8, 32	A3	I	SSTL	
M2, 35	A4	I	SSTL	
L3, 36	A5	I	SSTL	
L2, 37	A6	I	SSTL	
K3, 38	A7	I	SSTL	
K2, 39	A8	I	SSTL	
J3, 40	A9	I	SSTL	
K8, 28	A10	I	SSTL	
	AP	I	SSTL	
J2, 41	A11	I	SSTL	
H2, 42	A12	I	SSTL	**Address Signal 12**
				Note: Module based on 256 Mbit or larger dies
	NC	NC	—	Note: Module based on 128 Mbit or smaller dies
F9, 17	A13	I	SSTL	**Address Signal 13**
				Note: 1 Gbit based module
	NC	NC	—	Note: Module based on 512 Mbit or smaller dies
Data Signals ×8 organization				
A8, 2	DQ0	I/O	SSTL	**Data Signal Bus 7:0**
B7, 5	DQ1	I/O	SSTL	
C7, 8	DQ2	I/O	SSTL	
D7, 11	DQ3	I/O	SSTL	
D3, 56	DQ4	I/O	SSTL	
C3, 59	DQ5	I/O	SSTL	
B3, 62	DQ6	I/O	SSTL	
A2, 65	DQ7	I/O	SSTL	
Data Strobe ×8 organisation				
E3, 51	DQS	I/O	SSTL	**Data Strobe**
				Note: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data.
Data Mask ×8 organization				
F3, 47	DM	I	SSTL	**Data Mask**
				Note: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.

Table 1   Pin Configuration of DDR SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Data Signals ×16 organization				
A8, 2	DQ0	I/O	SSTL	**Data Signal 15:0**
B9, 4	DQ1	I/O	SSTL	
B7, 5	DQ2	I/O	SSTL	
C9, 7	DQ3	I/O	SSTL	
C7, 8	DQ4	I/O	SSTL	
D9, 10	DQ5	I/O	SSTL	
D7, 11	DQ6	I/O	SSTL	
E9, 13	DQ7	I/O	SSTL	
E1, 54	DQ8	I/O	SSTL	
D3, 56	DQ9	I/O	SSTL	
D1, 57	DQ10	I/O	SSTL	
C3, 59	DQ11	I/O	SSTL	
C1, 60	DQ12	I/O	SSTL	
B3, 62	DQ13	I/O	SSTL	
B1, 63	DQ14	I/O	SSTL	
A2, 65	DQ15	I/O	SSTL	
Data Strobe ×16 organization				
E3, 51	UDQS	I/O	SSTL	**Data Strobe Upper Byte**
E7, 16	LDQS	I/O	SSTL	**Data Strobe Lower Byte**
Data Mask ×16 organization				
F3, 47	UDM	I	SSTL	**Data Mask Upper Byte**
F7, 20	LDM	I	SSTL	**Data Mask Lower Byte**
Power Supplies				
F1, 49	V_{REF}	AI	—	**I/O Reference Voltage**
A9, B2, C8, D2, E8, 3, 9, 15, 55, 61	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
A7, F8, M3, M7, 1, 18, 33	V_{DD}	PWR	—	**Power Supply**
A1, B8, C2, D8, E2, 6, 12, 52, 58, 64	V_{SSQ}	PWR	—	**Power Supply**
F2, 34	V_{SS}	PWR	—	**Power Supply**
Not Connected				
B1, 63	NC	NC	—	**Not Connected** *Note: ×8 organisation*
B9, 4	NC	NC	—	**Not Connected** *Note: ×8 organization*
C1, 60	NC	NC	—	**Not Connected** *Note: ×8 organization*

Table 1   Pin Configuration of DDR SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
C9, 7	NC	NC	—	**Not Connected** *Note: x8 organization*
D1, 57	NC	NC	—	**Not Connected** *Note: x8 organization*
D9, 10	NC	NC	—	**Not Connected** *Note: x8 organization*
E1, 54	NC	NC	—	**Not Connected** *Note: x8 organization*
E7, 16	NC	NC	—	**Not Connected** *Note: x8 organization*
E9, 13	NC	NC	—	**Not Connected** *Note: x8 organization*
F7, 20	NC	NC	—	**Not Connected** *Note: x8 organization*
14, 17, 19, 25, 43, 50	NC	NC	—	**Not Connected** *x16 and x8 organization*

Table 2   Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 3   Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

1	2	3	4	5	6	7	8	9
V_{SSQ}	DQ7	V_{SS}		A		V_{DD}	DQ0	V_{DDQ}
N.C.	V_{DDQ}	DQ6		B		DQ1	V_{SSQ}	N.C.
N.C.	V_{SSQ}	DQ5		C		DQ2	V_{DDQ}	N.C.
N.C.	V_{DDQ}	DQ4		D		DQ3	V_{SSQ}	N.C.
N.C.	V_{SSQ}	DQS		E		N.C.	V_{DDQ}	N.C.
V_{REF}	V_{SS}	DM		F		N.C.	V_{DD}	NC,A13
	CK	$\overline{CK}$		G		$\overline{WE}$	$\overline{CAS}$	
	NC,A12	CKE		H		$\overline{RAS}$	$\overline{CS}$	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10/AP	
	A6	A5		L		A2	A1	
	A4	V_{SS}		M		V_{DD}	A3	

(x8)

MPPD0420
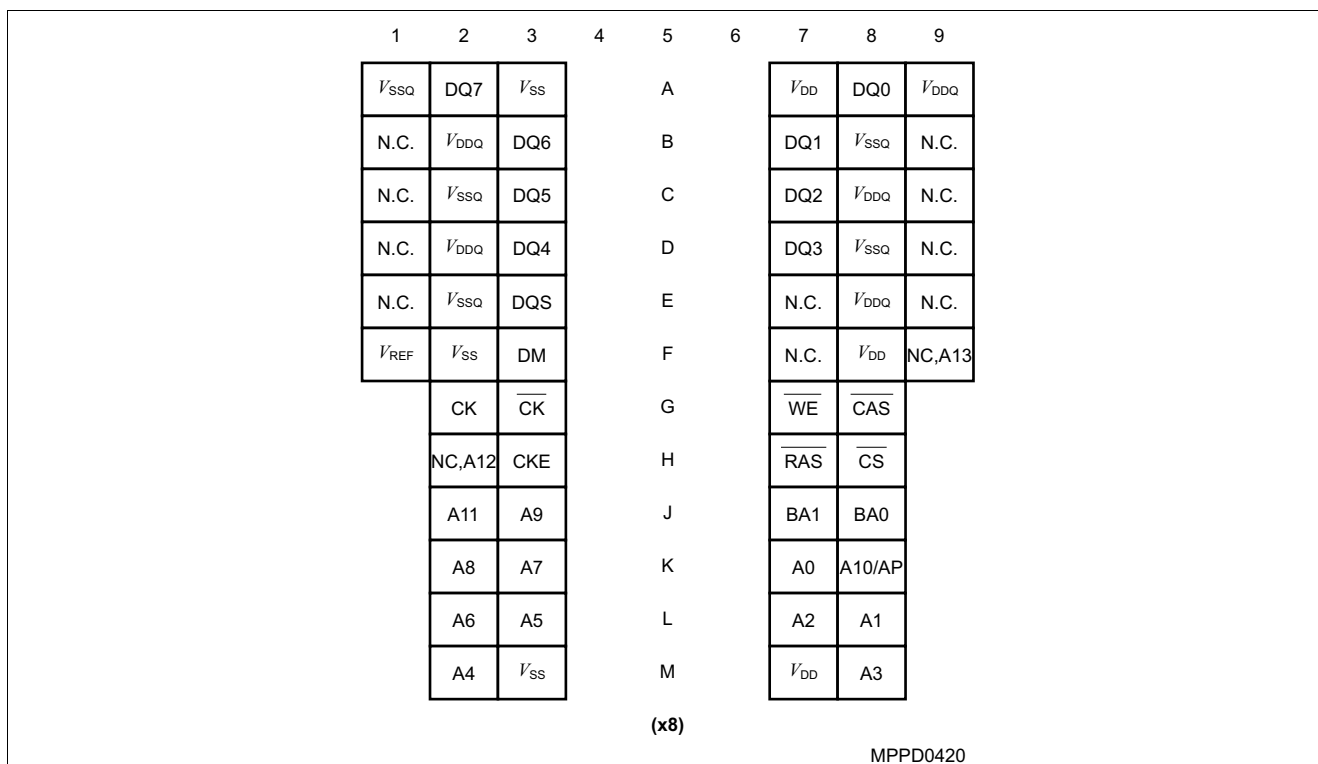
Figure 1   Pin Configuration PG-TFBGA-60 (top view) for ×8, see the balls throught the package

1	2	3	4	5	6	7	8	9
V_{SSQ}	DQ15	V_{SS}		A		V_{DD}	DQ0	V_{DDQ}
DQ14	V_{DDQ}	DQ13		B		DQ2	V_{SSQ}	DQ1
DQ12	V_{SSQ}	DQ11		C		DQ4	V_{DDQ}	DQ3
DQ10	V_{DDQ}	DQ9		D		DQ6	V_{SSQ}	DQ5
DQ8	V_{SSQ}	UDQS		E		LDQS	V_{DDQ}	DQ7
V_{REF}	V_{SS}	UDM		F		LDM	V_{DD}	NC,A13
	CK	$\overline{CK}$		G		$\overline{WE}$	$\overline{CAS}$	
	NC,A12	CKE		H		$\overline{RAS}$	$\overline{CS}$	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10/AP	
	A6	A5		L		A2	A1	
	A4	V_{SS}		M		V_{DD}	A3	

(x16)

MPPD0430
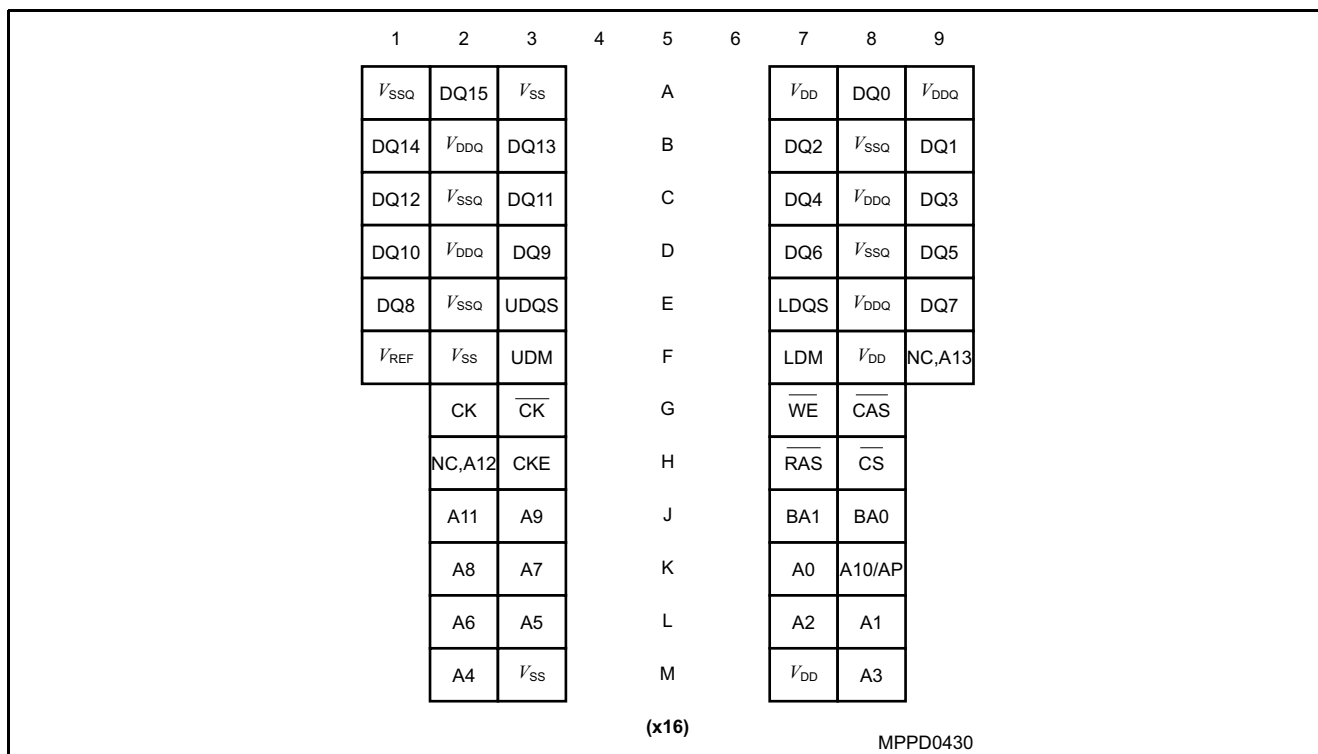
Figure 2   Pin Configuration PG-TFBGA-60 (top view) for ×16, see the balls throught the package

Pin Configuration
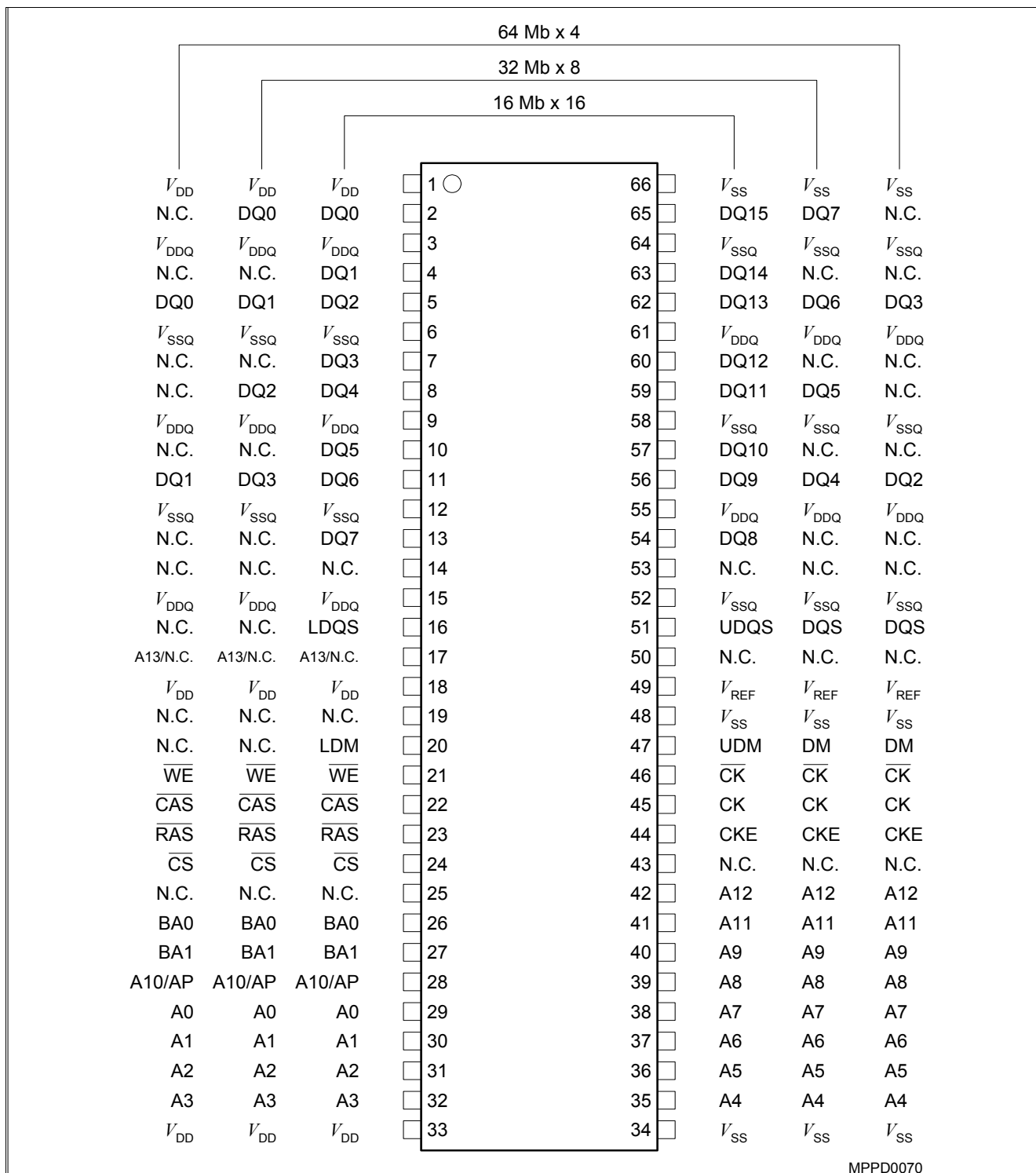
Figure 3   Pin Configuration PG-TSOPII-66
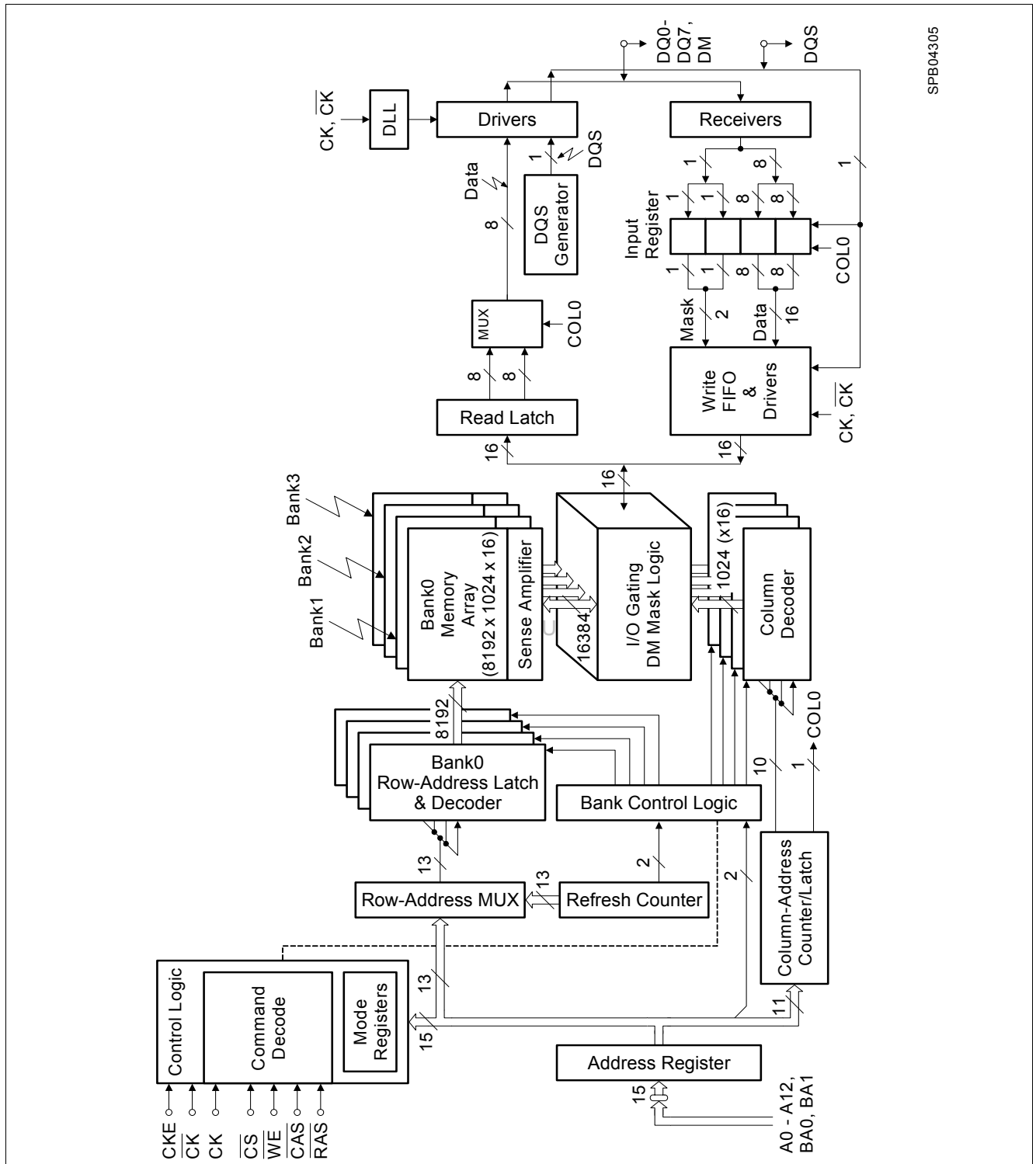
Figure 4   Block Diagram 512Mbit 64 Mbit ×8
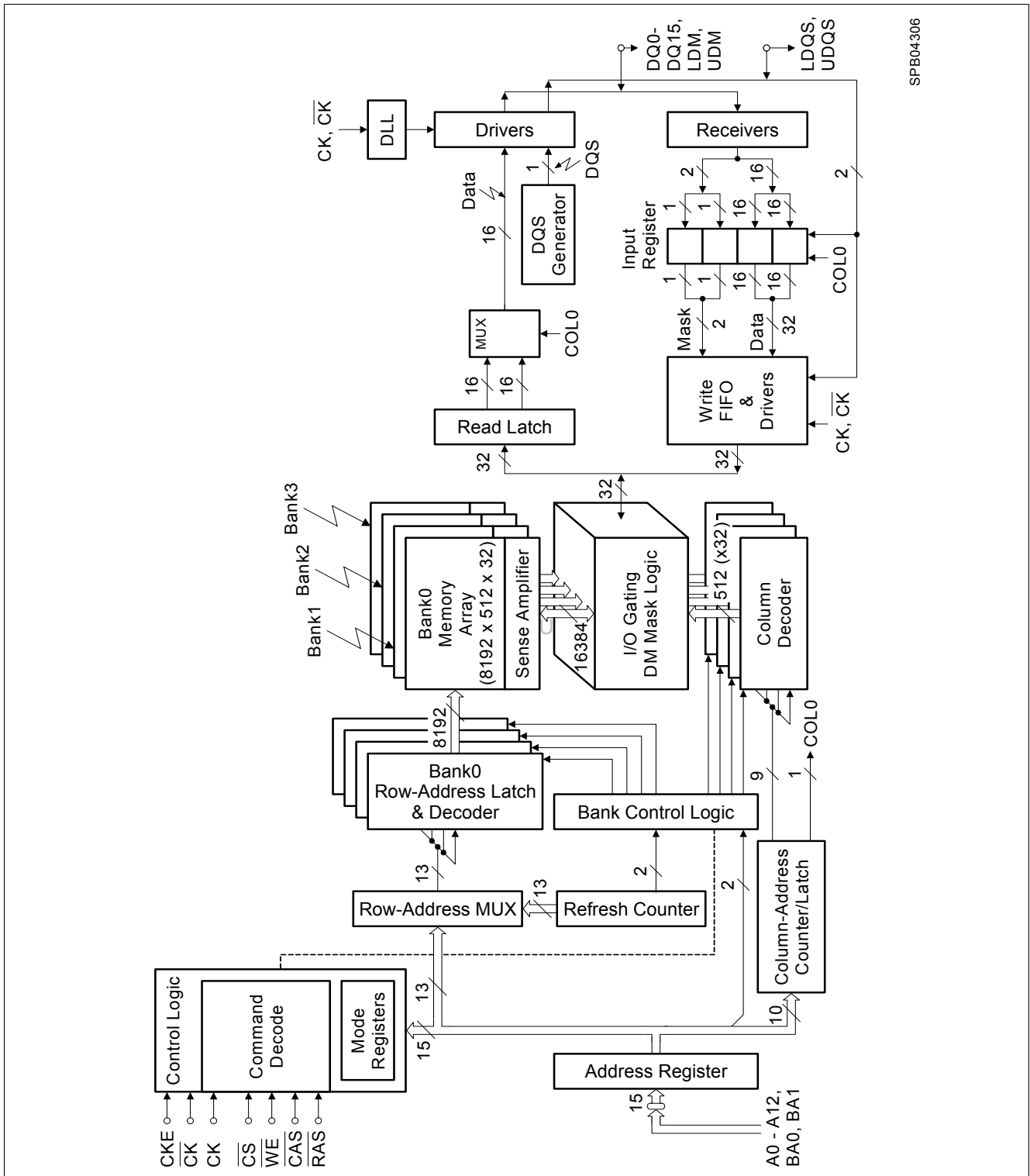
Figure 5   Block Diagram 512Mbit 32 Mbit ×16

2 Functional Description

The 512-Mbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The 512-Mbit Double-Data-Rate SDRAM is internally configured as a quad-bank DRAM.

The 512-Mbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512-Mbit Double-Data-Rate SDRAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

2.1 Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following criteria must be met:

No power sequencing is specified during power up or power down given the following criteria:

- V_{DD} and V_{DDQ} are driven from a single power converter output
- V_{TT} meets the specification
- A minimum resistance of 42 Ω limits the input current from the V_{TT} supply into any pin and V_{REF} tracks $V_{DDQ}/2$

or the following relationship must be followed:

- V_{DDQ} is driven after or with V_{DD} such that $V_{DDQ} < V_{DD} + 0.3$ V
- V_{TT} is driven after or with V_{DDQ} such that $V_{TT} < V_{DDQ} + 0.3$ V
- V_{REF} is driven after or with V_{DDQ} such that $V_{REF} < V_{DDQ} + 0.3$ V

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 μs delay prior to applying an executable command.

Once the 200 μs delay has been satisfied, a Deselect or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a Precharge ALL command should be applied. Next a Mode Register Set command should be issued for the Extended Mode Register, to enable the DLL, then a Mode Register Set command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any executable command. During the 200 cycles of clock for DLL locking, a Deselect or NOP command must be applied. After the 200 clock cycles, a Precharge ALL command should be applied, placing the device in the "all banks idle" state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

2.2 Mode Register Definition

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode. The Mode Register is programmed via the Mode Register Set command (with BA0 = 0 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Mode Register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 specify the operating mode.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements results in unspecified operation.

MR
Mode Register Definition (BA[1:0] = 00$_B$)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	Operating MODE						CL			BT	BL		
reg. addr		w						w			w	w		

Field	Bits	Type[1]	Description
BL	[2:0]	w	**Burst Length** Number of sequential bits per DQ related to one read/write command; see **Chapter 2.2.1**. *Note: All other bit combinations are RESERVED.* 001 2 010 4 011 8
BT	3		**Burst Type** See **Table 4** for internal address sequence of low order address bits; see **Chapter 2.2.2**. 0 Sequential 1 Interleaved
CL	[6:4]		**CAS Latency** Number of full clocks from read command to first data valid window; see **Chapter 2.2.3**. *Note: All other bit combinations are RESERVED.* 010 2 110 2.5 011 3
MODE	[12:7]		**Operating Mode** See **Chapter 2.2.4**. *Note: All other bit combinations are RESERVED.* 000000 Normal Operation without DLL Reset 000010 Normal DLL Reset

1) w = write only register bit

2.2.1 Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2-Ai when the burst length is set to four and by A3-Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

2.2.2 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in **Table 4**.

Table 4   Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes

1. *For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.*
3. *For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access within the block.*
4. *Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.*

2.2.3 Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2, 2.5 and 3 clocks. If a Read command is registered at clock edge n, and the latency is m clocks, the data is available nominally coincident with clock edge $n + m$.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

2.2.4　Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode.

All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.
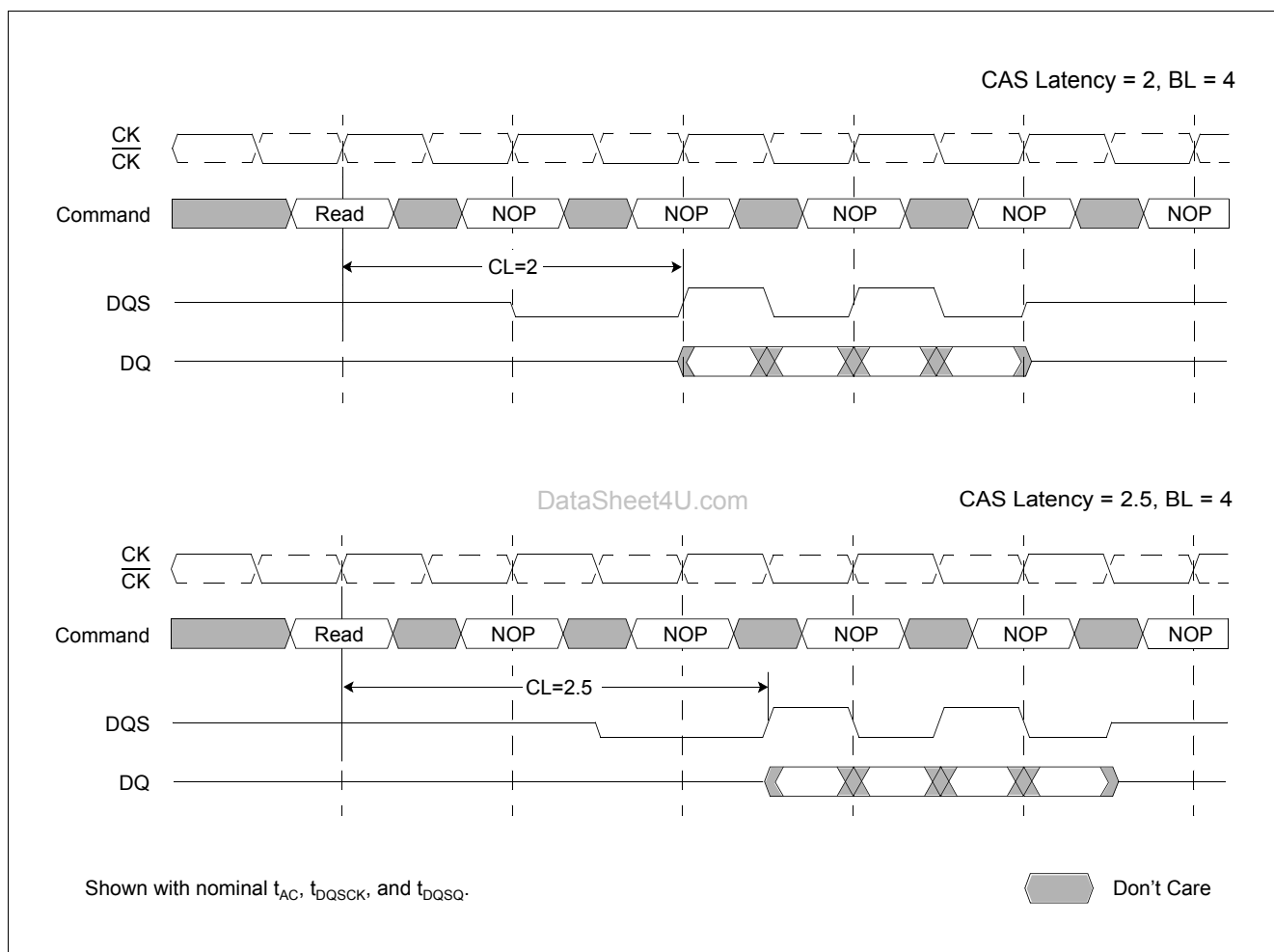
Figure 6　Required CAS Latencies

2.3 Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, and output drive strength selection. These functions are controlled via the bits shown in the Extended Mode Register Definition. The Extended Mode Register is programmed via the Mode Register Set command (with BA0 = 1 and BA1 = 0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements result in unspecified operation.

2.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur before a Read command can be issued. This is the reason 200 clock cycles must occur before issuing a Read or Write command upon exit of self refresh operation.

2.3.2 Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. In addition this design version supports a weak driver mode for lighter load and/or point-to-point environments which can be activated during mode register set. I-V curves for the normal and weak drive strength are included in this document.

EMR
Extended Mode Register Definition $(BA[1:0] = 01_B)$

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**1**					**Operating MODE**						**0**	**DS**	**DLL**
reg. addr						w						w	w	w

Field	Bits	Type[1]	Description
DLL	0	w	**DLL Status** See **Chapter 2.3.1**. 0 Enabled 1 Disabled
DS	1		**Drive Strength** See **Chapter 2.3.2**, **Chapter 3.2** and **Chapter 3.3**. 0 Normal 1 Weak
MODE	[12:3]		**Operating Mode** *Note:* 1. A2 must be 0 to provide compatibility with early DDR devices 2. *All other bit combinations are RESERVED.* 00000000000 Normal Operation

1) w = write only register bit

2.4 Commands

Deselect

The Deselect function prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The No Operation (NOP) command is used to perform a NOP to a DDR SDRAM. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Mode Register Set

The mode registers are loaded via inputs A0-A12, BA0 and BA1. See mode register descriptions in **Chapter 2.2**. The Mode Register Set command can only be issued when all banks are idle and no bursts are in progress. A subsequent executable command cannot be issued until t_{MRD} is met.

Active

The Active command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A12 selects the row. This row remains active (or open) for accesses until a Precharge (or Read or Write with Auto Precharge) is issued to that bank. A Precharge (or Read or Write with Auto Precharge) command must be issued and completed before opening a different row in the same bank.

Read

The Read command is used to initiate a burst read access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where [i = 8, j = don't care] for x16, [i = 9, j = don't care] for x8 and [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Read burst; if Auto Precharge is not selected, the row remains open for subsequent accesses.

Write

The Write command is used to initiate a burst write access to an active (open) row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-Ai, Aj (where[i = 8, j=don't care] for x16, where [i = 9, j = don't care] for x8; where [i = 9, j = 11] for x4) selects the starting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed is precharged at the end of the Write burst; if Auto Precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data is written to memory; if the DM signal is registered high, the corresponding data inputs are ignored, and a Write is not executed to that byte/column location.

Precharge

The Precharge command is used to deactivate (close) the open row in a particular bank or the open row(s) in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care". Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank. A precharge command is treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

Auto Precharge

Auto Precharge is a feature which performs the same individual-bank precharge functions described above, but without requiring an explicit command. This is accomplished by using A10 to enable Auto Precharge in conjunction with a specific Read or Write command. A precharge of the bank/row that is addressed with the Read or Write command is automatically performed upon completion of the Read or Write burst. Auto Precharge is nonpersistent in that it is either enabled or disabled for each individual Read or Write command. Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit Precharge command was issued at the earliest possible time, as described for each burst type in **Chapter 2.5**.

Burst Terminate

The Burst Terminate command is used to truncate read bursts (with Auto Precharge disabled). The most recently registered Read command prior to the Burst Terminate command is truncated, as shown in **Chapter 2.5**.

Auto Refresh

Auto Refresh is used during normal operation of the DDR SDRAM and is analogous to $\overline{CAS}$ Before $\overline{RAS}$ (CBR) Refresh in previous DRAM types. This command is nonpersistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The 512-Mbit Double-Data-Rate SDRAM requires Auto Refresh cycles at an average periodic interval of 7.8 µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto Refresh commands can be posted in the system, meaning that the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 9×7.8 µs (70.2 µs). This maximum absolute interval is short enough to allow for DLL updates internal to the DDR SDRAM to be restricted to Auto Refresh cycles, without allowing too much drift in t_{AC} between updates.

Self Refresh

The Self Refresh command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The Self Refresh command is initiated as an Auto Refresh command coincident with CKE transitioning low. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh (200 clock cycles must then occur before a Read command can be issued). Input signals except CKE (low) are "Don't Care" during Self Refresh operation. Since CKE is an SSTL_2 input , V_{REF} must be maintained during SELF REFRESH.

The procedure for exiting self refresh requires a sequence of commands. CK (and $\overline{CK}$) must be stable prior to CKE returning high. Once CKE is high, the SDRAM must have NOP commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for 200 clock cycles before applying any other command.

Table 5   Truth Table 1a: Commands

Name (Function)	CS	RAS	CAS	WE	Address	MNE	Notes
Deselect (NOP)	H	X	X	X	X	NOP	1)2)
No Operation (NOP)	L	H	H	H	X	NOP	1)2)
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	ACT	1)3)
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	Read	1)4)
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	Write	1)4)
Burst Terminate	L	H	H	L	X	BST	1)5)
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	PRE	1)6)
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	AR/SR	1)7)8)
Mode Register Set	L	L	L	L	Op-Code	MRS	1)9)

1) CKE is HIGH for all commands shown exceptSelf Refresh.
V_{REF} must be maintained during Self Refresh operation.

2) Deselect and NOP are functionally interchangeable.

3) BA0-BA1 provide bank address and A0-A12 provide row address.

4) BA0, BA1 provide bank address; A0-Ai provide column address (where i = 8 for x16, i = 9 for x8 and 9, 11 for x4);
A10 HIGH enables the Auto Precharge feature (nonpersistent), A10 LOW disables the Auto Precharge feature.

5) Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts.

6) A10 LOW: BA0, BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0, BA1 are "Don't Care".

7) This command is AUTO REFRESH if CKE is HIGH; Self Refresh if CKE is LOW.

8) Internal refresh counter controls row and bank addressing; all inputs and I/Os are "Don't Care" except for CKE.

9) BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A12 provide the op-code to be written to the selected Mode Register).

Table 6   Truth Table 1b: DM Operation

Name (Function)	DM	DQs	Notes
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

1) Used to mask write data; provided coincident with the corresponding data.

2.5 Operations

2.5.1 Bank/Row Activation

Before any Read or Write commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened" (activated). This is accomplished via the Active command and addresses A0-A12, BA0 and BA1 (see **Figure 7**), which decode and select both the bank and the row to be activated. After opening a row (issuing an Active command), a Read or Write command may be issued to that row, subject to the t_{RCD} specification. A subsequent Active command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive Active commands to the same bank is defined by t_{RC}. A subsequent Active command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive Active commands to different banks is defined by t_{RRD}.
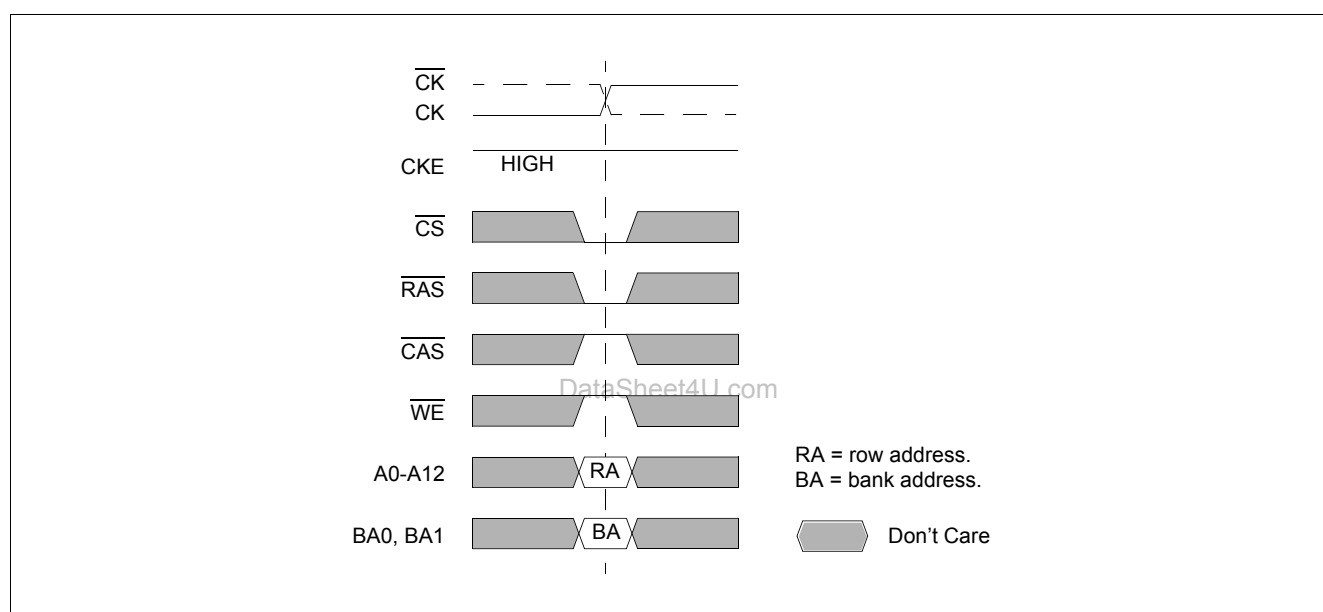
Figure 7   Activating a Specific Row in a Specific Bank
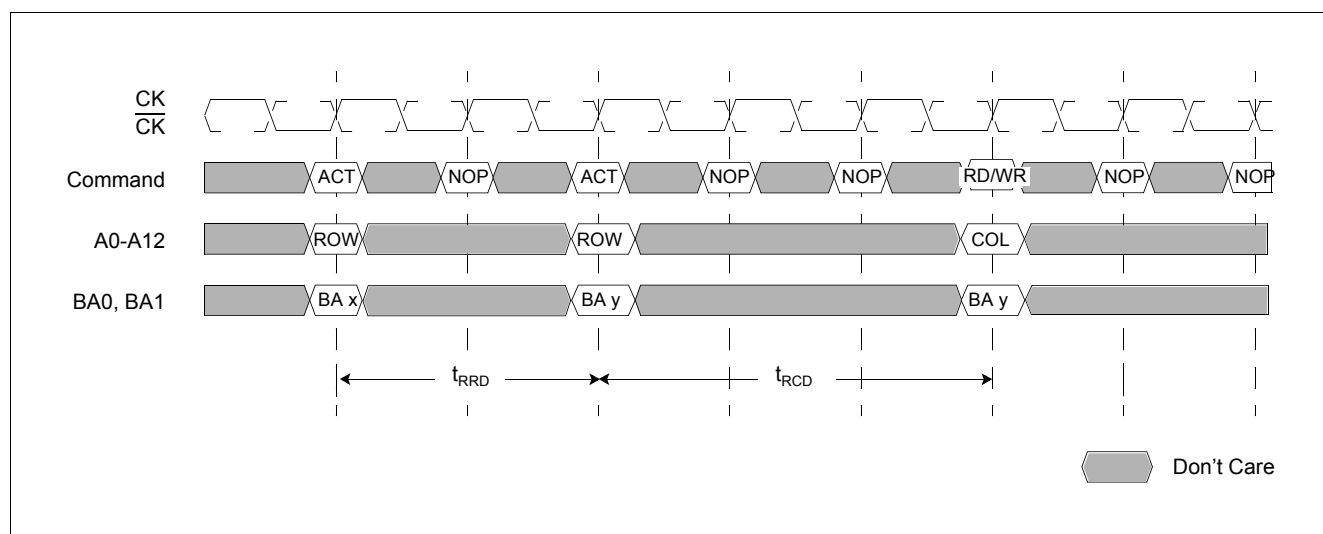
Figure 8 t_{RCD} and t_{RRD} Definition

2.5.2 Reads

Subsequent to programming the mode register with CAS latency, burst type, and burst length, Read bursts are initiated with a Read command, as shown on **Figure 9**.

The starting column and bank addresses are provided with the Read command and Auto Precharge is either enabled or disabled for that burst access. If Auto Precharge is enabled, the row that is accessed starts precharge at the completion of the burst, provided t_{RAS} has been satisfied. For the generic Read commands used in the following illustrations, Auto Precharge is disabled.

During Read bursts, the valid data-out element from the starting column address is available following the CAS latency after the Read command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (i.e. at the next crossing of CK and $\overline{CK}$). **Figure 10** shows general timing for each supported CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial low state on DQS is known as the read preamble; the low state coincident with the last data-out element is known as the read postamble. Upon completion of a burst, assuming no other commands have been initiated, the DQs goes High-Z. Data from any Read burst may be concatenated with or truncated with data from a subsequent Read command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Read command should be issued x cycles after the first Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown on **Figure 11**. A Read command can be initiated on any clock cycle following a previous Read command. Nonconsecutive Read data is illustrated on **Figure 12**. Full-speed Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8) within a page (or pages) can be performed as shown on **Figure 13**.
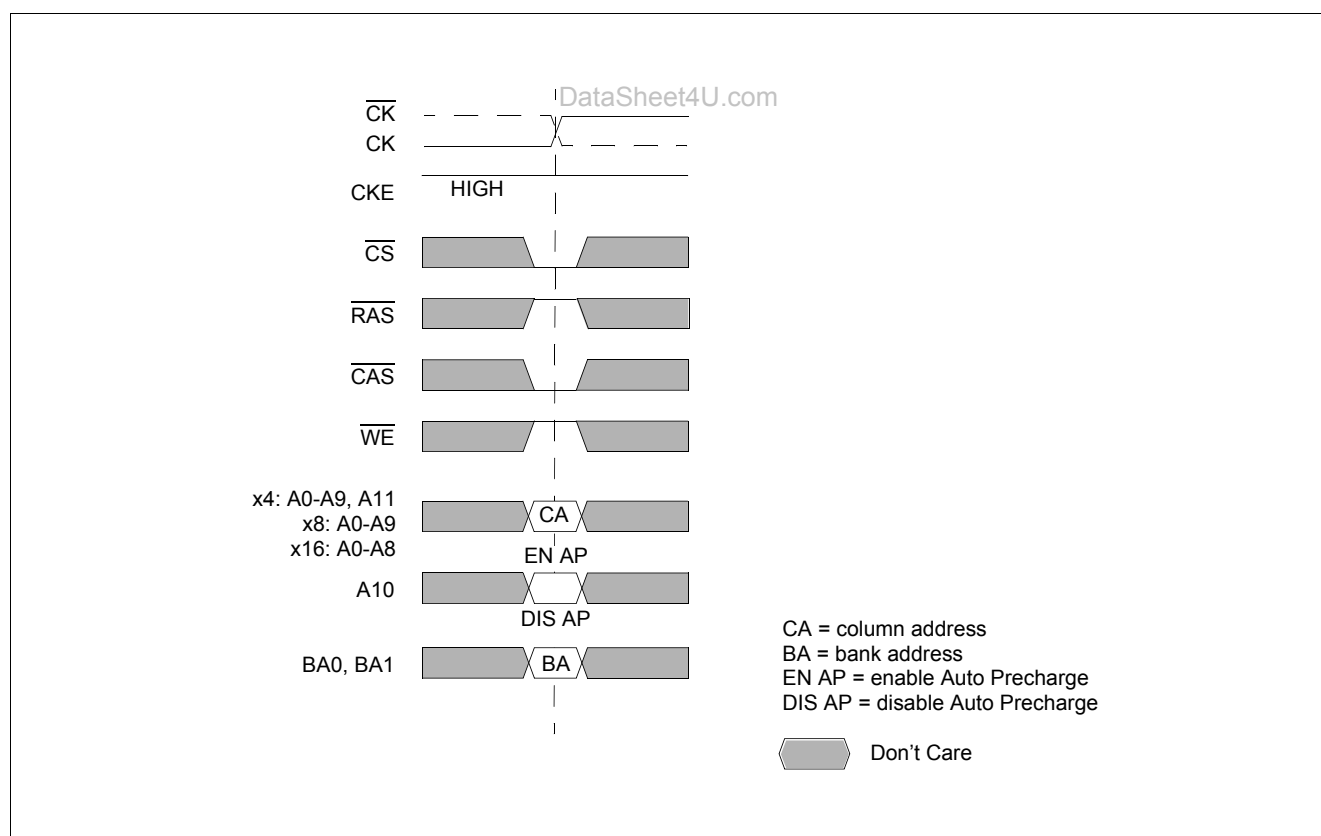
Figure 9   Read Command
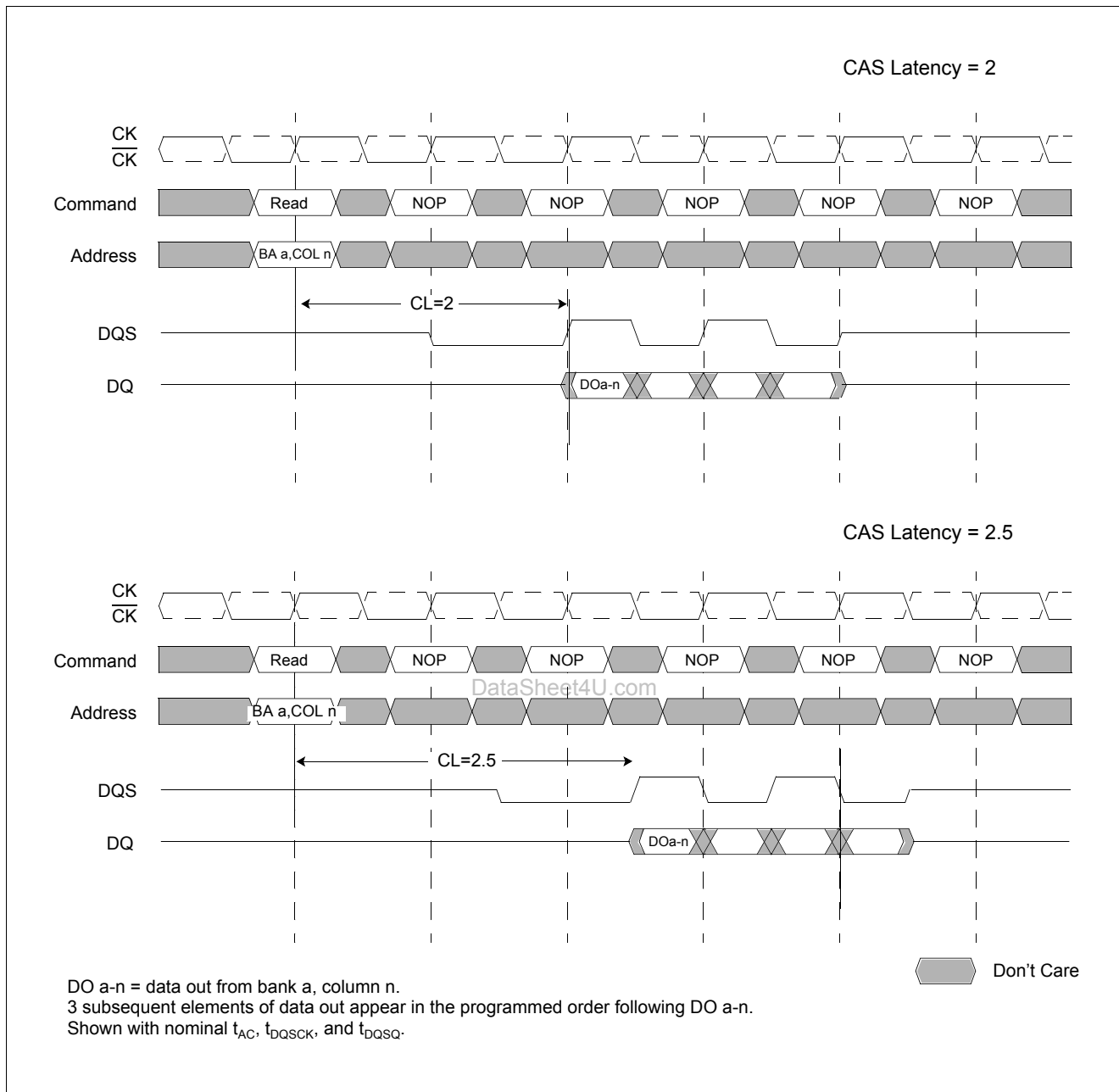
Figure 10   Read Burst: CAS Latencies (Burst Length = 4)

CAS Latency = 2

CAS Latency = 2.5

DO a-*n* (or a-*b*) = data out from bank a, column *n* (or bank a, column *b*).
When burst length = 4, the bursts are concatenated.
When burst length = 8, the second burst interrupts the first.
3 subsequent elements of data out appear in the programmed order following DO a-*n*.
3 (or 7) subsequent elements of data out appear in the programmed order following DO a-*b*.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care

Figure 11   Consecutive Read Bursts: CAS Latencies (Burst Length = 4 or 8)
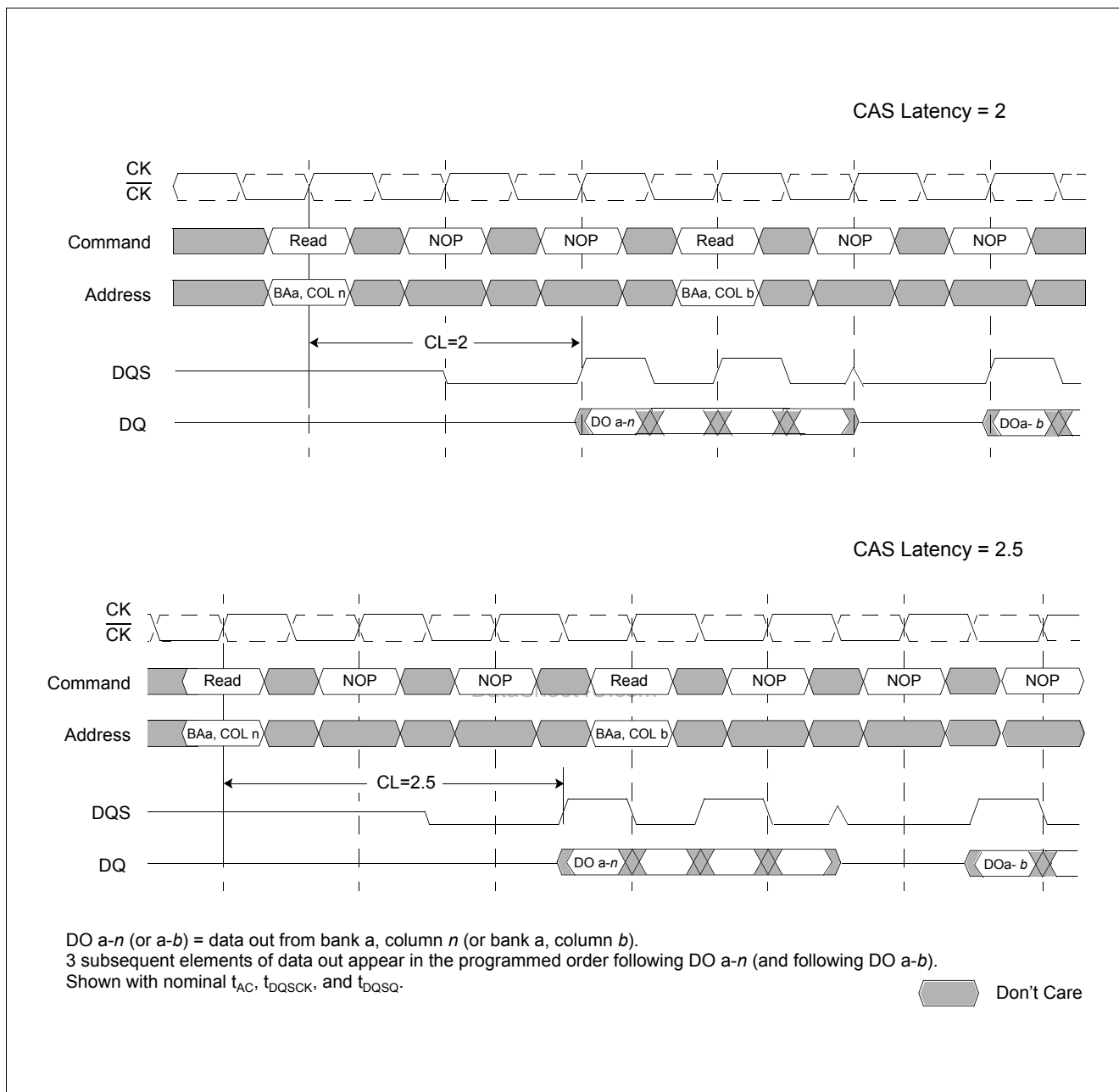
Figure 12   Non-Consecutive Read Bursts: CAS Latencies (Burst Length = 4)
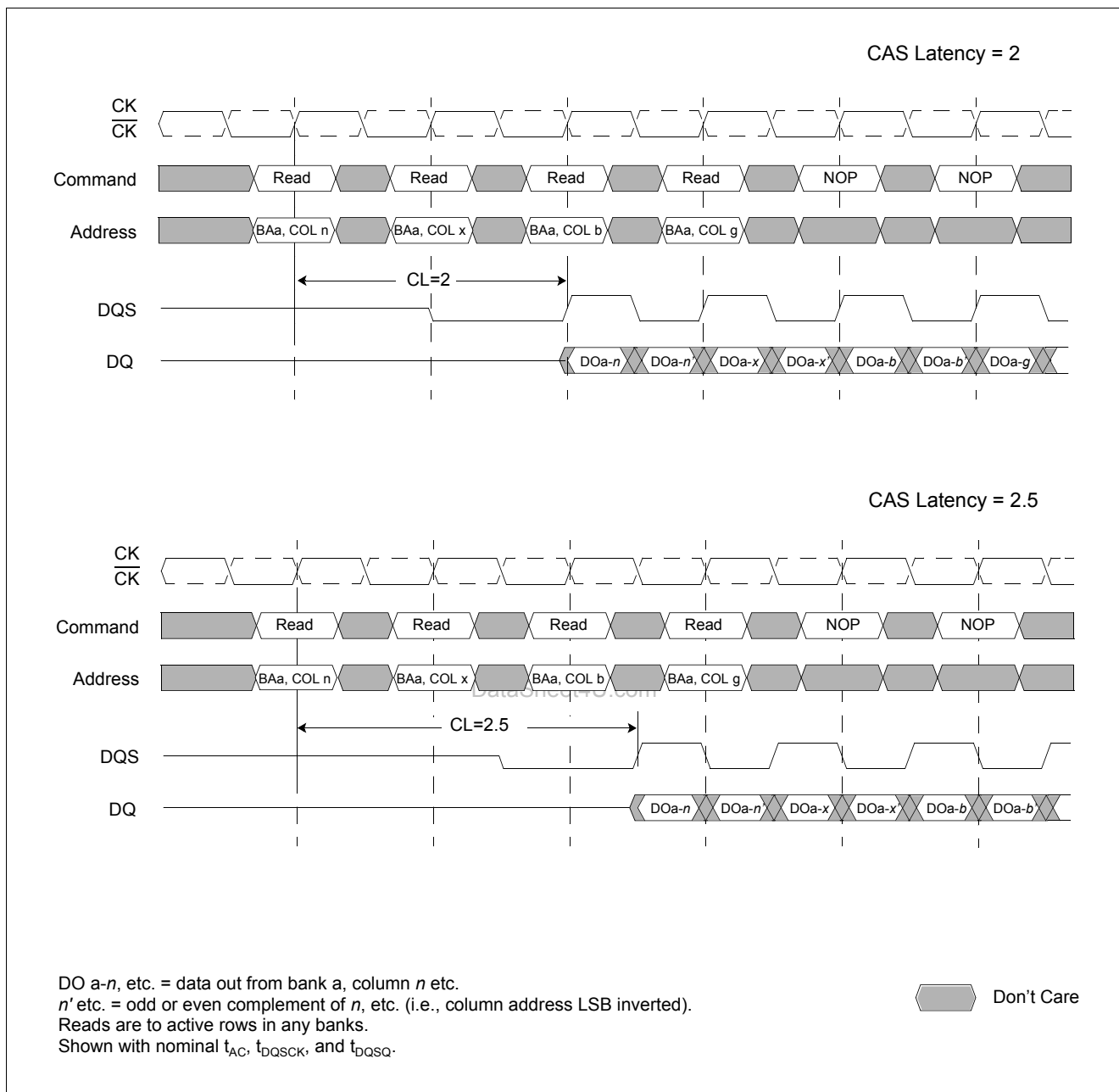
Figure 13   Random Read Accesses: CAS Latencies (Burst Length = 2, 4 or 8)

Data from any Read burst may be truncated with a Burst Terminate command, as shown on **Figure 14**. The Burst Terminate latency is equal to the read (CAS) latency, i.e. the Burst Terminate command should be issued x cycles after the Read command, where x equals the number of desired data element pairs.

Data from any Read burst must be completed or truncated before a subsequent Write command can be issued. If truncation is necessary, the Burst Terminate command must be used, as shown on **Figure 15**. The example is shown for $t_{DQSS(min)}$. The $t_{DQSS(max)}$ case, not shown here, has a longer bus idle time. $t_{DQSS(min)}$ and $t_{DQSS(max)}$ are defined in **Chapter 2.5.3**.

A Read burst may be followed by, or truncated with, a Precharge command to the same bank (provided that Auto Precharge was not activated). The Precharge command should be issued x cycles after the Read command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). This is shown on **Figure 16** for Read latencies of 2 and 2.5. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data elements.

In the case of a Read being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same Read burst with Auto Precharge enabled. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.

Functional Description
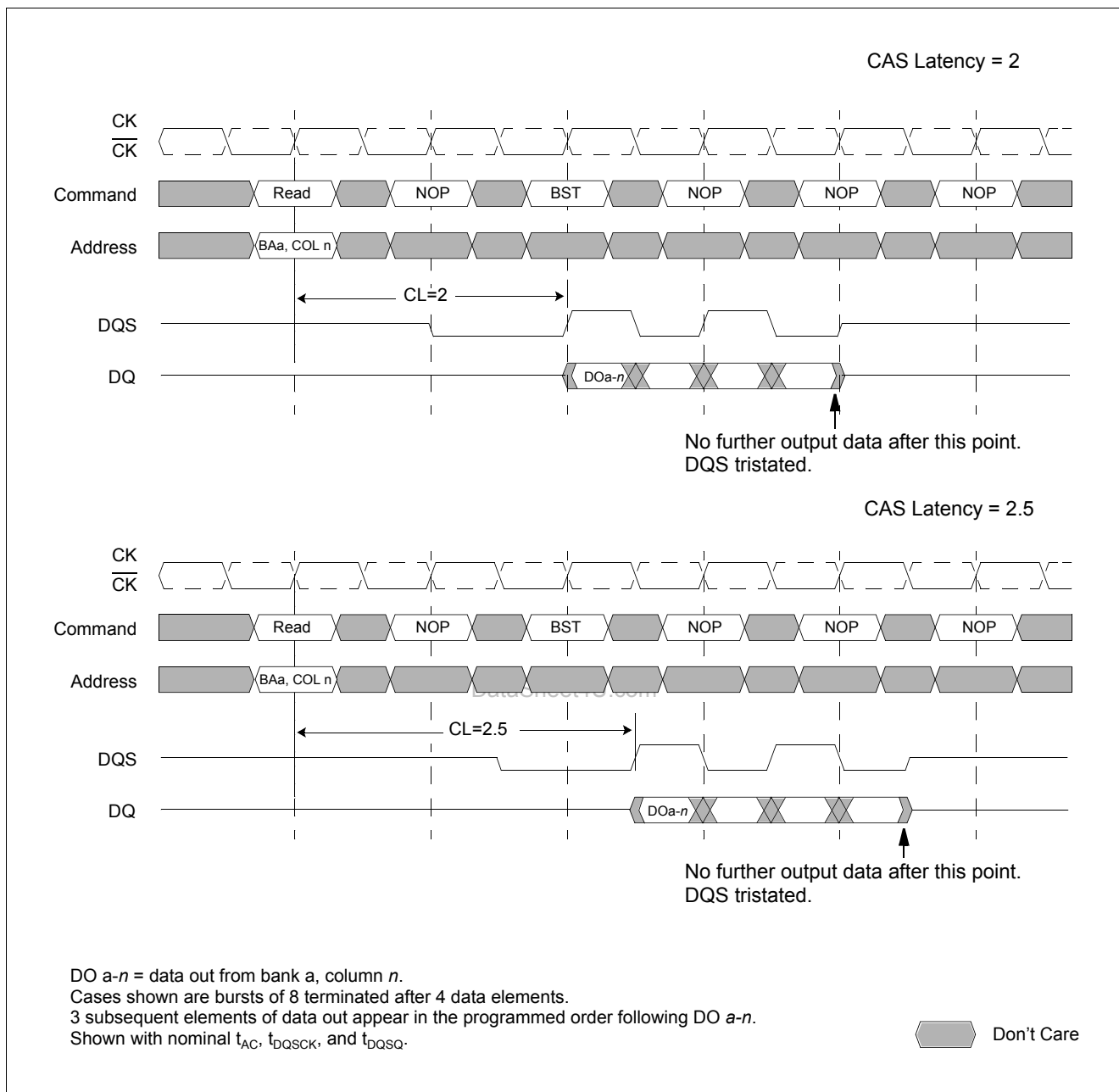
Figure 14   Terminating a Read Burst: CAS Latencies (Burst Length = 8)

Figure 15   Read to Write: CAS Latencies (Burst Length = 4 or 8)

DO a-*n* = data out from bank a, column *n*
DI a-*b* = data in to bank a, column *b*
1 subsequent elements of data out appear in the programmed order following DO a-*n*.
Data In elements are applied following DI a-b in the programmed order, according to burst length.
Shown with nominal t_{AC}, t_{DQSCK}, and t_{DQSQ}.

Don't Care
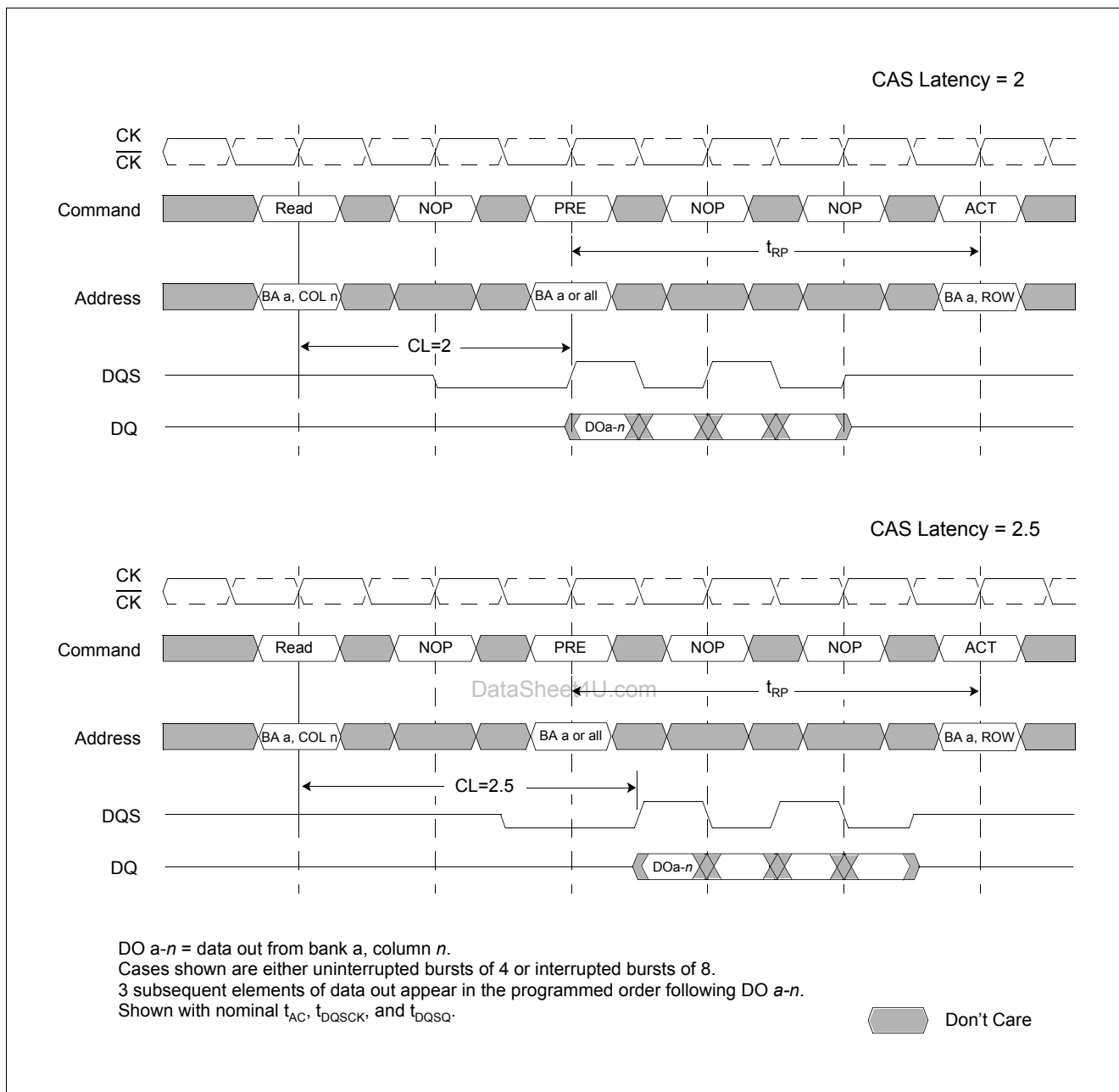
Figure 16   Read to Precharge: CAS Latencies (Burst Length = 4 or 8)

2.5.3 Writes

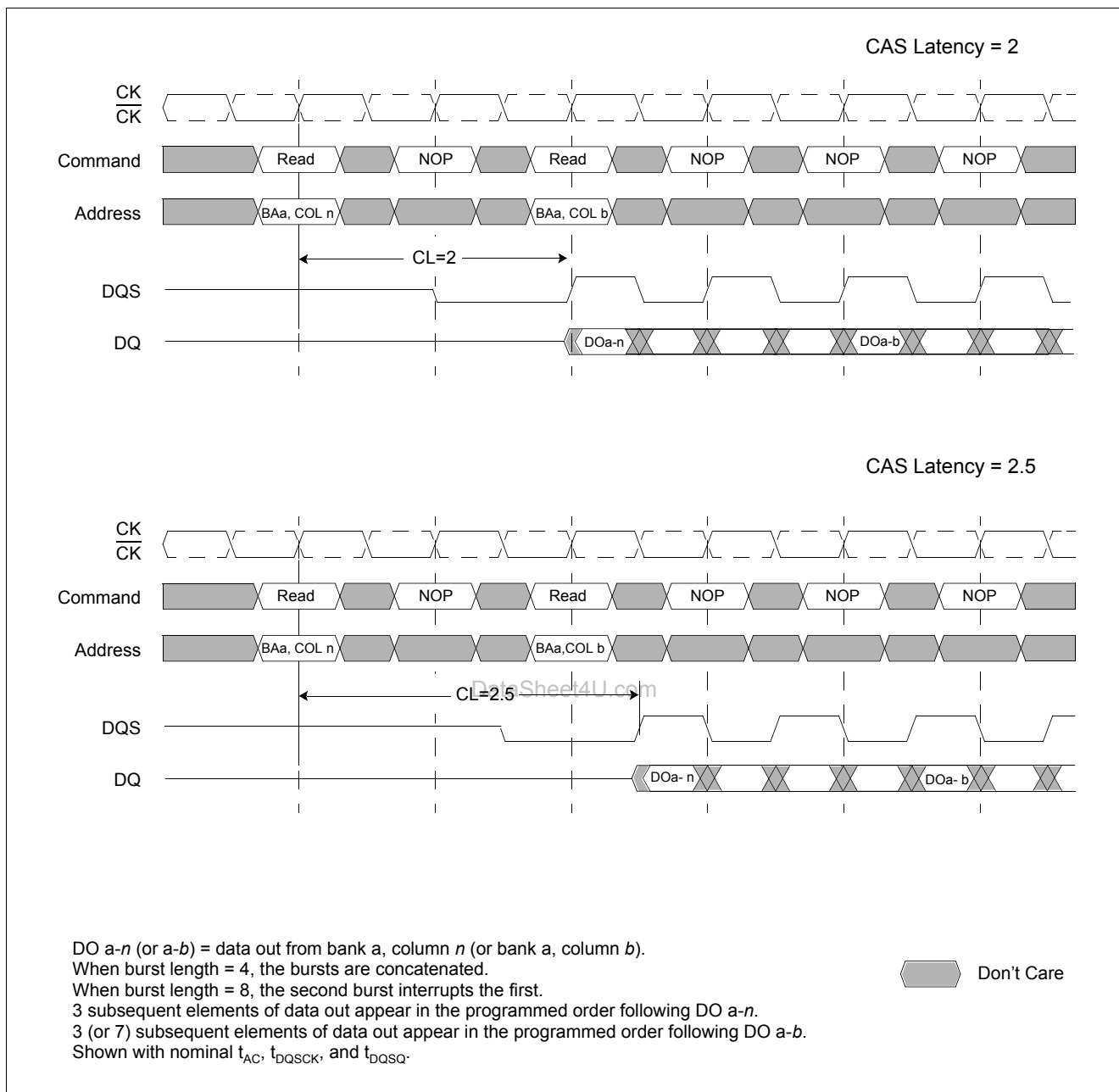Write bursts are initiated with a Write command, as shown in **Figure 17**.

The starting column and bank addresses are provided with the Write command, and Auto Precharge is either enabled or disabled for that access. If Auto Precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic Write commands used in the following illustrations, Auto Precharge is disabled.

During Write bursts, the first valid data-in element is registered on the first rising edge of DQS following the write command, and subsequent data elements are registered on successive edges of DQS. The Low state on DQS between the Write command and the first rising edge is known as the write preamble; the Low state on DQS following the last data-in element is known as the write postamble. The time between the Write command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of one clock cycle), so most of the Write diagrams that follow are drawn for the two extreme cases (i.e. $t_{DQSS(min)}$ and $t_{DQSS(max)}$). **Figure 18** shows the two extremes of t_{DQSS} for a burst of four. Upon completion of a burst, assuming no other commands have been initiated, the DQs and DQS enters High-Z and any additional input data is ignored.

Data for any Write burst may be concatenated with or truncated with a subsequent Write command. In either case, a continuous flow of input data can be maintained. The new Write command can be issued on any positive edge of clock following the previous Write command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new Write command should be issued x cycles after the first Write command, where x equals the number of desired data element pairs (pairs are required by the 2n prefetch architecture). **Figure 19** shows concatenated bursts of 4. An example of non-consecutive Writes is shown in **Figure 20**. Full-speed random write accesses within a page or pages can be performed as shown in **Figure 21**. Data for any Write burst may be followed by a subsequent Read command. To follow a Write without truncating the write burst, t_{WTR} (Write to Read) should be met as shown in **Figure 22**.

Data for any Write burst may be truncated by a subsequent Read command, as shown in **Figure 23** to **Figure 25**. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in must be masked with DM, as shown in the diagrams noted previously.

Data for any Write burst may be followed by a subsequent Precharge command. To follow a Write without truncating the write burst, t_{WR} should be met as shown in **Figure 26**.

Data for any Write burst may be truncated by a subsequent Precharge command, as shown in **Figure 27** to **Figure 29**. Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data in should be masked with DM. Following the Precharge command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

In the case of a Write burst being executed to completion, a Precharge command issued at the optimum time (as described above) provides the same operation that would result from the same burst with Auto Precharge. The disadvantage of the Precharge command is that it requires that the command and address busses be available at the appropriate time to issue the command. The advantage of the Precharge command is that it can be used to truncate bursts.
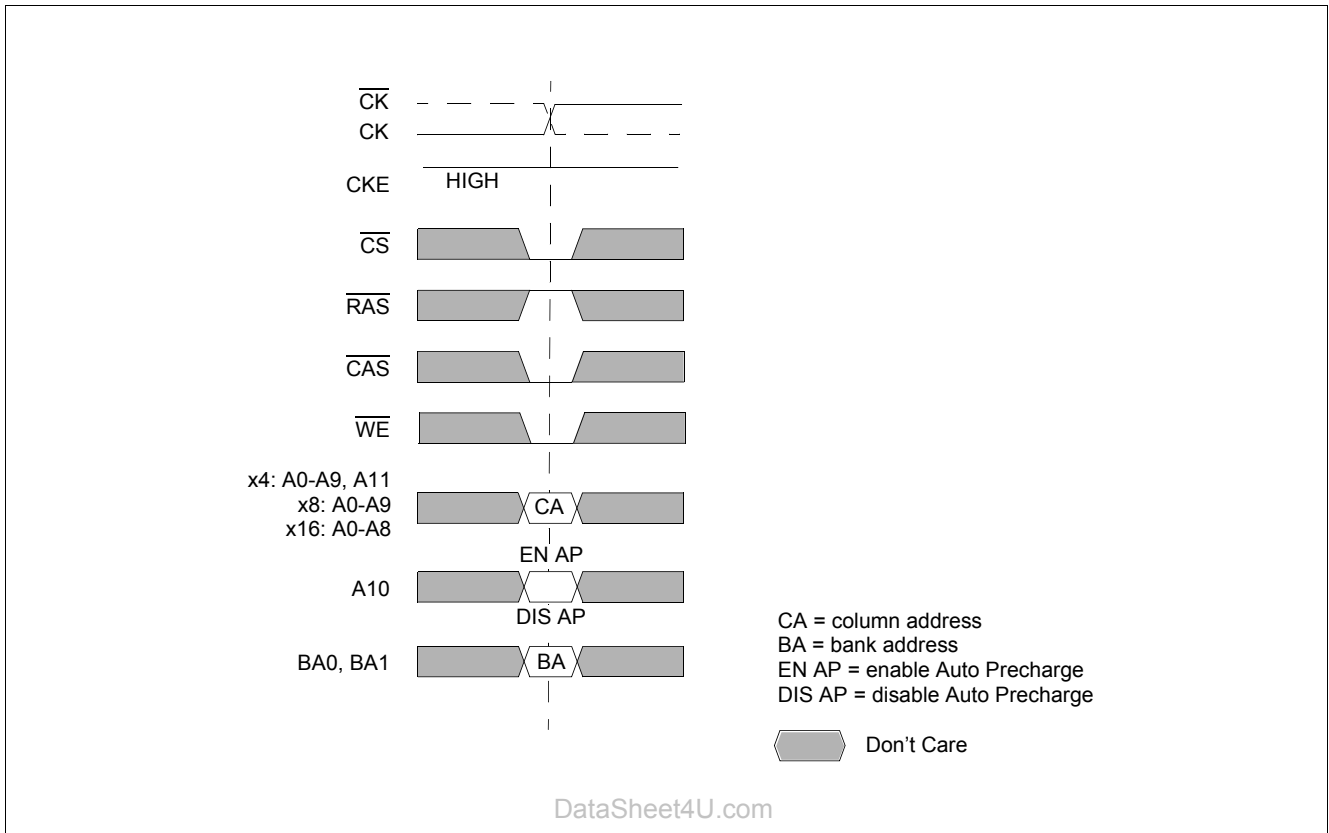
Figure 17   Write Command
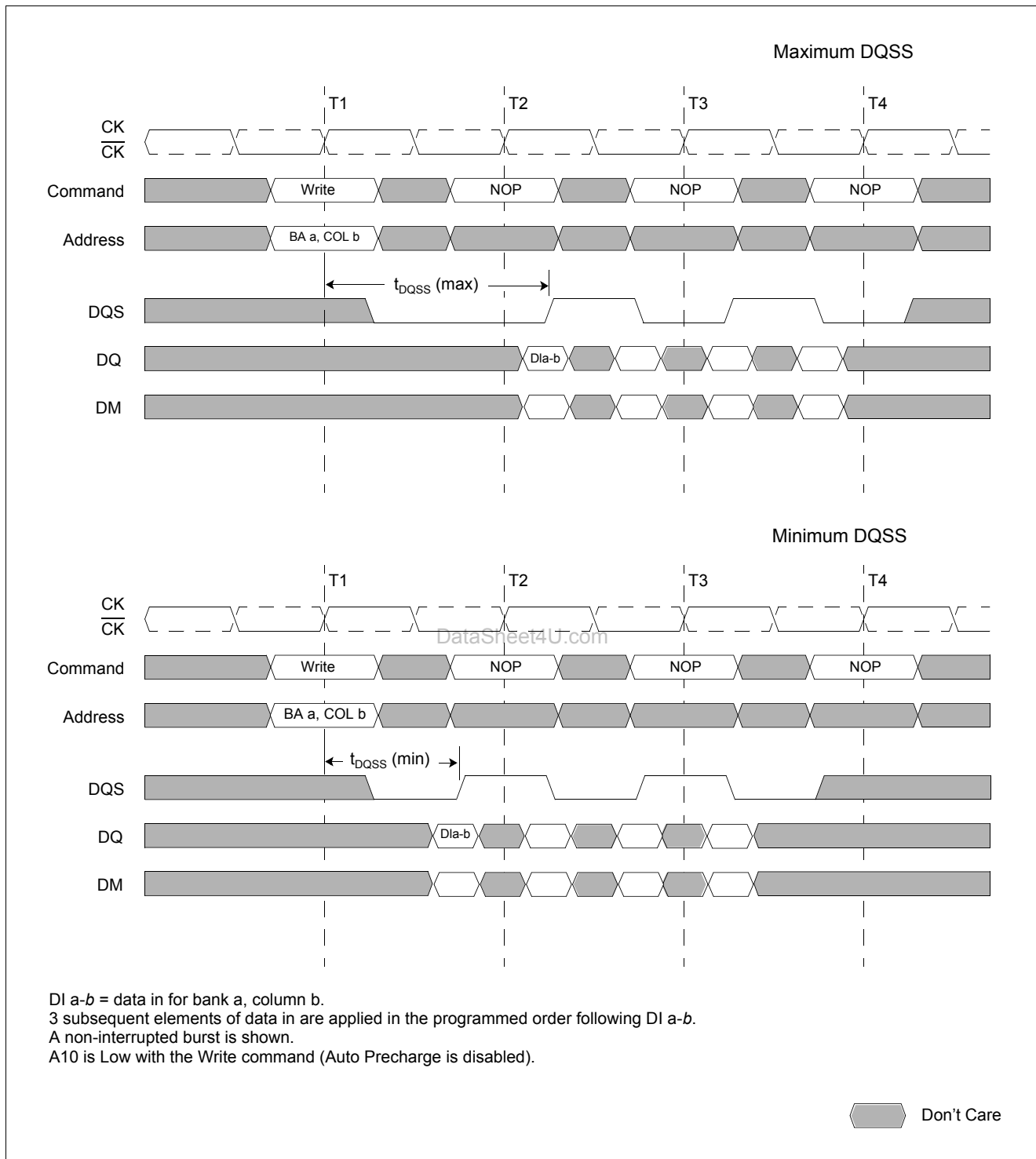
Figure 18   Write Burst (Burst Length = 4)
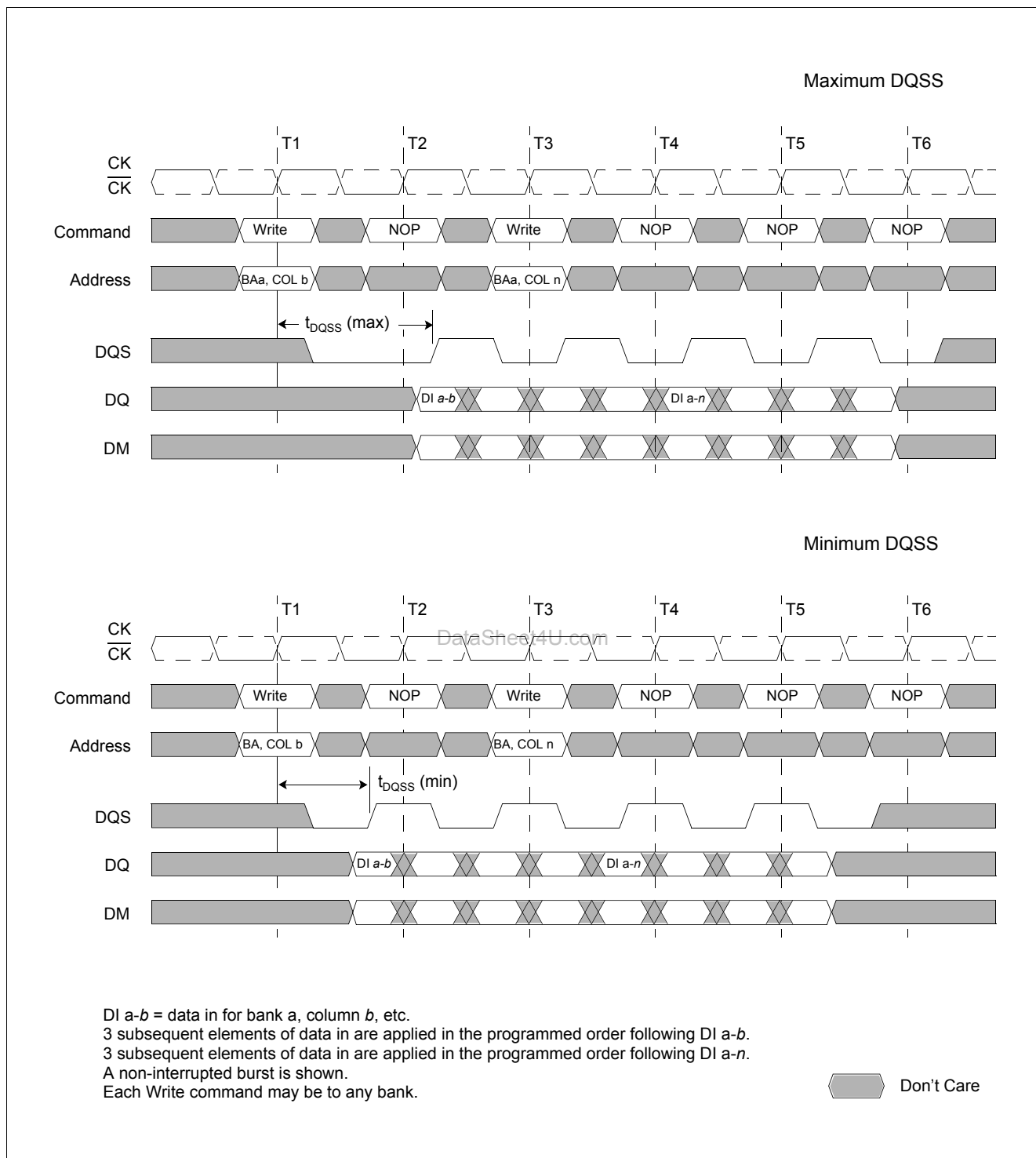
Figure 19   Write to Write (Burst Length = 4)
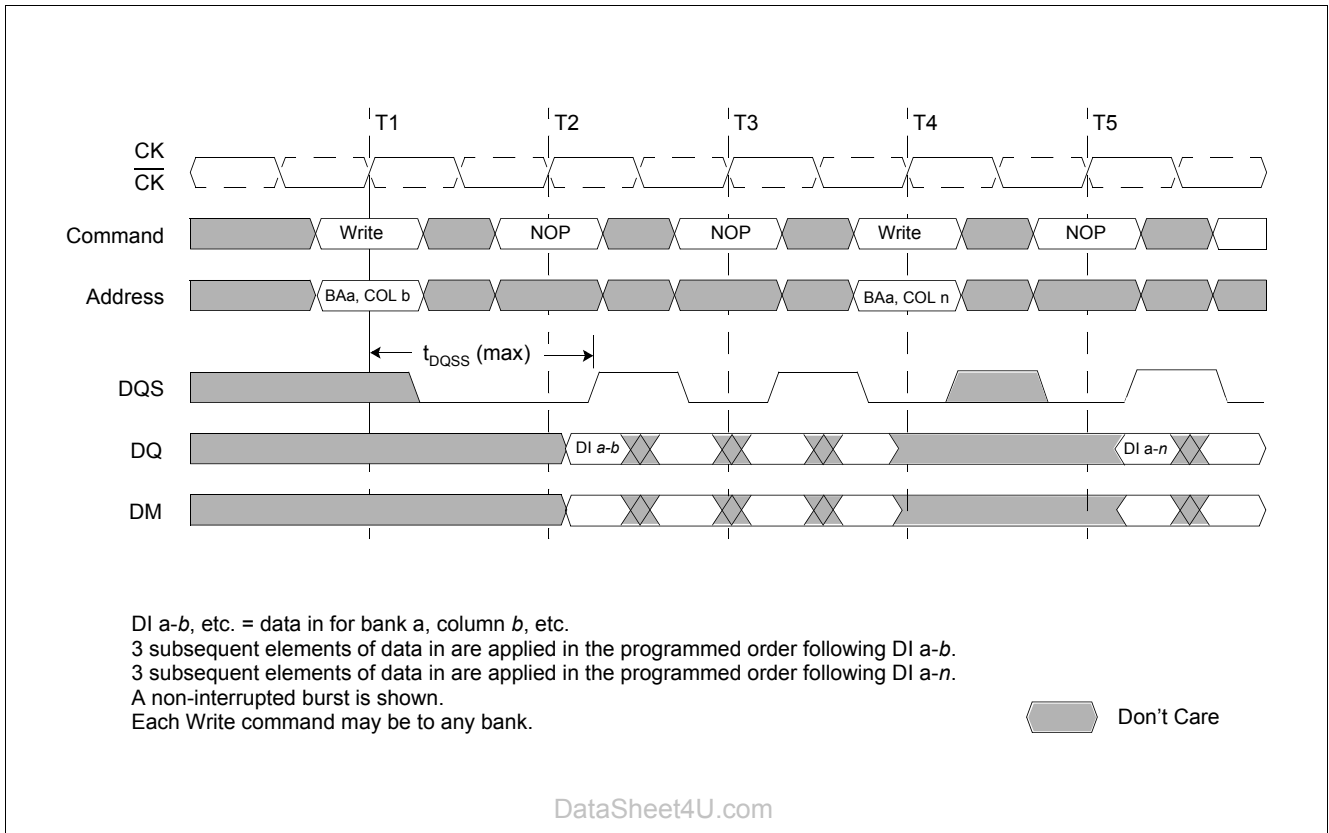
Figure 20   Write to Write: Max. DQSS, Non-Consecutive (Burst Length = 4)
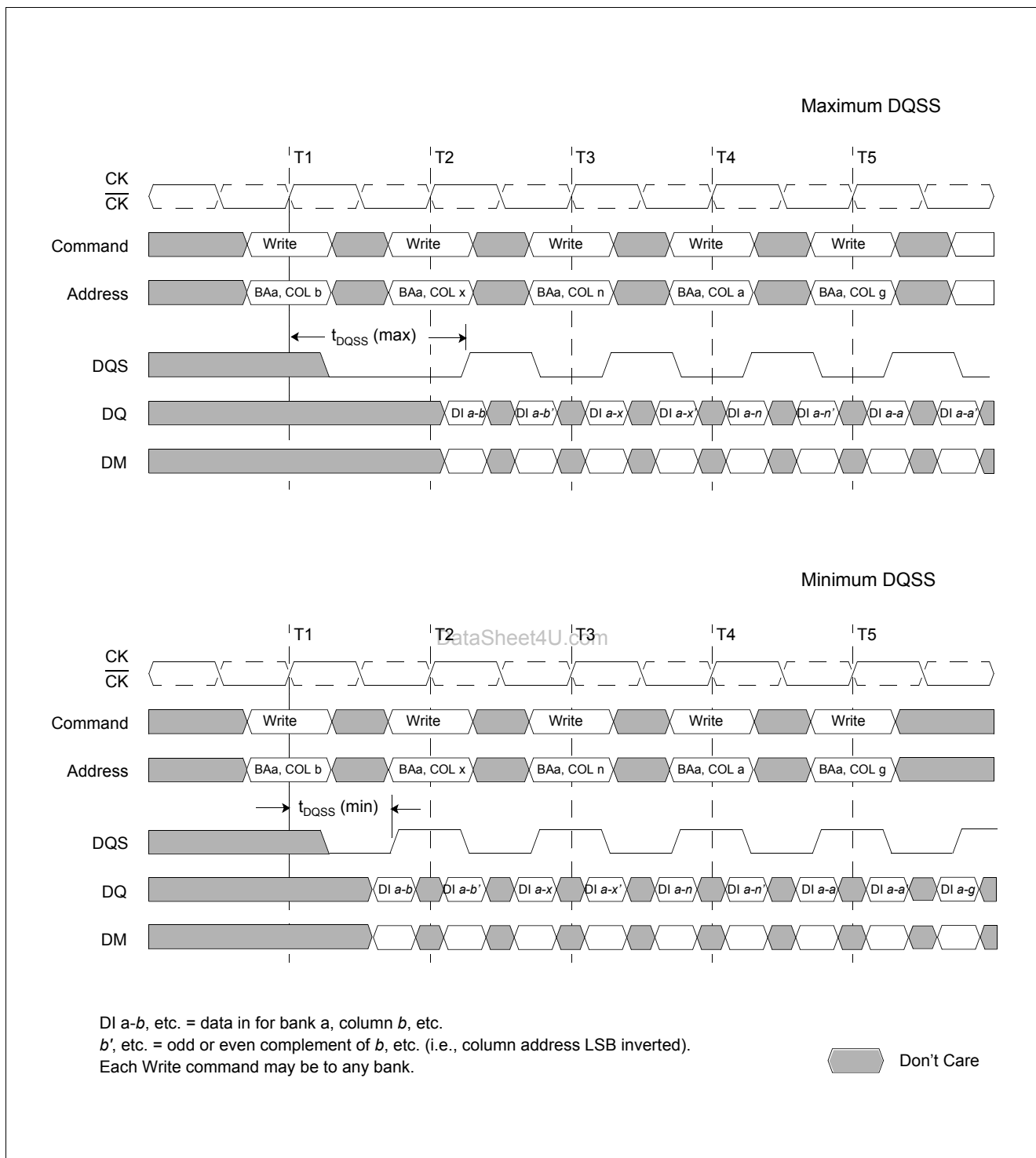
Figure 21   Random Write Cycles (Burst Length = 2, 4 or 8)

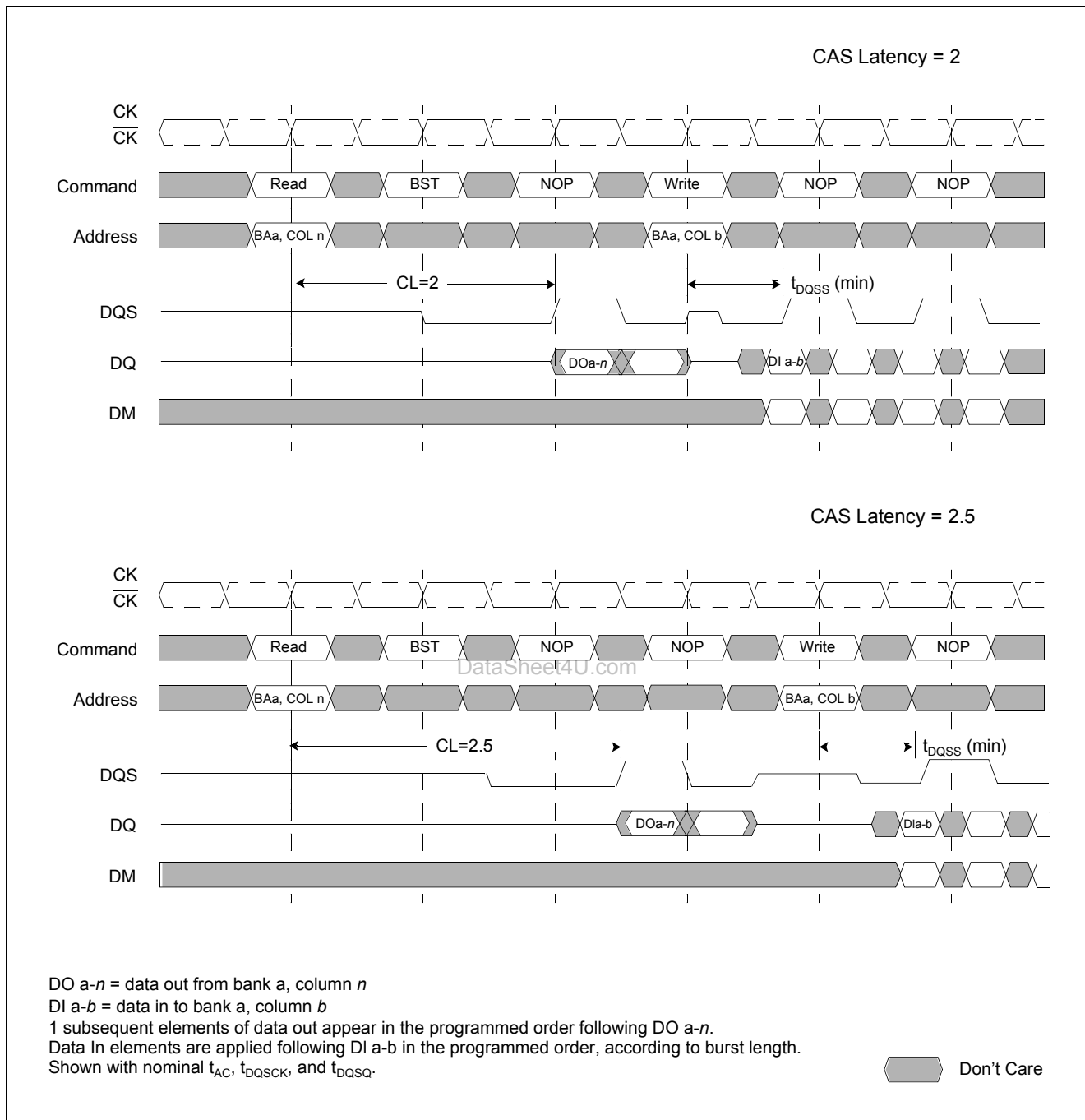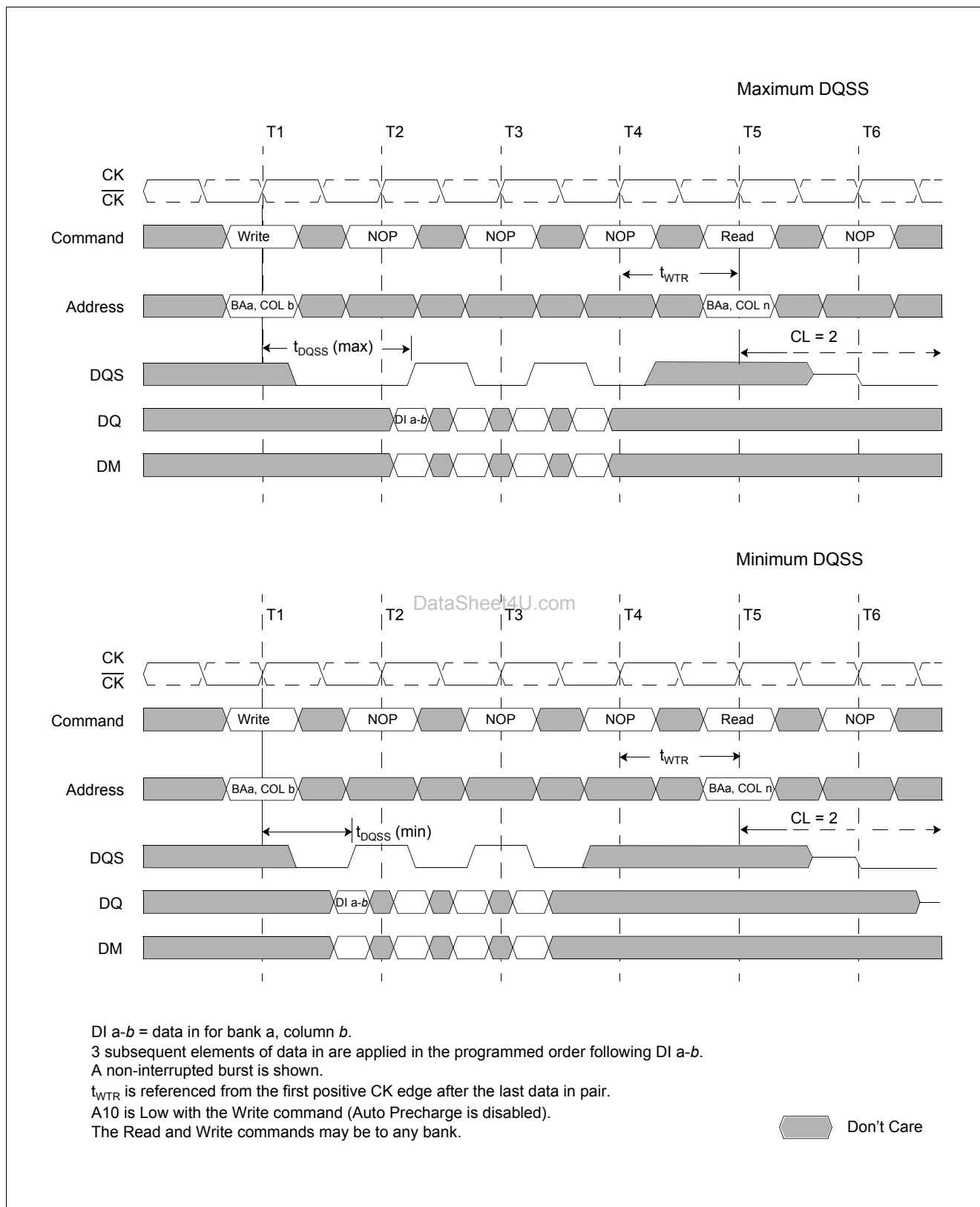**Figure 22   Write to Read: Non-Interrupting (CAS Latency = 2; Burst Length = 4)**

Functional Description

DI a-*b* = data in for bank a, column *b*.

An interrupted burst is shown, 4 data elements are written.

3 subsequent elements of data in are applied in the programmed order following DI a-*b*.

t_{WTR} is referenced from the first positive CK edge after the last data in pair.

The Read command masks the last 2 data elements in the burst.

A10 is Low with the Write command (Auto Precharge is disabled).

The Read and Write commands are not necessarily to the same bank.

1 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Figure 23   Write to Read: Interrupting (CAS Latency = 2; Burst Length = 8)

Functional Description

DI a-*b* = data in for bank a, column *b*.

An interrupted burst is shown, 3 data elements are written.

2 subsequent elements of data in are applied in the programmed order following DI *a-b*.

t_{WTR} is referenced from the first positive CK edge after the last desired data in pair (not the last desired data in element)

The Read command masks the last 2 data elements in the burst.

A10 is Low with the Write command (Auto Precharge is disabled).

The Read and Write commands are not necessarily to the same bank.

1 = This bit is correctly written into the memory array if DM is low.

2 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Figure 24   Write to Read: Min. DQSS, Odd Number of Data (3-bit Write), Interrupting (CL = 2; BL = 8)
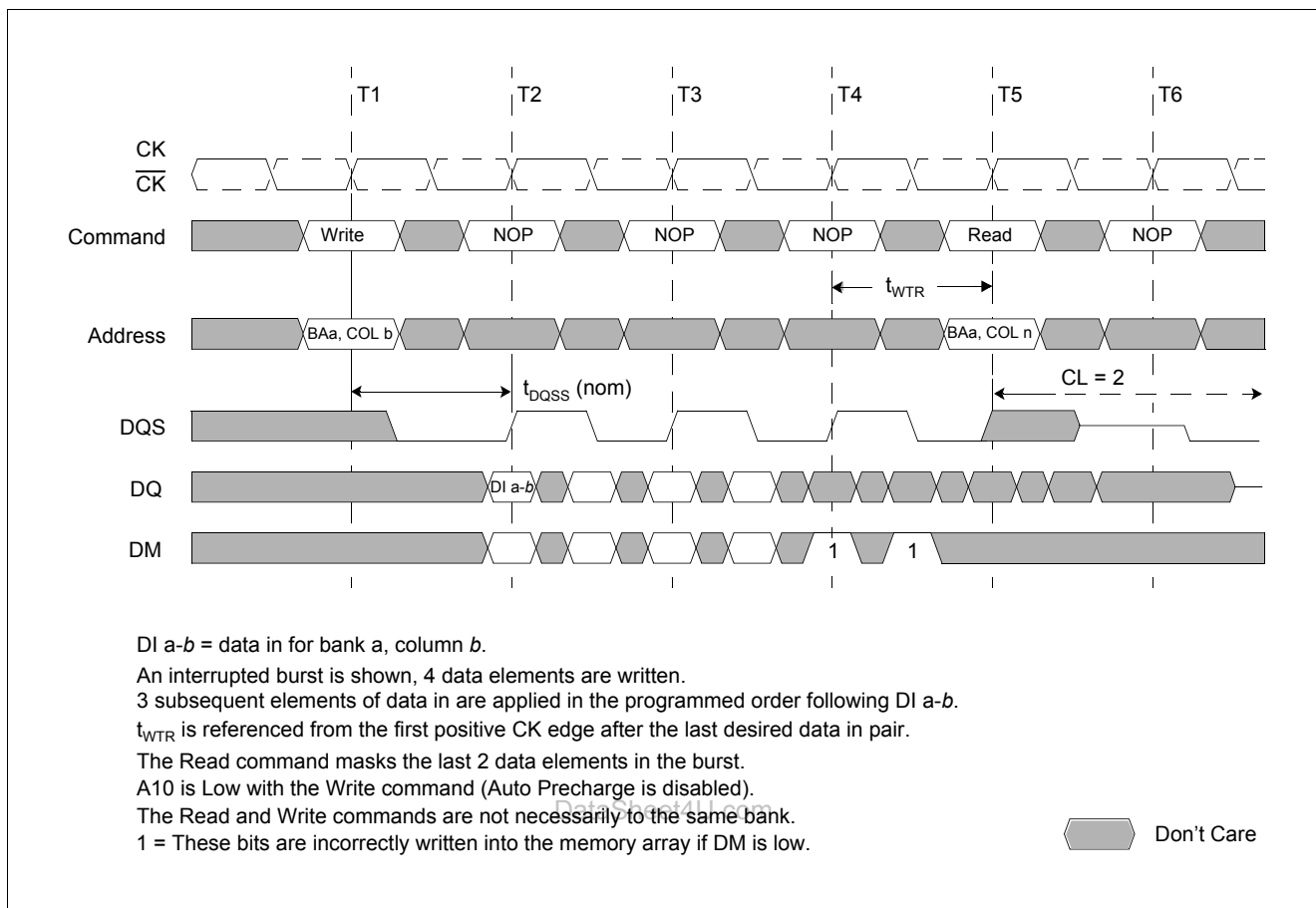
Figure 25   Write to Read: Nominal DQSS, Interrupting (CAS Latency = 2; Burst Length = 8)

Figure 26   Write to Precharge: Non-Interrupting (Burst Length = 4)

DI a-*b* = data in for bank a, column *b*.
3 subsequent elements of data in are applied in the programmed order following DI a-*b*.
A non-interrupted burst is shown.
t_{WR} is referenced from the first positive CK edge after the last data in pair.
A10 is Low with the Write command (Auto Precharge is disabled).

Figure 27   Write to Precharge: Interrupting (Burst Length = 4 or 8)

DI a-b = data in for bank a, column b.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI a-b.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst, for burst length = 8.

A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Figure 28   Write to Precharge: Min. DQSS, Odd Number of Data (1-bit Write), Interrupting (BL = 4 or 8)

DI a-*b* = data in for bank a, column *b*.

An interrupted burst is shown, 1 data element is written.

t_{WR} is referenced from the first positive CK edge after the last desired data in pair.

The Precharge command masks the last 2 data elements in the burst.

A10 is Low with the Write command (Auto Precharge is disabled).

1 = Can be don't care for programmed burst length of 4.

2 = For programmed burst length of 4, DQS becomes don't care at this point.

3 = This bit is correctly written into the memory array if DM is low.

4 = These bits are incorrectly written into the memory array if DM is low.

Don't Care

Figure 29   Write to Precharge: Nominal DQSS (2-bit Write), Interrupting (Burst Length = 4 or 8)

DI a-*b* = Data In for bank a, column *b*.
An interrupted burst is shown, 2 data elements are written.
1 subsequent element of data in is applied in the programmed order following DI *a-b*.
t_{WR} is referenced from the first positive CK edge after the last desired data in pair.
The Precharge command masks the last 2 data elements in the burst.
A10 is Low with the Write command (Auto Precharge is disabled).
1 = Can be don't care for programmed burst length of 4.
2 = For programmed burst length of 4, DQS becomes don't care at this point.
3 = These bits are incorrectly written into the memory array if DM is low.

2.5.4 Precharge

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the Precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care". Once a bank has been precharged, it is in the idle state and must be activated prior to any Read or Write commands being issued to that bank.
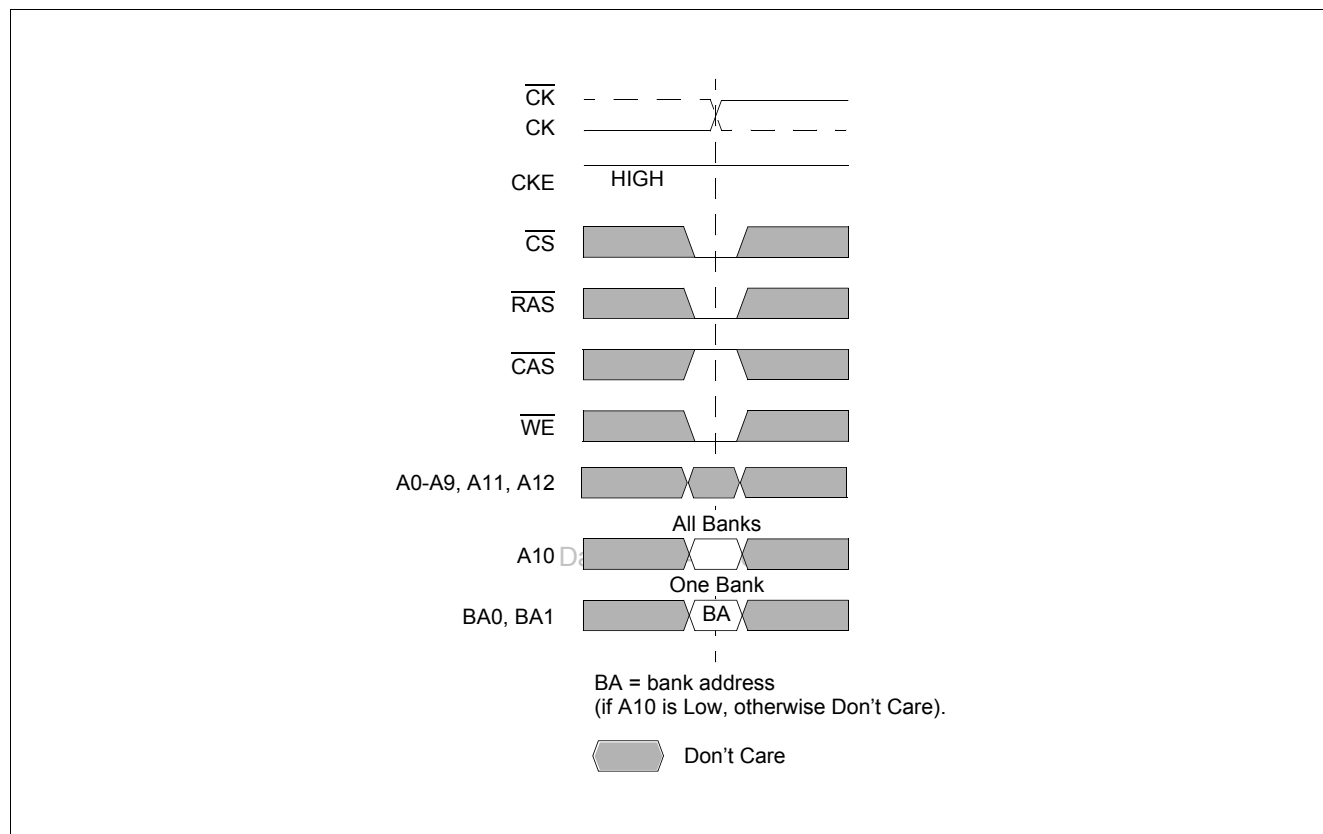
Figure 30   Precharge Command

2.5.5 Power-Down

Power-down is entered when CKE is registered LOW (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK and CKE. The DLL is still running in Power Down mode, so for maximum power savings, the user has the option of disabling the DLL prior to entering Power-down. In that case, the DLL must be enabled after exiting power-down, and 200 clock cycles must occur before a Read command can be issued. In power-down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR SDRAM, and all other input signals are "Don't Care". However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled power-down mode.

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or Deselect command). A valid, executable command may be applied one clock cycle later.
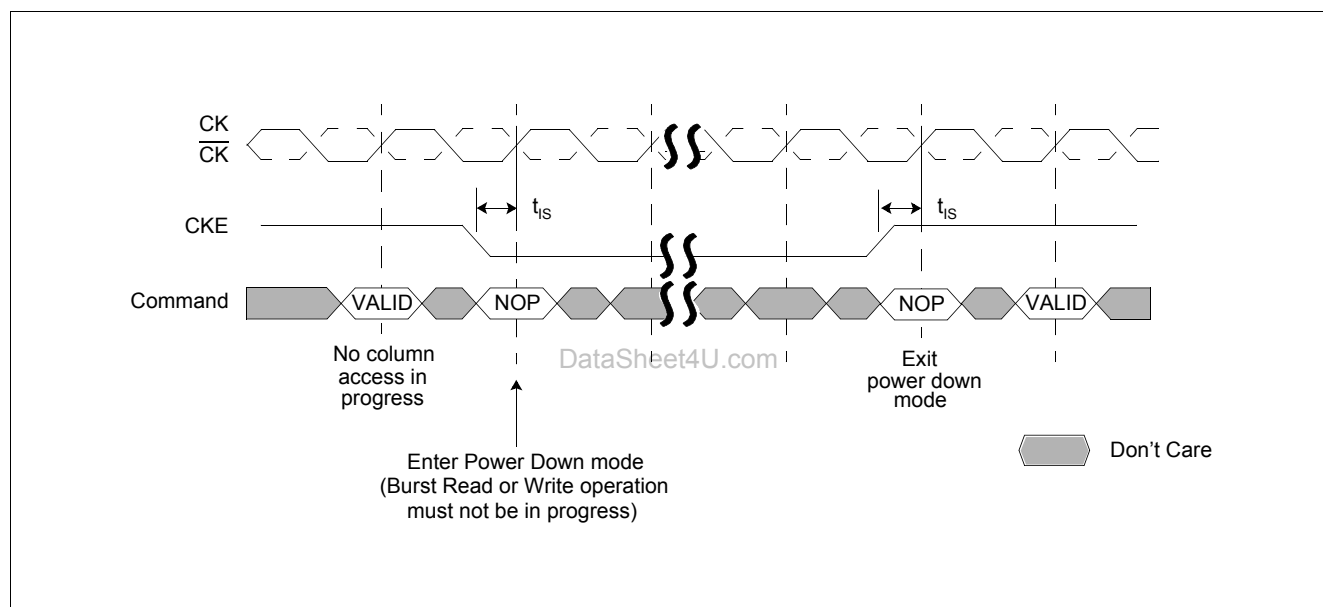
Figure 31   Power Down

Table 7   Truth Table 2: Clock Enable (CKE)

Current State	CKE n-1	CKEn	Command n	Action n	Notes
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	1)
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	2)
Power Down	L	L	X	Maintain Power-Down	–
Power Down	L	H	Deselect or NOP	Exit Power-Down	–
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	–
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	–
Bank(s) Active	H	L	Deselect or NOP	Active Power-Down Entry	–
	H	H	See **Table 8**	–	–

1) V_{REF} must be maintained during Self Refresh operation

2) Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.

1. CKEn is the logic state of CKE at clock edge n: CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMAND n is the command registered at clock edge n, and ACTION n is a result of COMMAND n.
4. All states and sequences not shown are illegal or reserved.

Table 8   Truth Table 3: Current State Bank n - Command to Bank n (same bank)

Current State	CS	RAS	CAS	WE	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation.	1)2)3)4)5)6)
	L	H	H	H	No Operation	NOP. Continue previous operation.	1) to 6)
Idle	L	L	H	H	Active	Select and activate row	1) to 6)
	L	L	L	H	AUTO REFRESH	–	1) to 7)
	L	L	L	L	MODE REGISTER SET	–	1) to 7)
Row Active	L	H	L	H	Read	Select column and start Read burst	1) to 6), 8)
	L	H	L	L	Write	Select column and start Write burst	1) to 6), 8)
	L	L	H	L	Precharge	Deactivate row in bank(s)	1) to 6), 9)
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	1) to 6), 8)
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	1) to 6), 9)
	L	H	H	L	BURST TERMINATE	BURST TERMINATE	1) to 6), 10)
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	1) to 6), 8), 11)
	L	H	L	L	Write	Select column and start Write burst	1) to 6), 8)
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	1) to 6), 9), 11)

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 7** and after t_{XSNR}/t_{XSRD} has been met (if the previous state was self refresh).

2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.

3) Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) The following states must not be interrupted by a command issued to the same bank.
   Precharging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the idle state.
   Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the "row active" state.
   Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   Deselect or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 9**.

5) The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RFC} is met. Once t_{RFC} is met, the DDR SDRAM is in the "all banks idle" state.
   Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR SDRAM is in the "all banks idle" state.
   Precharging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks is in the idle state.

6) All states and sequences not shown are illegal or reserved.

7) Not bank-specific; requires that all banks are idle.

8) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.

9) May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.

10) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.

11) Requires appropriate DM masking.

Table 9 Truth Table 4: Current State Bank n - Command to Bank m (different bank)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	Deselect	NOP. Continue previous operation.	1)2)3)4)5)6)
	L	H	H	H	No Operation	NOP. Continue previous operation.	1) to 6)
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	–	1) to 6)
Row Activating, Active, or Precharging	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 7)
	L	H	L	L	Write	Select column and start Write burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start new Read burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 8)
	L	H	L	L	Write	Select column and start new Write burst	1) to 7)
	L	L	H	L	Precharge	–	1) to 6)
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start new Read burst	1) to 7), 9)
	L	H	L	L	Write	Select column and start Write burst	1) to 7), 9), 10)
	L	L	H	L	Precharge	–	1) to 6)
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	1) to 6)
	L	H	L	H	Read	Select column and start Read burst	1) to 7), 9)
	L	H	L	L	Write	Select column and start new Write burst	1) to 7), 9)
	L	L	H	L	Precharge	–	1) to 6)

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 7**: Clock Enable (CKE) and after t_{XSNR}/t_{XSRD} has been met (if the previous state was self refresh).

2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3) Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Read with Auto Precharge Enabled: See 10).
   Write with Auto Precharge Enabled: See 10).

4) AUTO REFRESH and Mode Register Set commands may only be issued when all banks are idle.

5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.

6) All states and sequences not shown are illegal or reserved.

7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.

8) Requires appropriate DM masking.

9) **Concurrent Auto Precharge:**
This device supports "Concurrent Auto Precharge". When a read with auto precharge or a write with auto precharge is enabled any command may follow to the other banks as long as that command does not interrupt the read or write data transfer and all other limitations apply (e.g. contention between READ data and WRITE data must be avoided). The minimum delay from a read or write command with auto precharge enable, to a command to a different banks is summarized in **Table 10**.

10) A Write command may be applied after the completion of data output.

Table 10   Truth Table 5: Concurrent Auto Precharge

From Command	To Command (different bank)	Minimum Delay with Concurrent Auto Precharge Support	Unit
WRITE w/AP	Read or Read w/AP	$1 + (BL/2) + t_{WTR}$	t_{CK}
	Write to Write w/AP	BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}
Read w/AP	Read or Read w/AP	BL/2	t_{CK}
	Write or Write w/AP	CL (rounded up) + BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}

2.5.6   Input Clock Frequency Change

DDR SDRAM Input clock frequency cannot be changed during normal operation. Clock frequency change is only permitted during Self Refresh or during Power Down. In the latter case the following conditions must be met: DDR SDRAM must be in pre charged mode with CKE at logic Low level. After a minimum of 2 clocks after CKE goes LOW, the clock frequency may change to any frequency between minimum and maximum operating frequeny specified for the particular speed grade. During an input clock frequency change, CKE must be held LOW. Once the input clock frequency is changed, a stable clock must be provided to DRAM before pre charge power down mode may be exited. The DLL must be RESET via EMRS after pre charge power down exit. An additional MRS command may need to be issued to appropriately set CL etc.. After the DLL relock time, the DRAM is ready to operate with the new clock frequency.
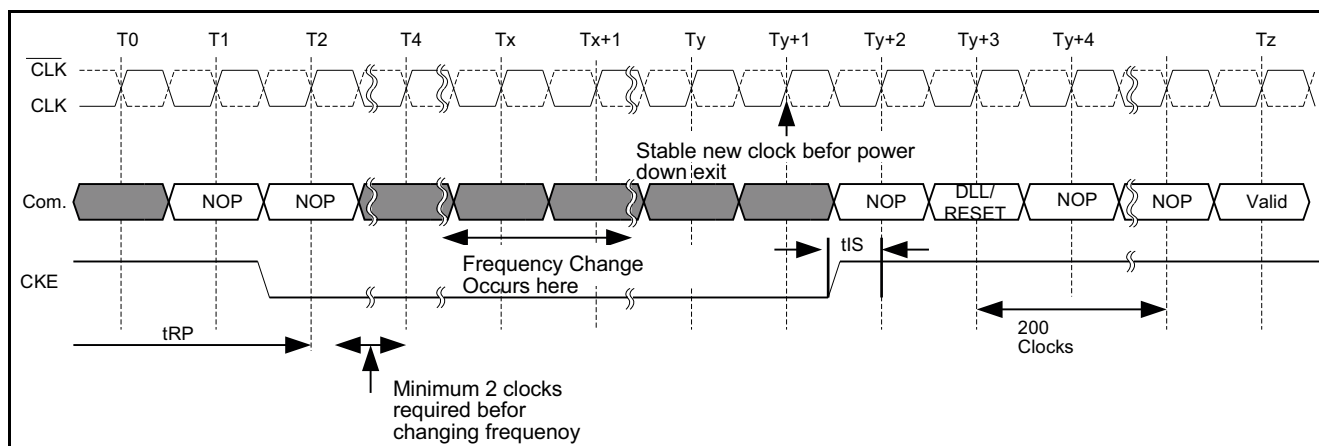
Figure 32   Clock frequency change in pre charge power down mode

2.6 Simplified State Diagram

Figure 33   Simplified State Diagram

PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

3 Electrical Characteristics

3.1 Operating Conditions

Table 11 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Input and Output Capacitances

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input Capacitance: CK, $\overline{CK}$	C_{I1}	2.0	—	3.0	pF	TSOPII [1]
		1.5	—	2.5	pF	TFBGA [1]
Delta Input Capacitance	C_{dI1}	—	—	0.25	pF	[1]
Input Capacitance: All other input-only pins	C_{I2}	1.5	—	2.5	pF	TFBGA [1]
		2.0	—	3.0	pF	TSOPII [1]
Delta Input Capacitance: All other input-only pins	C_{dIO}	—	—	0.5	pF	[1]
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	3.5	—	4.5	pF	TFBGA [1][2]
		4.0	—	5.0	pF	TSOPII [1][2]
Delta Input/Output Capacitance: DQ, DQS, DM	C_{dIO}	—	—	0.5	pF	[1]

1) These values are not subject to production test - verified by design/characterization and are tested on a sample base only. V_{DDQ} = V_{DD} = 2.5 V ± 0.2 V, f = 100 MHz, T_A = 25 °C, $V_{OUT(DC)}$ = V_{DDQ}/2, V_{OUT} (Peak to Peak) 0.2 V. Unused pins are tied to ground.

2) DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

3.2 Normal Strength Pull-down and Pull-up Characteristics

Table 12   Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz [2][3]
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	[4]
I/O Termination Voltage (System)	V_{TT}	$V_{REF} - 0.04$		$V_{REF} + 0.04$	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$		$V_{DDQ} + 0.3$	V	[6]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.15$	V	[6]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	-0.3		$V_{DDQ} + 0.3$	V	[6]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		$V_{DDQ} + 0.6$	V	[6][7]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[8]
Input Leakage Current	I_I	-2		2	µA	Any input 0 V $\leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [6][9]
Output Leakage Current	I_{OZ}	-5		5	µA	DQs are disabled; 0 V $\leq V_{OUT} \leq V_{DDQ}$ [6]
Output High Current, Normal Strength Driver	I_{OH}	—		-16.2	mA	V_{OUT} = 1.95 V [6]
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V [6]

1) $0\ °C \leq T_A \leq 70\ °C$

2) DDR400 conditions apply for all clock frequencies above 166 MHz

3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

4) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

6) Inputs are not recognized as valid until V_{REF} stabilizes.

7) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

8) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

9) Values are shown per component

1. The nominal pull-down V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
2. The full variation in driver pull-down current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.
3. The nominal pull-up V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
4. The full variation in driver pull-up current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.
5. The full variation in the ratio of the maximum to minimum pull-up and pull-down current does not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
6. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10%, for device drain to source voltages from 0.1 to 1.0 V.
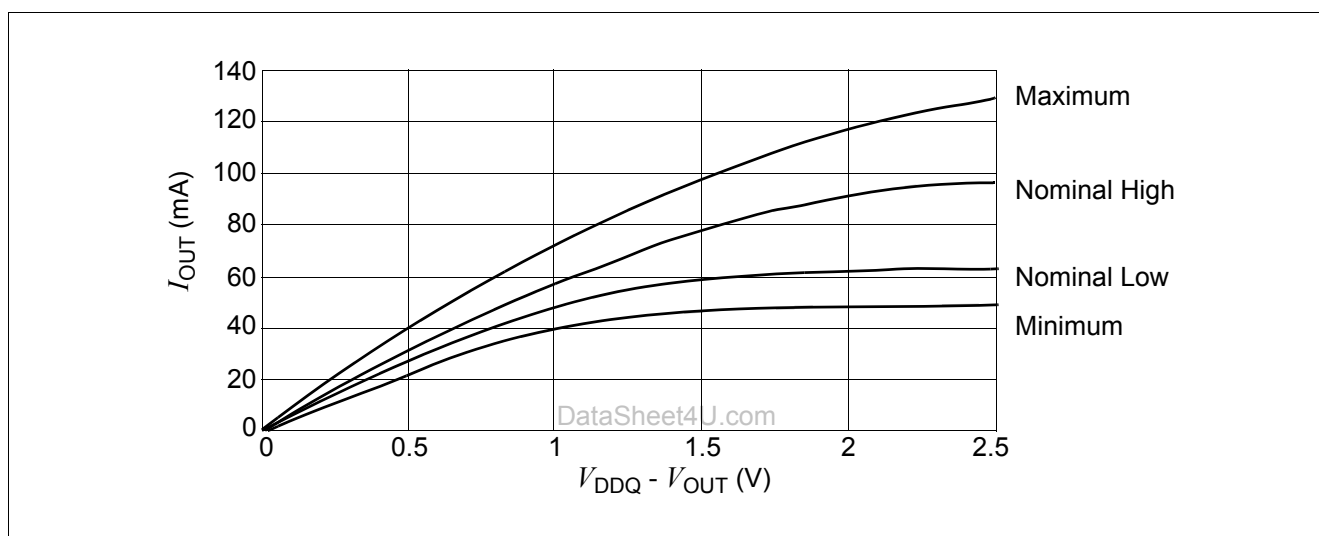
Figure 34   Normal Strength Pull-down Characteristics
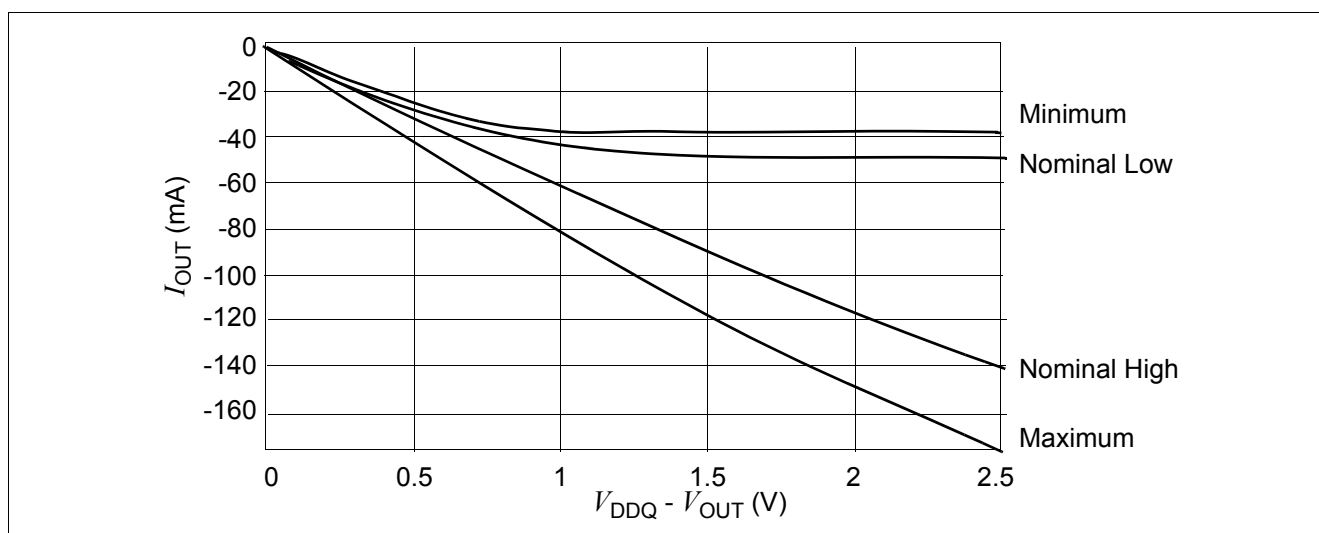
Figure 35   Normal Strength Pull-up Characteristics

Table 13 Normal Strength Pull-down and Pull-up Currents

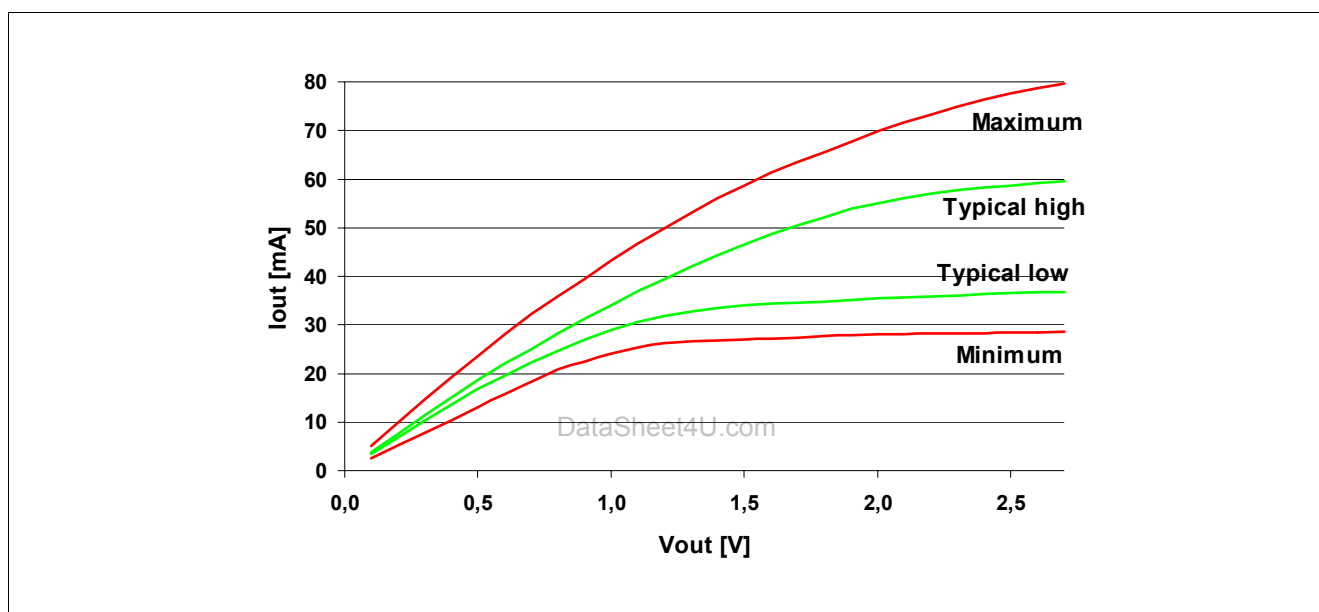| Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Nominal Low	Nominal High	min.	max.	Nominal Low	Nominal High	min.	max.
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.9	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

Table 14 Pull-down and Pull-up Process Variations and Conditions

Parameter	Nominal	Minimum	Maximum
Operating Temperature	25 °C	0 °C	70 °C
V_{DD}/V_{DDQ}	2.5 V	2.3 V	2.7 V

3.3 Weak Strength Pull-down and Pull-up Characteristics

1. The weak pull-down V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
2. The weak pull-up V-I curve for DDR SDRAM devices is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve.
3. The full variation in driver pull-up current from minimum to maximum process, temperature, and voltage lie within the outer bounding lines of the V-I curve.
4. The full variation in the ratio of the maximum to minimum pull-up and pull-down current does not exceed 1.7, for device drain to source voltages from 0.1 to 1.0.
5. The full variation in the ratio of the nominal pull-up to pull-down current should be unity $\pm10\%$, for device drain to source voltages from 0.1 to 1.0 V.

Figure 36   Weak Strength Pull-down Characteristics
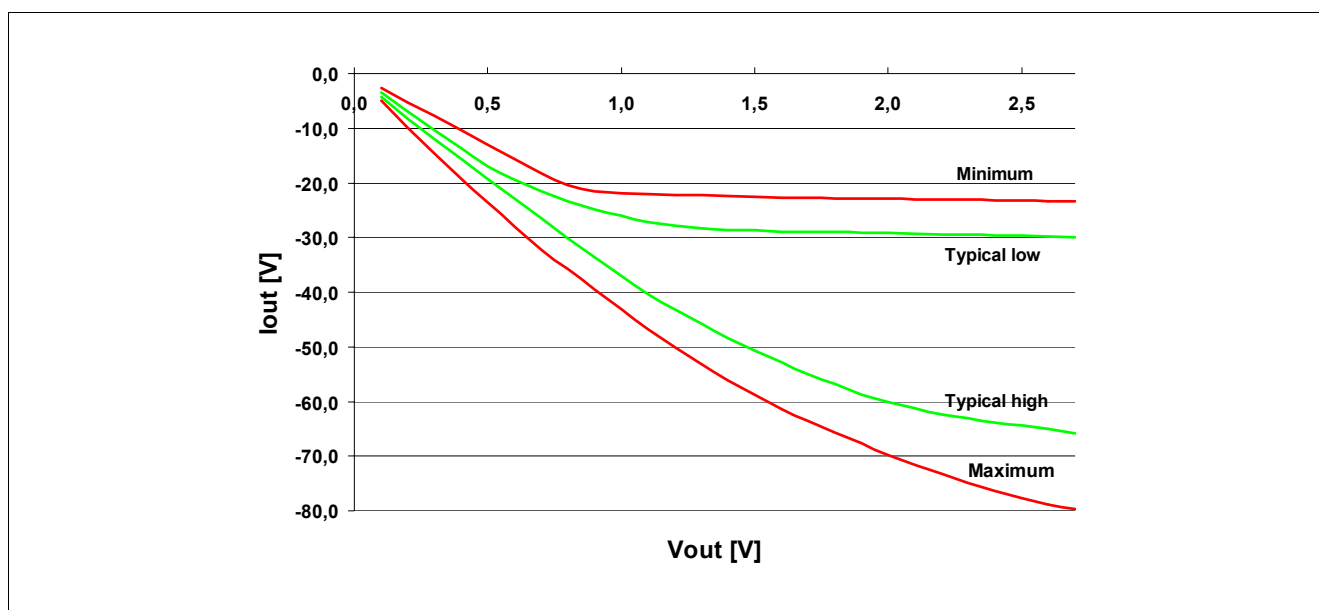
Figure 37   Weak Strength Pull-up Characteristics

Table 15   Weak Strength Driver Pull-down and Pull-up Characteristics

| Voltage (V)	Pulldown Current (mA)				Pullup Current (mA)			
	Nominal Low	Nominal High	min.	max.	Nominal Low	Nominal High	min.	max.
0.1	3.4	3.8	2.6	5.0	-3.5	-4.3	-2.6	-5.0
0.2	6.9	7.6	5.2	9.9	-6.9	-8.2	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12.0	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13.0	23.6	-16.9	-19.3	-13.0	-23.6
0.6	19.6	22.1	15.7	28.0	-19.4	-22.9	-15.7	-28.0
0.7	22.3	25.0	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1.0	29.0	34.1	24.1	43.2	-26.0	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50.0	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42.0	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34.0	46.6	27.0	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55.0	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29.0	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2.0	35.4	55.0	28.0	69.8	-29.2	-60.0	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23.0	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23.0	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

3.4   AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.)

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. **Figure 38** represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5 V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level).
6. For System Characteristics like Setup & Holdtime Derating for Slew Rate, I/O Delta Rise/Fall Derating, DDR SDRAM Slew Rate Standards, Overshoot & Undershoot specification and Clamp V-I characteristics see the latest JEDEC specification for DDR components.
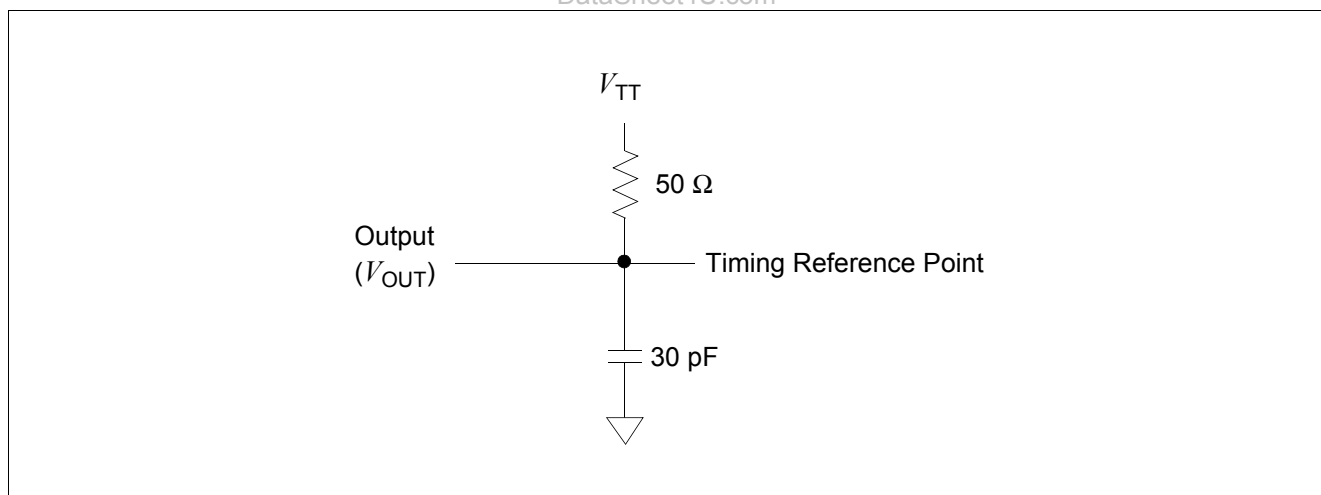
Figure 38   AC Output Load Circuit Diagram / Timing Reference Load

Table 16   AC Operating Conditions[1]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Input High (Logic 1) Voltage, DQ, DQS and DM Signals	$V_{IH(AC)}$	$V_{REF} + 0.31$	—	V	2)3)
Input Low (Logic 0) Voltage, DQ, DQS and DM Signals	$V_{IL(AC)}$	—	$V_{REF} - 0.31$	V	2)3)
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(AC)}$	0.7	$V_{DDQ} + 0.6$	V	2)3)4)
Input Closing Point Voltage, CK and $\overline{CK}$ Inputs	$V_{IX(AC)}$	$0.5 \times V_{DDQ} - 0.2$	$0.5 \times V_{DDQ} + 0.2$	V	2)3)5)

1) V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR200 - DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400); 0 °C ≤ T_A ≤ 70 °C

2) Input slew rate = 1 V/ns.

3) Inputs are not recognized as valid until V_{REF} stabilizes.

4) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

5) The value of V_{IX} is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

Table 17   AC Timing - Absolute Specifications for DDR400B and DDR333

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.5	+0.5	–0.7	+0.7	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock cycle time	t_{CK}	5	8	6	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$				t_{CK}	2)3)4)5)6)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	ns	TFBGA 2)3)4)5)
		—	+0.40	—	+0.45	ns	TSOPII 2)3)4)5)
Write command to 1st DQS latching transition	t_{DQSS}	0.72	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)

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Table 17   AC Timing - Absolute Specifications for DDR400B and DDR333

Parameter	Symbol	–5 DDR400B		–6 DDR333		Unit	Note/ Test Condition [1]
		Min.	Max.	Min.	Max.		
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})	—	min. (t_{CL}, t_{CH})	—	ns	2)3)4)5)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate3)4)5)6)8)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)9)
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)8)
		0.7	—	0.8	—	ns	slow slew rate3)4)5)6)8)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.70	–0.70	+0.70	ns	2)3)4)5)7)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	ns	TFBGA 2)3)4)5)
		—	+0.50	—	+0.55	ns	TSOPII 2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	t_{RCD}	—	t_{RCD}	—	ns	2)3)4)5)
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)8)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	65	—	72	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	18	—	ns	2)3)4)5)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)

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Table 17   AC Timing - Absolute Specifications for DDR400B and DDR333

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	2)3)4)5)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)10)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)11)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)

1) $0\ °C \leq T_A \leq 70\ °C$; V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V

2) Input slew rate $\geq$ 1 V/ns

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are $\geq$ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) Fast slew rate $\geq$ 1.0 V/ns , slow slew rate $\geq$ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.

9) These parameters guarantee device timing, but they are not necessarily tested on each device.

10) The specific requirement is that DQS be valid (HIGH,LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specificationsof the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW at this time, depending on t_{DQSS}.

11) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

I_{DD} Specification and Conditions

Parameter	Symbol
Operating Current: one bank; active/ precharge; t_{RC} = t_{RCMIN}; t_{CK} = t_{CKMIN}; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	I_{DD1}
Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE $\leq V_{ILMAX}$; t_{CK} = t_{CKMIN}	I_{DD2P}

I_{DD} Specification and Conditions (cont'd)

Parameter	Symbol
Precharge Floating Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE $\geq V_{IHMIN}$; $t_{CK} = t_{CKMIN}$, address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE $\geq V_{IHMIN}$; $t_{CK} = t_{CKMIN}$, address and other control inputs stable at $\geq V_{IHMIN}$ or $\leq V_{ILMAX}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD2Q}
Active Power-Down Standby Current: one bank active; power-down mode; CKE $\leq V_{ILMAX}$; $t_{CK} = t_{CKMIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD3P}
Active Standby Current: one bank active; $\overline{CS} \geq V_{IHMIN}$; CKE $\geq V_{IHMIN}$; $t_{RC} = t_{RASMAX}$; $t_{CK} = t_{CKMIN}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$; $I_{OUT} = 0$ mA	I_{DD4R}
Operating Current: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$	I_{DD4W}
Auto-Refresh Current: $t_{RC} = t_{RFCMIN}$, burst refresh	I_{DD5}
Self-Refresh Current: CKE ≤ 0.2 V; external clock on; $t_{CK} = t_{CKMIN}$	I_{DD6}
Operating Current: four bank; four bank interleaving with BL = 4; Refer to the following page for detailed test conditions.	I_{DD7}

Table 18 I_{DD} Specification for HYB25DC512[800/160C[E/F]

Symbol	−6 DDR333 Typ.	Max.	−5 DDR400B Typ.	Max.	Unit	Note[1]
I_{DD0}	60	70	60	75	mA	×4/×8 [2)3)]
	70	85	75	90	mA	×16 [3)]
I_{DD1}	65	80	70	85	mA	×4/×8 [3)]
	80	95	90	110	mA	×16 [3)]
I_{DD2P}	1.1	4.6	1.1	4.6	mA	[3)]
I_{DD2F}	21	25	25	30	mA	[3)]
I_{DD2Q}	15	22	17	23	mA	[3)]
I_{DD3P}	11	15	12	16	mA	[3)]
I_{DD3N}	32	37	35	42	mA	×4/×8[3)]
	33	40	38	45	mA	×16 [3)]
I_{DD4R}	70	85	80	90	mA	×4/×8 [3)]
	95	115	110	135	mA	×16 [3)]
I_{DD4W}	75	90	85	95	mA	×4/×8 [3)]
	100	120	115	135	mA	×16 [3)]
I_{DD5}	130	175	145	190	mA	[3)]
I_{DD6}	1.6	5	1.6	5	mA	[4)]
	–	2.5	–	2.5	mA	low power(L)

Table 18 I_{DD} Specification for HYB25DC512[800/160C[E/F]

Symbol	−6 DDR333		−5 DDR400B		Unit	Note[1]
	Typ.	Max.	Typ.	Max.		
I_{DD7}	175	205	195	230	mA	×4/×8[3]
	190	230	210	250	mA	×16 [3]

1) Test conditions for typical values: V_{DD} = 2.6 V, T_A = 25 °C, test conditions for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

2) I_{DD} specifications are tested after the device is properly initialized and measured at 200 MHz.

3) Input slew rate = 1 V/ns.

4) Enables on-chip refresh and address counters.

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3.4.1 I_{DD} Current Measurement Conditions

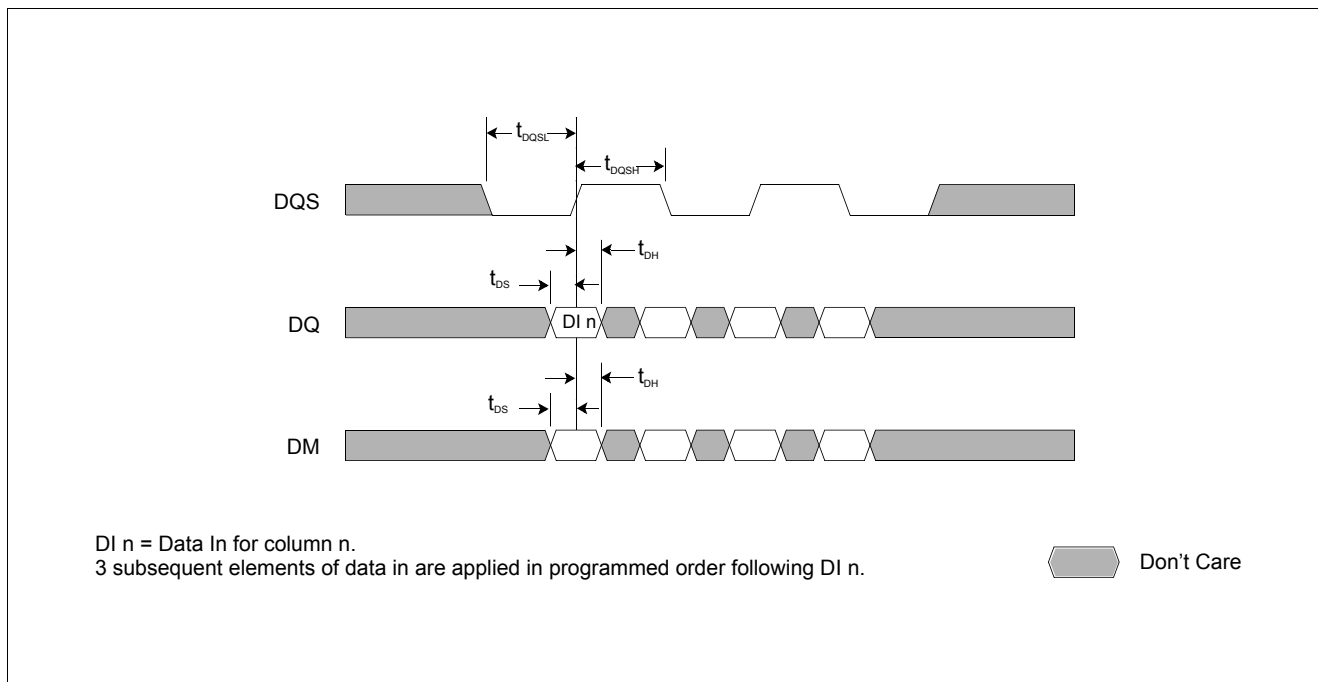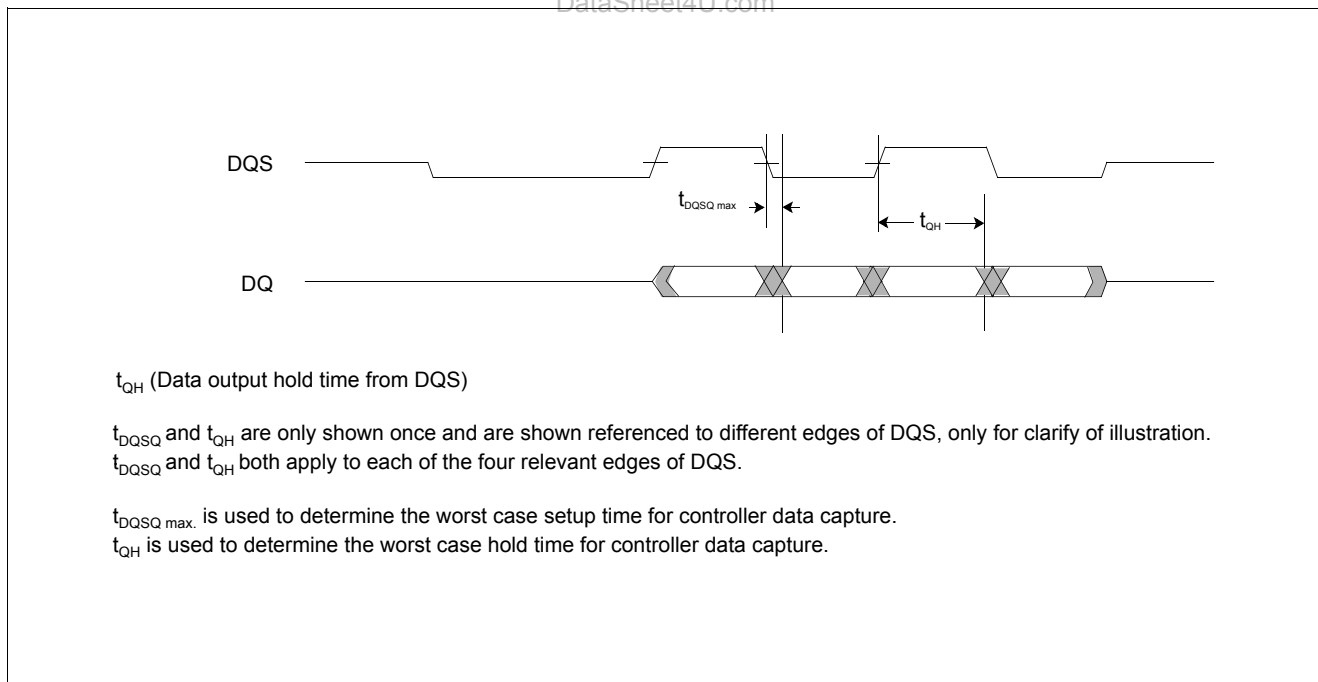Legend: A = Activate, R = Read, RA = Read with Autoprecharge, P = Precharge, N = NOP or DESELECT

I_{DD1}: Operating Current: One Bank Operation

1. General test condition
   a) Only one bank is accessed with $t_{RC,MIN}$.
   b) Burst Mode, Address and Control inputs are changing once per NOP and DESELECT cycle.
   c) 50% of data changing at every transfer
   d) I_{OUT} = 0 mA.
2. Timing patterns
   a) **DDR333** (166 MHz, CL = 2.5): t_{CK} = 6 ns, BL = 4, t_{RCD} = 3 × t_{CK}, t_{RC} = 10 × t_{CK}, t_{RAS} = 7 × t_{CK}
      Setup: A0 N N R0 N N N P0 N N
      Read: A0 N N R0 N N N P0 N N - repeat the same timing with random address changing
   b) **DDR400B** (200 MHz, CL = 3): t_{CK} = 5 ns, BL = 4, t_{RCD} = 3 × t_{CK}, t_{RC} = 11 × t_{CK}, t_{RAS} = 8 × t_{CK}
      Setup:A0 N N R0 N N N P0 N N
      Read: A0 N N R0 N N N P0 N N -repeat the same timing with random address changing

I_{DD7}: Operating Current: Four Bank Operation

1. General test condition
   a) Four banks are being interleaved with t_{RCMIN}.
   b) Burst Mode, Address and Control inputs on NOP edge are not changing.
   c) 50% of data changing at every transfer
   d) I_{OUT} = 0 mA.
2. Timing patterns
   a) **DDR333** (166 MHz, CL = 2.5): t_{CK} = 6 ns, BL = 4, t_{RRD} = 2 × t_{CK}, t_{RCD} = 3 × t_{CK}, t_{RAS} = 5 × t_{CK}
      Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3
      Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 - repeat the same timing with random address changing
   b) **DDR400B** (200 MHz, CL = 3): t_{CK} = 5 ns, BL = 4, t_{RRD} = 2 × t_{CK}, t_{RCD} = 3 *× t_{CK}, t_{RAS} = 8 × t_{CK}
      Setup: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N
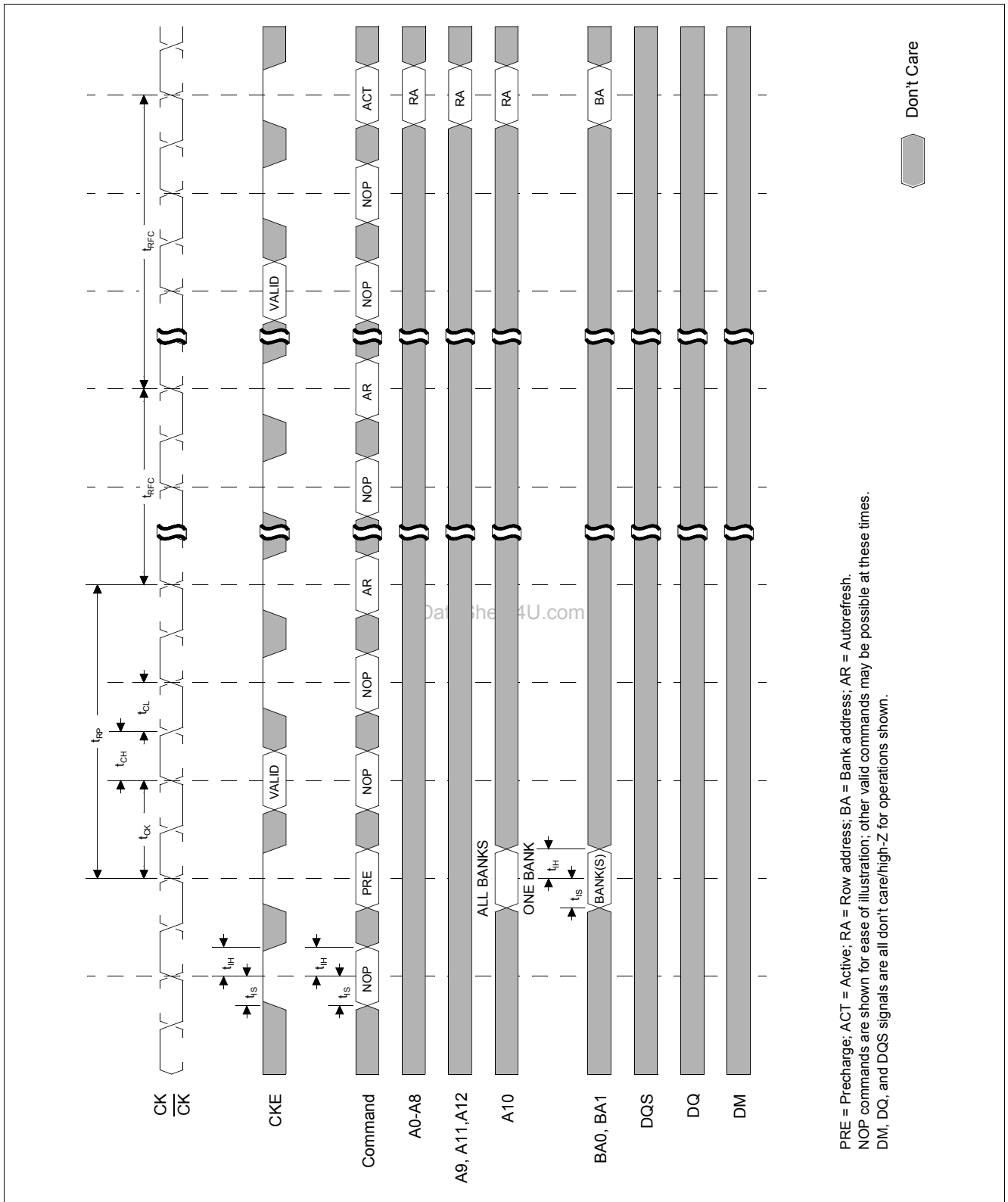   Read: A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N - repeat the same timing with random address

4 Timing Diagrams

Figure 39 Data Input (Write), Timing Burst Length = 4

t_{QH} (Data output hold time from DQS)

t_{DQSQ} and t_{QH} are only shown once and are shown referenced to different edges of DQS, only for clarify of illustration.
t_{DQSQ} and t_{QH} both apply to each of the four relevant edges of DQS.

$t_{DQSQ\ max.}$ is used to determine the worst case setup time for controller data capture.
t_{QH} is used to determine the worst case hold time for controller data capture.

Figure 40 Data Output (Read), Timing Burst Length = 4

Figure 41   Initialize and Mode Register Sets

Figure 42   Power Down Mode
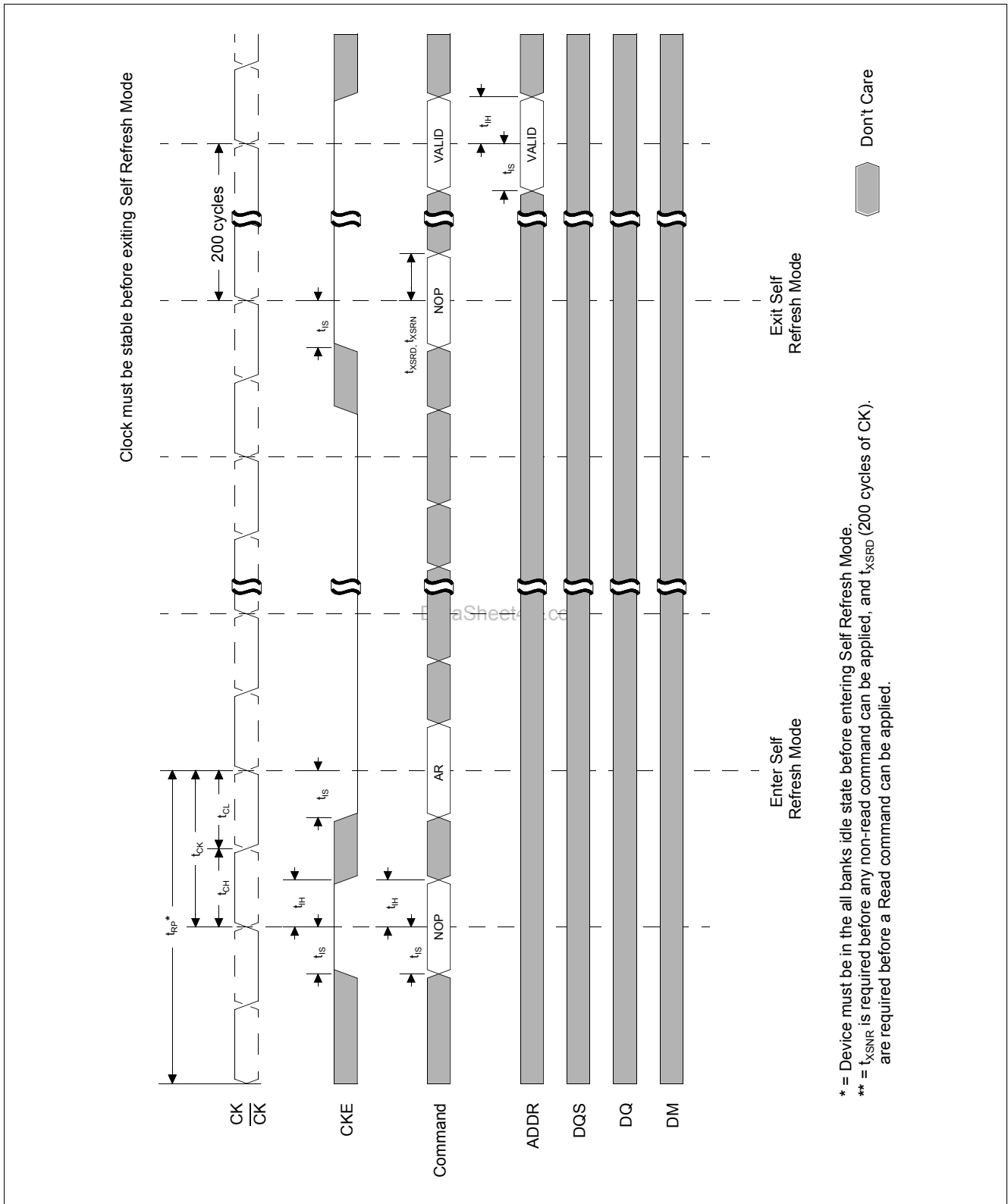
Figure 43   Auto Refresh Mode

PRE = Precharge; ACT = Active; RA = Row address; BA = Bank address; AR = Autorefresh.
NOP commands are shown for ease of illustration; other valid commands may be possible at these times.
DM, DQ, and DQS signals are all don't care/high-Z for operations shown.
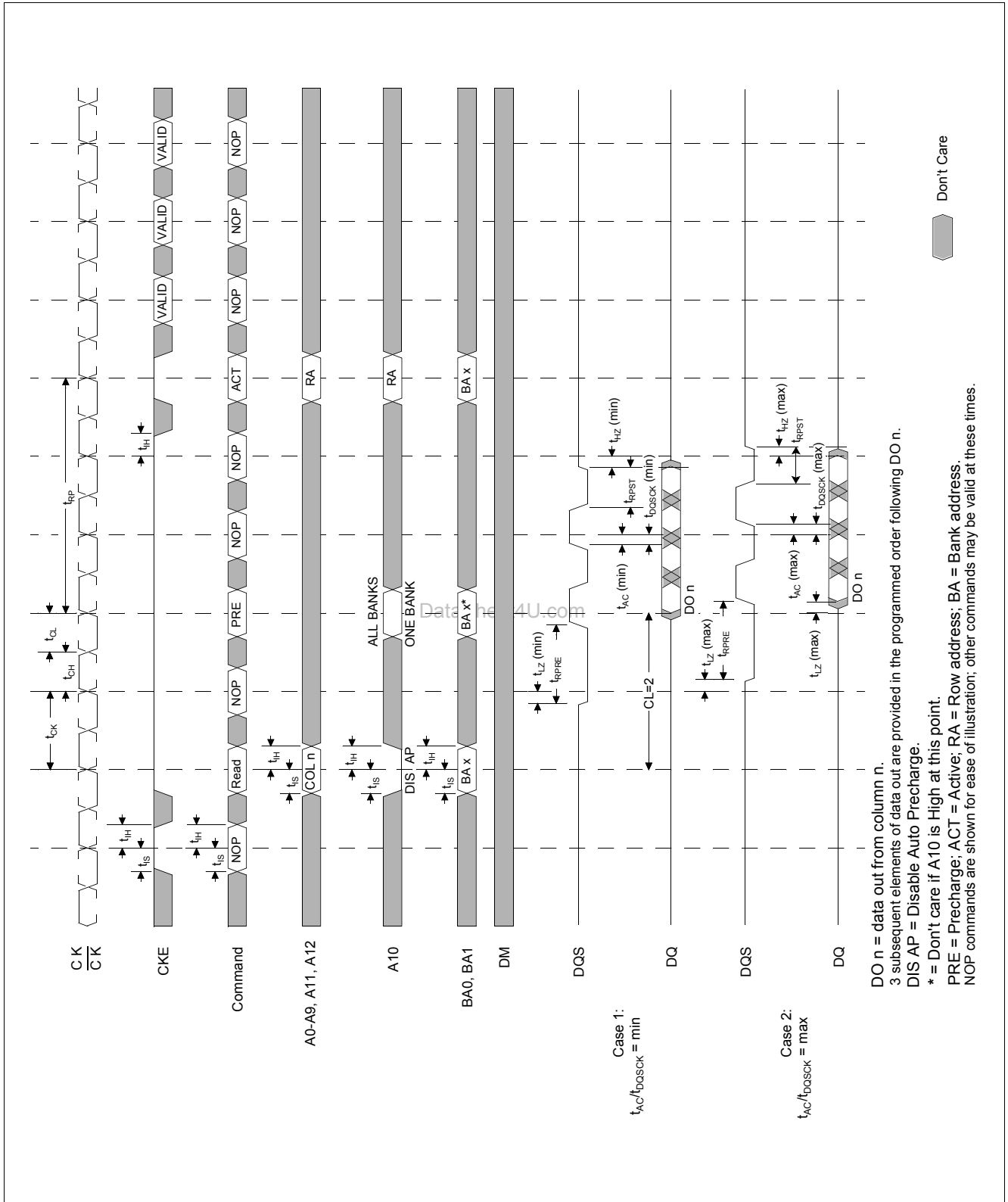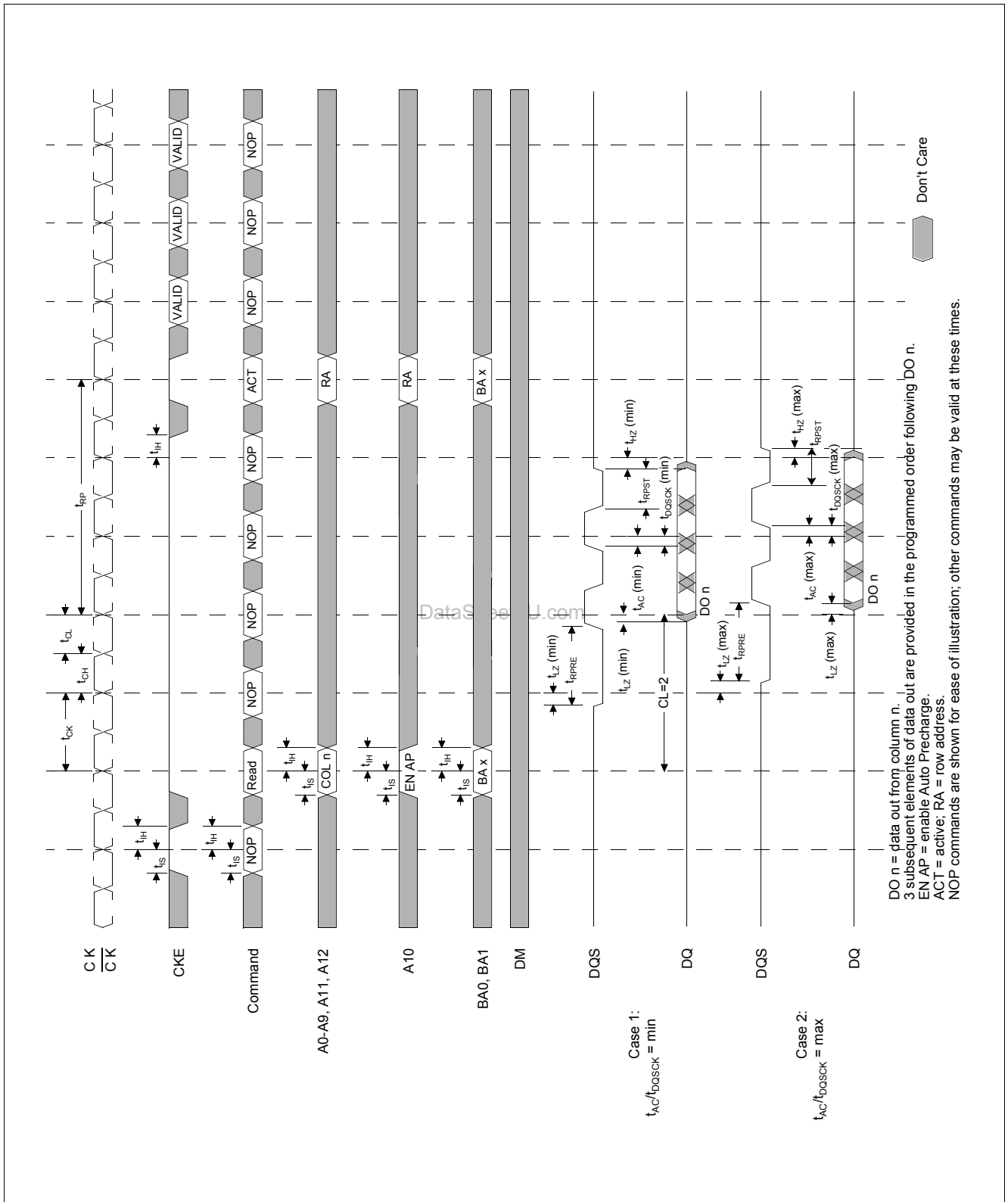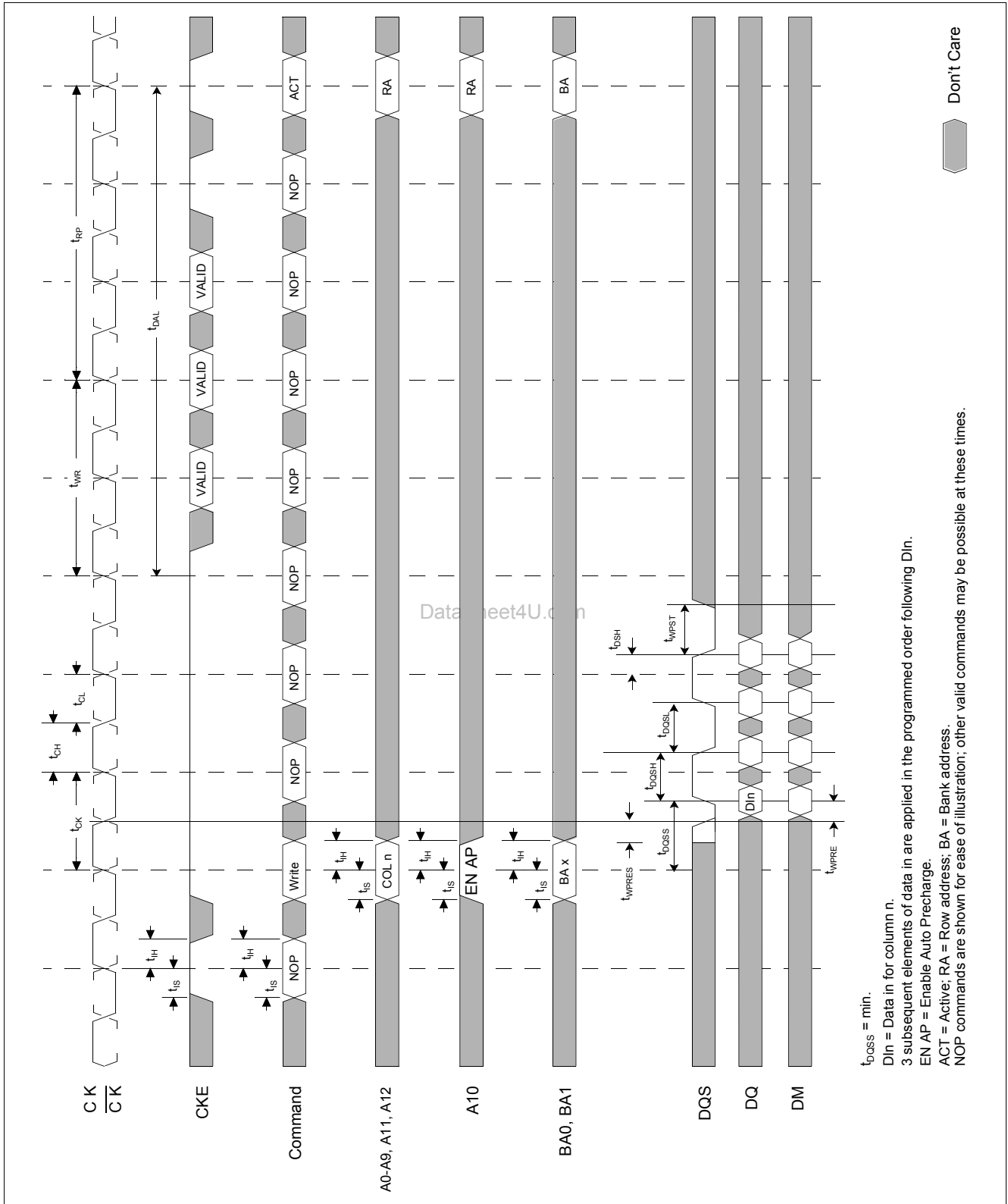
Don't Care

Figure 44   Self Refresh Mode

Figure 45   Read without Auto Precharge (Burst Length = 4)

Figure 46   Read with Auto Precharge (Burst Length = 4)

Figure 47   Bank Read Access (Burst Length = 4)

Figure 48   Write without Auto Precharge (Burst Length = 4)

Figure 49   Write with Auto Precharge (Burst Length = 4)

Figure 50   Bank Write Access (Burst Length = 4)

Figure 51   Write DM Operation (Burst Length = 4)

5 System Characteristics for DDR SDRAMs

The following specification parameters are required in systems using DDR400 devices to ensure proper system performance. These characteristics are for system simulation purposes and are not subject to production test - verified by design/characterization.

Table 19   Input Slew Rate for DQ, DQS, and DM

AC Characteristics	Symbol	DDR400		Units	Notes
Parameter		Min.	Max.		
DM/DQS inout slew rate measured berween $V_{IH(DC)}$, $V_{IL(DC)}$, and $V_{IL(DC)}$, $V_{IH(DC)}$	DCSLEW	0.5	4.0	V/ns	1)2)

1) Pullup slew rate is characterized under the test conditions as shown in **Figure 52**.

2) DQS, DM, amd DQ input slew rate is specified to prevent doble clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

Table 20   Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	Δt_{IS}	t_{IH}	Units	Notes
0.5 V/ns	0	0	ps	1)
0.4 V/ns	+50	0	ps	
0.3 V/ns	+100	0	ps	

1) A derating factor will be used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns as shown in **Table 20**. The input slew rate is based on the lesser of the slew rates determined by either $V_{IH\,(AC)}$ to $V_{IL\,(AC)}$ or $V_{IH\,(DC)}$ to $V_{IL\,(DC)}$, similarly for rising transitions.

Table 21   Input/Output Setup and Hold TIme Derating for Slew Rate

I/O Input Slew Rate	Δt_{DS}	t_{DH}	Units	Notes
0.5 ns/V	0	0	ps	1)
0.4 ns/V	+75	+75	ps	
0.3 ns/V	+100	+100	ps	

1) **Table 21** is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AV – AC slew rate and the DC – DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either $V_{IH\,(AC)}$ to $V_{IL\,(AC)}$ or $V_{IH\,(DC)}$ to $V_{IL\,(DC)}$, and similarly for rising transitions.

Table 22   Input/Output Setup and Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	Δt_{DS}	t_{DH}	Units	Notes
± 0.0 ns/V	0	0	ps	1)
± 0.25 ns/V	+50	+50	ps	
± 0.5 ns/V	+100	+100	ps	

1) A derating factor will be used to increase t_{DS} and t_{DH} in the case where DQ, DM and DQS slew rates differ, as shown in Tables 15 & 16. Input slew rate is based on the larger of AC – AC delta rise, fall rate and DC – DC delta rise, fall rate. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH\,(AC)}$ to $V_{IL\,(AC)}$ or $V_{IH\,(DC)}$ to $V_{IL\,(DC)}$, similarly for rising transitions.
The delta rise/fall rate is calculated as:{1/(Slew Rate1)} – {1/(Slew Rate2)}
For example: If Slew Rate 1 is 0.5 V/ns and Slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is –0.5 ns/V. Using the table given, this would result in the need for an increase in t_{DS} and t_{DH} of 100 ps. A

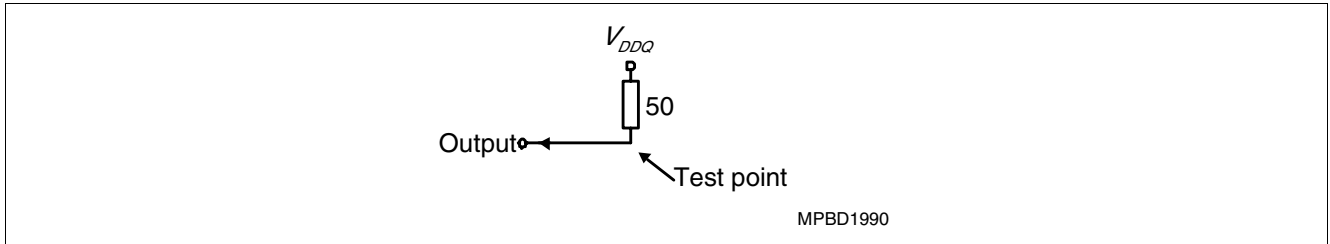**Table 23   Output Slew Rate Characteristrics (×8 Devices only)**

Slew Rate Characteristic	Typical Range (V/ns)	Minumum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 – 2.5	1.0	4.5	1)2)3)4)5)6)
Pulldown Slew Rate	1.2 – 2.5	1.0	4.5	2)3)4)5)5)7)2)2)

1) Pullup slew rate is characterized under the test conditions as shown in **Figure 52**

2) Pullup slew rate is measured between (V_{DDQ}/2 – 320 mV ± 250 mV)
   Pulldown slew rate is measured between (V_{DDQ}/2 + 320 mV ± 250 mV)
   Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.
   Example: For typical slew rate, DQ0 is switching
   For minimum slew rate, all DQ bits are switchiung worst case pattern
   For maximum slew rate, only one DQ is switching from either high to low, or low to high.
   the remainig DQ bits remain the same as previous state.

3) Evaluation conditions
   Typical: 25 °C (T Ambient), V_{DDQ} = nominal, typical process
   Minimum: 70 °C (T Ambient), V_{DDQ} = minimum, slow – slow process
   Maximum: 0 °C (T Ambient), V_{DDQ} = maximum, fast – fast process

4) Verified under typical conditions for qualification purposes.

5) TSOP II package devices only.

6) Only intended for operation up to 266 Mbps per pin.

7) Pulldown slew rate is measured under the test conditions shown in **Figure 53**.

Table 24   Output Slew Rate Characteristics (×16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum(V/ns)	Notes
Pullup Slew Rate	1.2 – 2.5	0.7	5.0	1)2)3)4)5)6)
Pulldown Slew Rate	1.2 – 2.5	0.7	5.0	7)

1) Pullup slew rate is characterizted under the test conditions as shown in **Figure 52**

2) Pullup slew rate is measured between (V_{DDQ}/2 – 320 mV ± 250 mV)
   Pulldown slew rate is measured between (V_{DDQ}/2 + 320 mV ± 250mV)
   Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.
   Example: For typical slew rate, DQ0 is switching
   For minimum slew rate, all DQ bits are switchiung worst case pattern
   For maximum slew rate, only one DQ is switching from either high to low, or low to high.
   the remainig DQ bits remain the same as previous state.

3) Evaluation conditions
   Typical: 25 °C (T Ambient), V_{DDQ} = nominal, typical process
   Minimum: 70 °C (T Ambient), V_{DDQ} = minimum, slow – slow process
   Maximum: 0 °C (T Ambient), V_{DDQ} = maximum, fast – fast process

4) Verified under typical conditions for qualification purposes.

5) TSOP II package devices only.

6) Only intended for operation up to 266 Mbps per pin.

7) Pulldown slew rate is measured under the test conditions shown in **Figure 53**.

Figure 52   Pullup slew rate test load
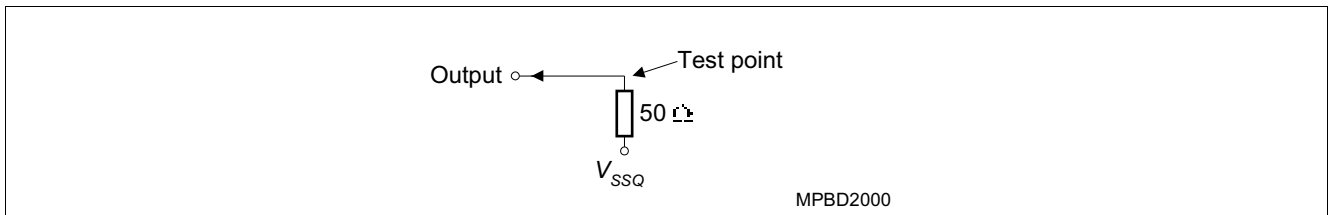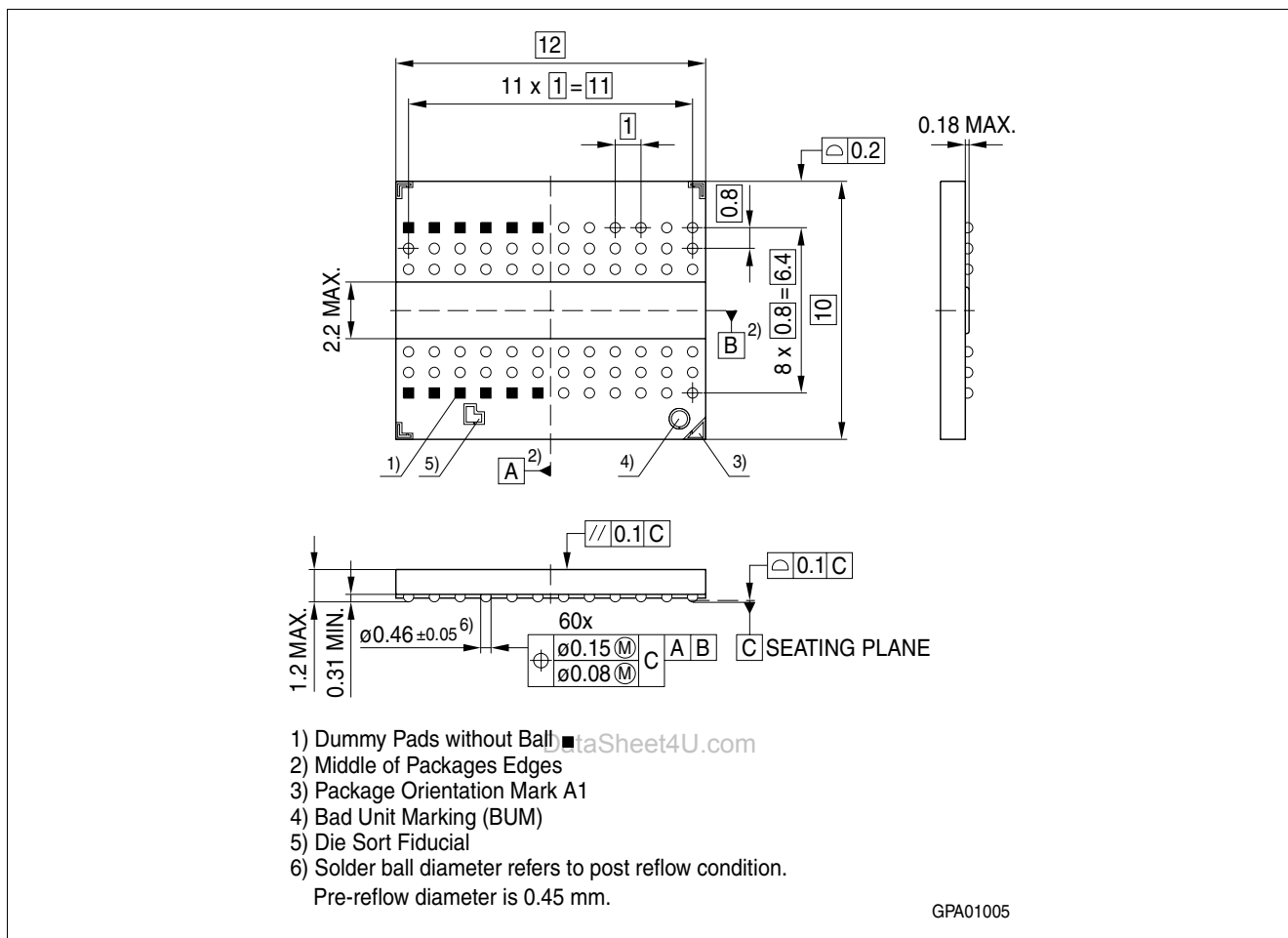

Figure 53   Pulldown slew rate test load

6 Package Outlines

There are two package types used for this product family each in lead-free and lead-containing assembly:

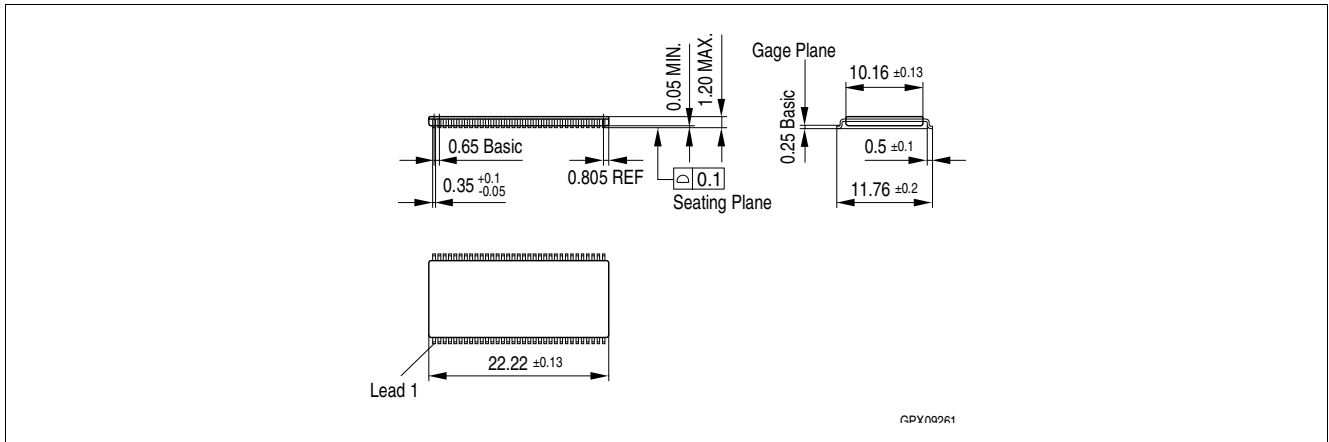• P-TFBGA: Plastic Thin Fine-Pitch Ball Grid Array Package

Table 25   TFBGA Common Package Properties (non-green/green)

Description	Size	Units
Ball Size	0.460	mm
Recommended Landing Pad	0.350	mm
Recommended Solder Mask	0.450	mm

-

1) Dummy Pads without Ball
2) Middle of Packages Edges
3) Package Orientation Mark A1
4) Bad Unit Marking (BUM)
5) Die Sort Fiducial
6) Solder ball diameter refers to post reflow condition.
   Pre-reflow diameter is 0.45 mm.

GPA01005

Figure 54   Package Outline P-TFBGA-60-11

• P-TSOPII: Plastic Thin Small Outline Package Type II

Figure 55   Package Outline of PG-TSOPII-66-1 (green/non-green)

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