1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12-bit digital-to-analog converter. The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Each D/A converter has a 2-byte (8 + 4) loading structure. It is designed for right-justified format. The device is easily interfaced to any 8-bit microprocessor system.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
–1	AD7537S(X)/883B
–2	AD7537T(X)/883B
–3	AD7537U(X)/883B

NOTE
[1]To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip, 0.3″ Width
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted, Pin numbers refer to DIP package)

V_{DD} (Pin 20) to DGND	−0.3V, +17V
V_{REFA}, V_{REFB} (Pins 4, 21) to AGNDA, AGNDB	±25V
V_{RFBA}, V_{RFBB} (Pins 3, 22) to AGNDA, AGNDB	±25V
Digital Input Voltage (Pins 5–19) to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN23} to DGND	−0.3V, V_{DD} +0.3V
AGNDA, AGNDB to DGND	−0.3V, V_{DD} +0.3V
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24 and E-28A
θ_{JA} = 120°C/W for Q-24 and E-28A

AD7537—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]/Comments	Units
Resolution	RES	– 1, 2, 3	12					Bits
Relative Accuracy	RA	– 1	1	1	1		V_{DD} = 10.8V	± LSB max
		– 2, 3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	– 1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 12 Bits from T_{min} to T_{max}. V_{DD} = 10.8V	± LSB max
Gain Error	A_E	– 1	6	6	6		Measured Using R_{FA} and R_{FB}. Both DAC Registers Loaded with All 1s. V_{DD} = 10.8V.	± LSB max
		– 2	3	6	3	3		
		– 3	2	6	2	2		
Gain Temperature Coefficient	dA_E/dT	– 1, 2, 3	5				Typical Value is 1ppm/°C	± ppm/°C max
Output Leakage Current (Pin 2)	I_{OUTA}	– 1, 2, 3	250	10	250		DAC A Register Loaded with All 0s; V_{DD} = 16.5V	nA max
Output Leakage Current (Pin 23)	I_{OUTB}	– 1, 2, 3	250	10	250		DAC B Register Loaded with All 0s; V_{DD} = 16.5V	nA max
Reference Input Resistance (Pin 4, Pin 21)	R_I	– 1, 2, 3	9	9	9		Typical Input Resistance is 14k V_{DD} = 10.8V	kΩ min
			20	20	20			kΩ max
Reference Input Resistance Match V_{REFA}, V_{REFB}	RM_{IN}	– 1, 2	3	3	3		Typically ± 0.5% V_{DD} = 10.8V	± % max
		– 3	1	3	3	1		
Digital Input High Voltage	V_{IH}	– 1, 2, 3	2.4	2.4	2.4		V_{DD} = 10.8V and 16.5V	V min
Digital Input Low Voltage	V_{IL}	– 1, 2, 3	0.8	0.8	0.8		V_{DD} = 10.8V and 16.5V	V max
Digital Input Current	I_{IN}	– 1, 2, 3	10	1	10		V_{IN} = V_{DD} = 16.5V	μA max
Digital Input Capacitance	C_I	– 1, 2, 3	10					pF max
Power Supply Voltage	V_{DD}	– 1, 2, 3	10.8					V min
			16.5					V max
Power Supply Current	I_{DD}	– 1, 2, 3	2	2	2		V_{DD} = 16.5V	mA max
Output Current Settling Time @ 25°C	t_{SL}	– 1, 2, 3	1.5				To 0.01% of Full-Scale Range. I_{OUT} Load = 100. C_{EXT} = 13pF. DAC Output Measured from Rising Edge of WR. Typical Value of Settling Time is 0.8μs.	μs max
AC Feedthrough V_{REFA} to I_{OUTA} and V_{REFB} to I_{OUTB}	FT	– 1, 2, 3	65				V_{REFA}, V_{REFB} = 20V p-p 10kHz Sine-Wave DAC Register Loaded with All 0s.	– dB max
Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	– 1, 2, 3	0.02	0.01	0.02		ΔV_{DD} = 12V ± 5%	± %/% max
Output Capacitance for DAC A and DAC B	C_{OUT}	– 1, 2, 3	70				DACA, DACB Loaded with All 0s.	pF max
			140				DAC A, DACB Loaded with All 1s.	
Address Valid to Write Setup Time, t_1	t_{ANS}	– 1, 2, 3	30					ns min
Address Valid to Write Hold Time, t_2	t_{ANH}	– 1, 2, 3	25					ns min
Data Setup Time, t_3	t_{DS}	– 1, 2, 3	80					ns min
Data Hold Time, t_4	t_{DH}	– 1, 2, 3	25					ns min
Chip Select to Write Setup Time, t_5	t_{CWS}	– 1, 2, 3	0					ns min
Chip Select to Write Hold Time, t_6	t_{CWH}	– 1, 2, 3	0					ns min
Write Pulse Width, t_7	t_{WR}	– 1, 2, 3	100					ns min
Clear Pulse Width, t_8	t_{CL}	– 1, 2, 3	100					ns min

NOTES

[1] V_{DD} = + 12V to + 15V ± 10% except where outherwise stated; V_{REFA} = V_{REFB} = 10V; V_{PIN2} = V_{PIN1} = 0V; V_{PIN23} = V_{PIN24} = 0V. Output amplifiers are AD644.
Pin numbers refer to DIP Package.

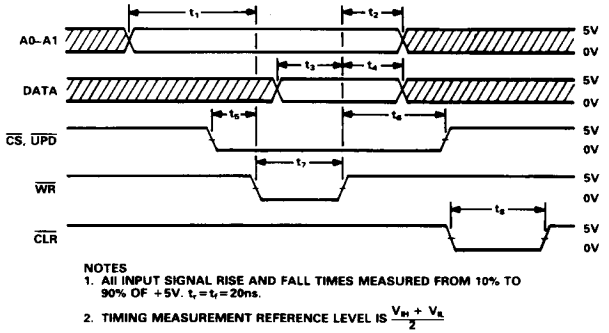
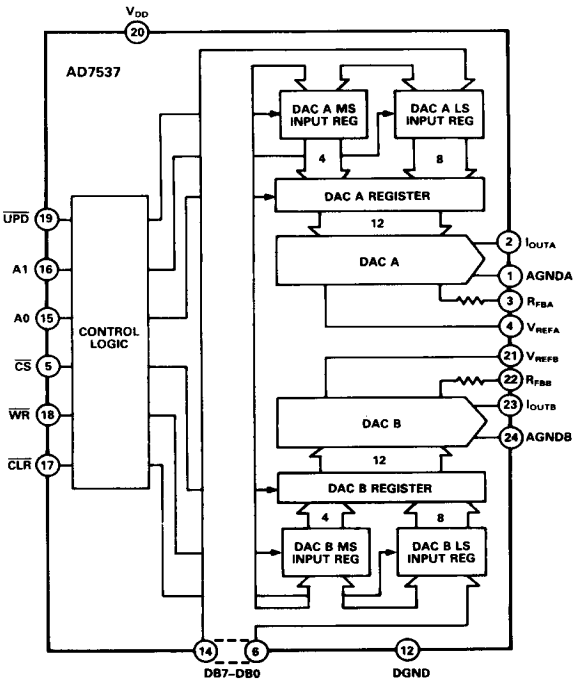
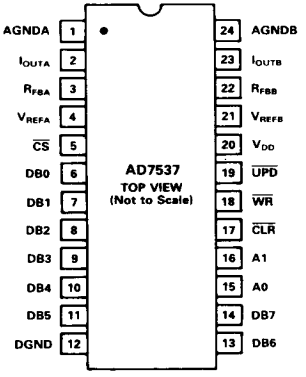


Figure 1. Timing Diagram for AD7537

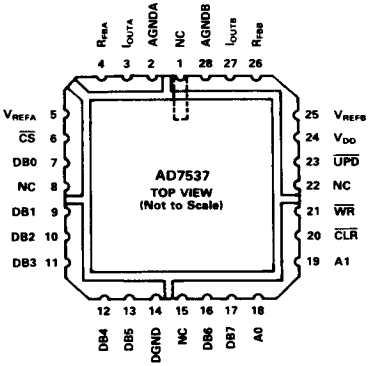
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)

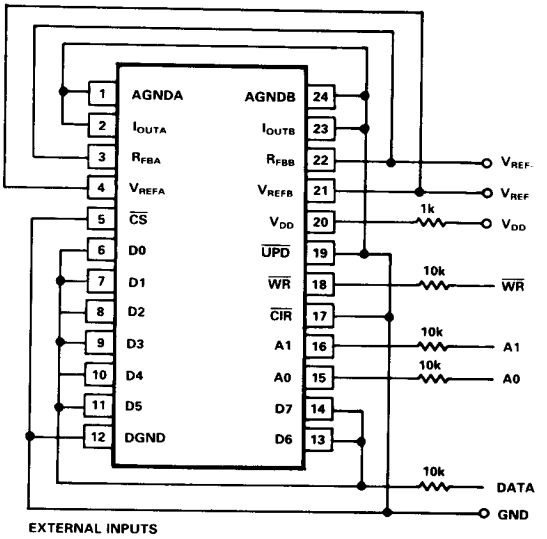


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

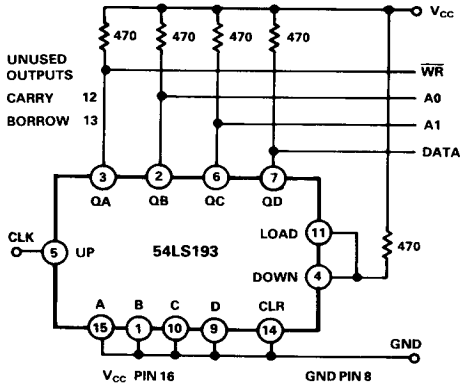
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



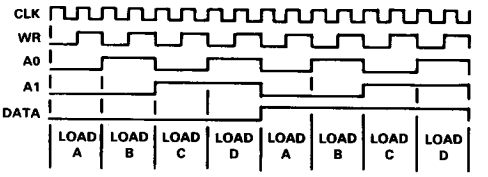
EXTERNAL INPUTS

V_{REF-}	−10V
V_{REF}	10V
V_{DD}	15V
CLK	
GND	

A0, A1, DATA AND $\overline{WR}$ ARE DERIVED FROM THE 54193 CONTROL CIRCUIT.



EXTERNAL INPUTS
V_{CC} 5V
GND
CLK
ALL RESISTORS 10%



1. THERE ARE 6 CONNECTIONS TO EACH BOARD.
   V_{DD} = 15V V_{REF} = 10V
   V_{CC} = 5V V_{REF-} = −10V
   CLOCK GND
2. EACH AD7537 SOCKET HAS 5 RESISTORS ASSOCIATED WITH IT. 1k ON THE V_{DD} LINE, 10k ON THE CONTROL LINES $\overline{WR}$, A0, A1 AND 10k COMMON TO ALL DATA LINES.
3. $\overline{UPD}$ IS TIED LOW SO THE DAC REAR RANK LATCHES ARE TRANSPARENT.
4. THE DAC CODES ARE TOGGLED BETWEEN 0 AND FULL SCALE EVERY 4 CLOCK PULSES.
5. EACH BOARD HAS A 54193 4-BIT COUNTER CONTROLLING THE LOADING AND TOGGLING OF DATA.
6. THIS BOARD IS FOR DYNAMIC BURN-IN ONLY.
7. RESISTOR TOLERANCE 10%.

5.0 Unipolar Binary Operation (2-Quadrant Multiplication)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table 2.

Operational amplifiers A1 and A2 can be in a single package (AD644) or separate packages (AD544, AD OP-27). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high-speed op amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all 0s and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is 0V. Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7537, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

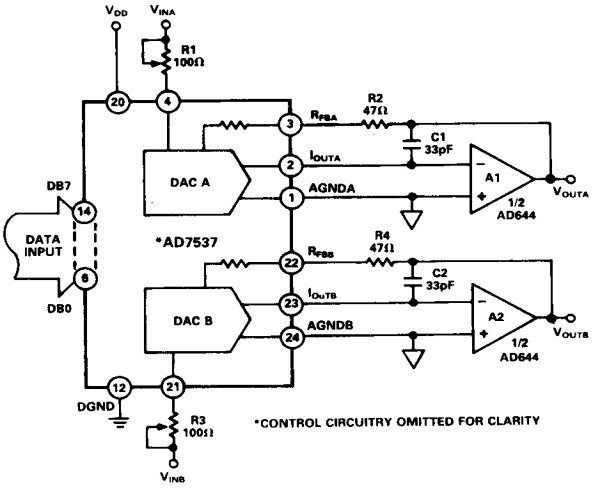


Figure 2. AD7537 Unipolar Binary Operation

Table 2. Unipolar Binary Code Table for Circuit of Figure 2

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

6.0 Bipolar Operation (4-Quadrant Multiplication)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, R10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

If R1, R2 (R3, R4) are not used, then resistors R5, R6, R7 (R8, R9, R10) should be ratio matched to 0.01% to ensure gain error performance to the data sheet specification. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table 3.

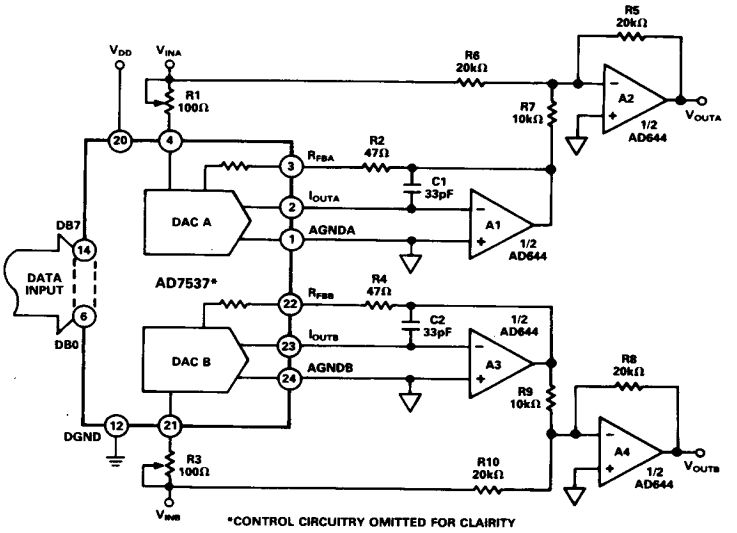


Figure 3. Bipolar Operation (Offset Binary Coding)

Table 3. Bipolar Code Table for Offset Binary Circuit of Figure 3

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right) = -V_{IN}$