

8-Bit Up/Down Counter

74ACT469A

Feature/Benefits

- Direct CMOS replacement of Monolithic Memories' SN74LS469A
- Zero standby power
- 8-bit up/down counter for microprogram-counter, DMA-controller and general-purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Expandable in 8-bit increments

Description

The 'ACT469A is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs (LD, UD, CBI) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE (CBI = LOW), and the up/down control line (UD) is LOW, otherwise the operation is a HOLD. The carry-out (CBO) is TRUE (CBO = LOW) when the output register (Q7-Q0) is all HIGHS, otherwise FALSE (CBO = HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE (CBI = LOW), and the up/down control line (UD) is HIGH, otherwise the operation is a HOLD. The borrow-out (CBO) is TRUE (CBO = LOW) when the output register (Q7-Q0) is all LOWs, otherwise FALSE (CBO = HIGH).

The data output pins are enabled when OE is LOW, and disabled (HI-Z) when OE is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469A 8-bit up/down counters may be cascaded to provide larger counters.

Function Table

| OE | CK | LD | UD | CBI | D7-D0 | Q7-Q0 | OPERATION |
|----|----|----|----|-----|-------|-----------|-----------|
| H | * | * | * | * | * | Z | HI-Z* |
| L | ↑ | L | X | X | D | D | LOAD |
| L | ↑ | H | L | H | X | Q | HOLD |
| L | ↑ | H | L | L | X | Q plus 1 | INCREMENT |
| L | ↑ | H | H | H | X | Q | HOLD |
| L | ↑ | H | H | L | X | Q minus 1 | DECREMENT |

* When OE is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the counter is not affected

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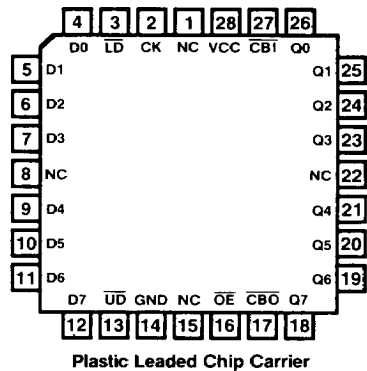
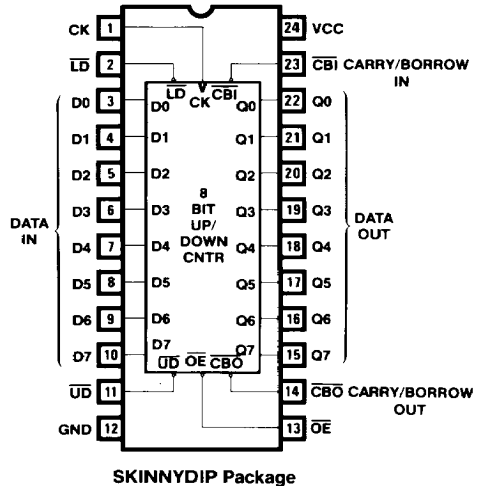
| Publication # | Rev | Amendment |
|---------------------------|-----|-----------|
| 10131 | A | /0 |
| Issue Date: December 1987 | | |

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Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
|-------------|-----------------|-------------|
| 74ACT469A | NS, JS, FN (28) | Com |

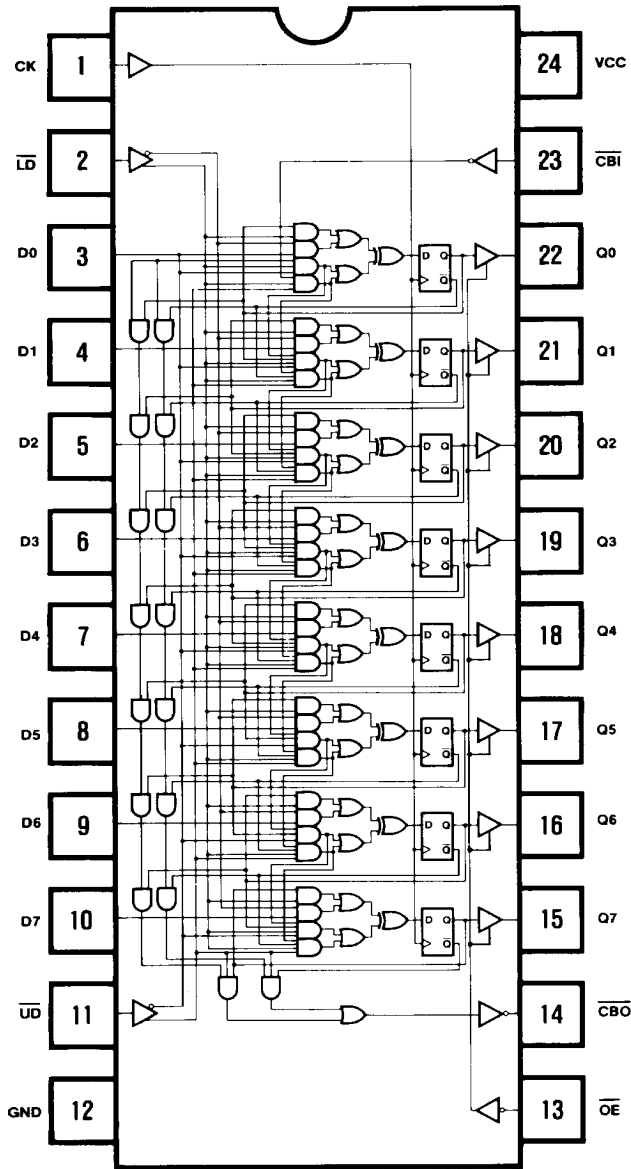
Logic Symbols



Monolithic Memories 

Logic Diagram

8-Bit Up/Down Counter



Operating Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------------|------|-----|------|------|
| V _{CC} | Supply voltage | 4.75 | 5 | 5.25 | V |
| t _w | Width of clock | 15 | 5 | | ns |
| t _{su} | Setup time from input to clock | 30 | 15 | | ns |
| t _h | Hold time | 0 | -10 | | ns |
| T _A | Operating free-air temperature | 0 | 25 | 75 | °C |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|-------------------------------------|---|---|----------------|-----------------|------|
| V _{IL} ² | Low-level input voltage | | 0 | | 0.8 | V |
| V _{IH} ² | High-level input voltage | | 2 | | V _{CC} | V |
| I _{IL} | Low-level input current | V _{CC} = MAX V _I = GND | | | -1 | μA |
| I _{IH} | High-level input current | Pin 10 ³ | | 8 | 30 | μA |
| | | All other pins | V _{CC} = MAX V _I = V _{CC} | | 1 | μA |
| V _{OL} | Low-level output voltage | V _{CC} = MIN I _{OL} = 8 mA | | 0.1 | 0.4 | V |
| | | V _{CC} = 5 V I _{OL} = 1 μA | | | 0.05 | |
| V _{OH} | High-level output voltage | V _{CC} = MIN I _{OH} = -6 mA | 3.76 ⁴ | 4.1 | | V |
| | | V _{CC} = 5 V I _{OH} = -1 μA | 4.95 | | | |
| I _{OZL} ⁵ | Off-state output current | V _{CC} = MAX | V _O = GND | 0 | -10 | μA |
| I _{OZH} ⁵ | | | V _O = V _{CC} | 0 | 10 | μA |
| I _{CC} | Standby supply current ⁶ | I _O = 0 mA, V _I = GND or V _{CC} | 0 | 100 | | μA |
| | Operating supply current | f = 1 MHz, I _O = 0 mA, V _I = GND or V _{CC} | 2 | 5 ⁷ | | mA |

Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See test Load/Waveforms) | MIN | TYP | MAX | UNIT |
|------------------|--------------------------------------|--|-----|-----|-----|------|
| f _{MAX} | Maximum clock frequency ¹ | R _L = 1KΩ C _L = 50 pF | 23 | | | MHz |
| t _{CLK} | Clock to Q | | 12 | | 15 | ns |
| tp _{ZX} | Output enable delay | | 15 | | 20 | ns |
| tp _{XZ} | Output disable delay | R _L = 1K C _L = 5 pF | 15 | | 20 | ns |

Notes: 1. f_{MAX} is derived from: 1/MAX [(t_{su} + t_h) + t_w (Low) + t_w (High) · t_{CLK}].

2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3. Pin 10 DIP, Pin 12 PLCC

6. Disable output pins = V_{CC} or GND.

4. JEDEC standard no. 7 for high-speed CMOS devices.

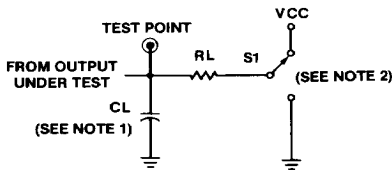
7. Add 3 mA per additional 1.0 MHz of operation over 1 MHz.

5. Applies to pins 14-23 for DIP.

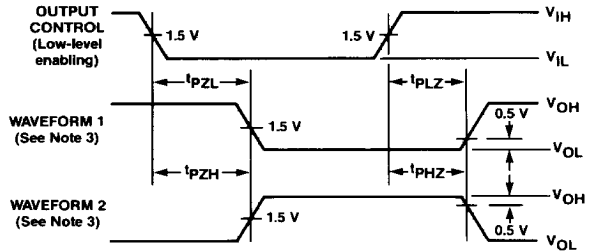
Absolute Maximum Ratings

| | |
|--|----------------------------|
| Supply voltage, V_{CC} | -0.5 V to 7.0 V |
| DC input voltage, V_I | -0.5 V to $V_{CC} + 0.5$ V |
| DC output voltage, V_O | -0.5 V to $V_{CC} + 0.5$ V |
| DC output source/sink current per output pin, I_O | ± 35 mA |
| DC V_{CC} or ground current, I_{CC} or I_{GND} | ± 100 mA |
| Input diode current, I_{IK} : | |
| $V_I < 0$ | -20 mA |
| $V_I > V_{CC}$ | +20 mA |
| Output diode current, I_{OK} : | |
| $V_O < 0$ | -20 mA |
| $V_O > V_{CC}$ | +20 mA |
| Storage temperature | -65°C to +150°C |

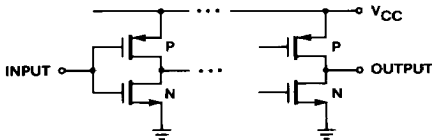
Switching Test Load



Enable/Disable Delay



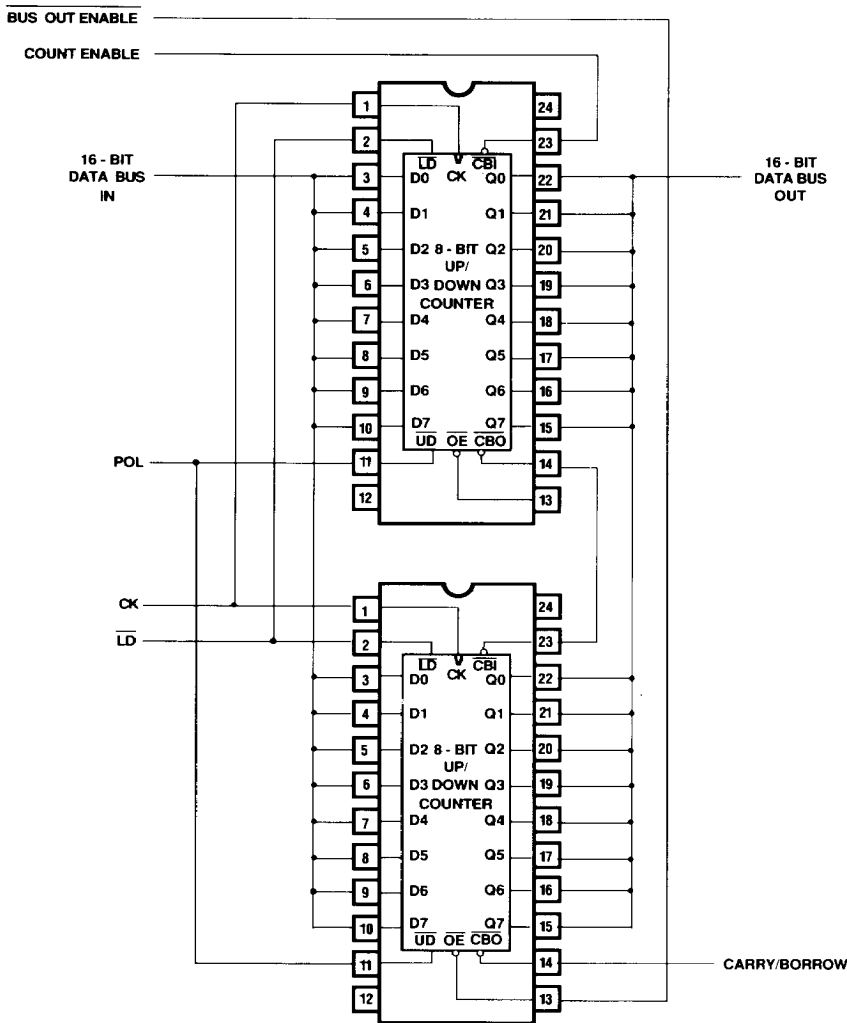
Schematic of Inputs and Outputs



- Notes:
1. C_L includes probe and jig capacitance.
 2. When measuring t_{PLZ} and t_{PZL} , S1 is tied to V_{CC} .
When measuring t_{PHZ} and t_{PZH} , S1 is tied to ground.
 t_{PXZ} is measured with $C_L = 50$ pF.
 t_{PXZ} is measured with $C_L = 5$ pF.
When measuring propagation delay times of three-state outputs, S1 is open, i.e., not connected to V_{CC} or ground.
 3. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Application

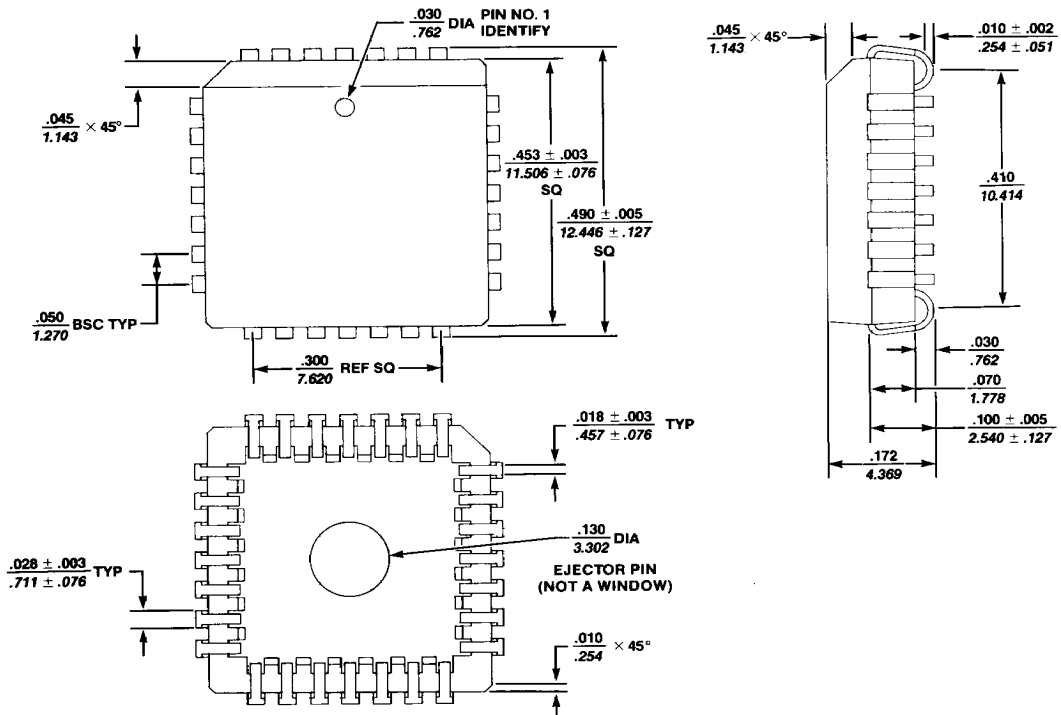
16-Bit Up/Down Counter



NOTE $t_{MAX} = \frac{1}{f_{PD\ CLK\ TO\ CO} \cdot f_{SU}}$

Package Drawings

28NL/FN Plastic Leaded Chip Carrier
(.451" x .451")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE $\pm .007$ INCHES

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