

# Dual D-Type Flip-Flop with Set and Clear With 5V-Tolerant Inputs

The MC74LVX74 is an advanced high speed CMOS D-type flip-flop. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

The signal level applied to the D input is transferred to O output during the positive going transition of the Clock pulse.

Clear ( $\overline{CD}$ ) and Set ( $\overline{SD}$ ) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

- High Speed:  $f_{max} = 145\text{MHz}$  (Typ) at  $V_{CC} = 3.3\text{V}$
- Low Power Dissipation:  $I_{CC} = 2\mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5\text{V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

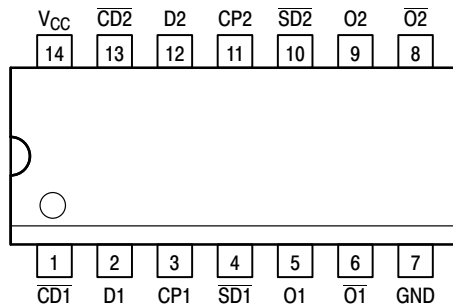


Figure 1. 14-Lead Pinout (Top View)

## MC74LVX74

# LVX

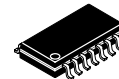
### LOW-VOLTAGE CMOS



**D SUFFIX**  
14-LEAD SOIC PACKAGE  
CASE 751A-03



**DT SUFFIX**  
14-LEAD TSSOP PACKAGE  
CASE 948G-01



**M SUFFIX**  
14-LEAD SOIC EIAJ PACKAGE  
CASE 965-01

#### PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
D1, D2	Data Inputs
$\overline{CD1}$ , $\overline{CD2}$	Direct Clear Inputs
$\overline{SD1}$ , $\overline{SD2}$	Direct Set Inputs
O <sub>n</sub> , $\overline{O_n}$	Outputs

# MC74LVX74

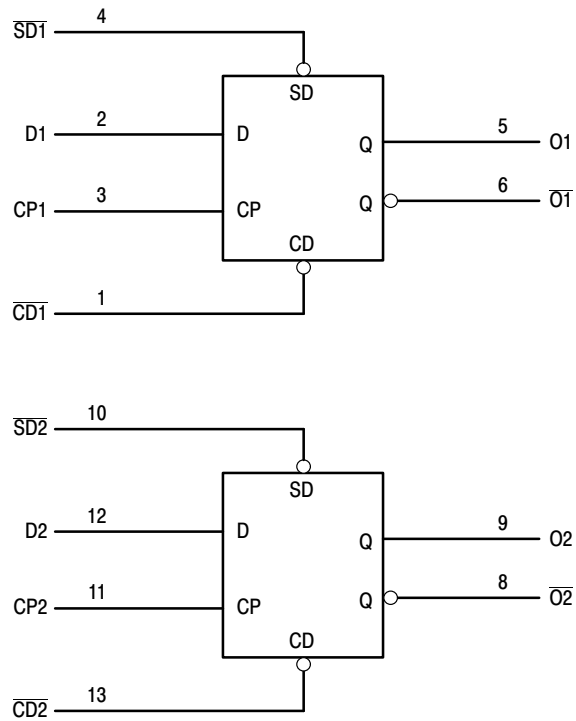


Figure 2. Logic Diagram

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SDn}$	$\overline{CDn}$	$CPn$	$Dn$	$On$	$\overline{On}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	$\uparrow$	h	H	L	Load and Read Register
H	H	$\uparrow$	l	L	H	
H	H	$\nabla$	X	NC	NC	Hold

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable;  $\uparrow$  = Low-to-High Transition;  $\nabla$  = Not a Low-to-High Transition; For  $I_{CC}$  Reasons DO NOT FLOAT Inputs

# MC74LVX74

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.0			2.0		
			3.6	2.4			2.4		
V <sub>IL</sub>	Low-Level Input Voltage		2.0					0.5	V
			3.0					0.8	
			3.6					0.8	
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OH</sub> = -50μA I <sub>OH</sub> = -50μA I <sub>OH</sub> = -4mA	2.0	1.9	2.0		1.9		V
			3.0	2.9	3.0		2.9		
			3.0	2.58			2.48		
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50μA I <sub>OL</sub> = 50μA I <sub>OL</sub> = 4mA	2.0		0.0	0.1		0.1	V
			3.0		0.0	0.1		0.1	
			3.0			0.36		0.44	
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6			±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6			2.0		20.0	μA

# MC74LVX74

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay CP to O or $\bar{O}$	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		7.3 9.8	15.0 18.5	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		5.7 8.2	9.7 13.2	1.0 1.0	11.5 15.0	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay $\bar{SD}$ or $\bar{CD}$ to O or $\bar{O}$	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		8.4 10.9	15.6 19.1	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$		6.6 9.1	10.1 13.6	1.0 1.0	12.0 15.5	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 2.7\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$	55 45	135 60		50 40		MHz
		$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$ $C_L = 50\text{pF}$	95 60	145 85		80 50		
$t_{OSHL}$ $t_{OSLH}$	Output-to-Output Skew (Note 1.)	$V_{CC} = 2.7\text{V}$ $C_L = 50\text{pF}$ $V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5 1.5		1.5 1.5	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

## TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -40 \text{ to } 85^\circ\text{C}$	
$t_w$	Minimum Pulse Width, CP	2.7V 3.3V $\pm 0.3$	8.5 6.0	10.0 7.0	ns
$t_w$	Minimum Pulse Width, $\bar{CD}$ or $\bar{SD}$	2.7V 3.3V $\pm 0.3$	8.5 6.0	10.0 7.0	ns
$t_{su}$	Minimum Setup Time, D to CP	2.7V 3.3V $\pm 0.3$	8.0 5.5	9.5 6.5	ns
$t_h$	Minimum Hold Time, D to CP	2.7V 3.3V $\pm 0.3$	0.5 0.5	0.5 0.5	ns
$t_{rec}$	Minimum Recovery Time, $\bar{SD}$ or $\bar{CD}$ to CP	2.7V 3.3V $\pm 0.3$	6.5 5.0	7.5 5.0	ns

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
		Min	Typ	Max	Min	Max	
$C_{in}$	Input Capacitance		4	10		10	pF
$C_{PD}$	Power Dissipation Capacitance (Note 2.)		25				pF

2.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$  (per flip-flop).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$ , $C_L = 50\text{pF}$ , $V_{CC} = 3.3\text{V}$ , Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.3	0.5	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.3	-0.5	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

# MC74LVX74

## SWITCHING WAVEFORMS

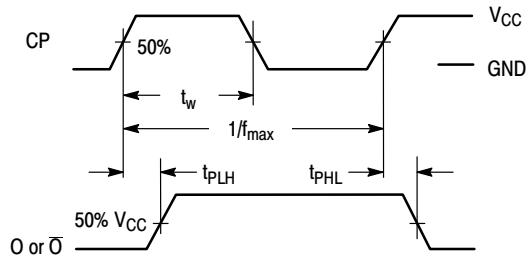


Figure 3.

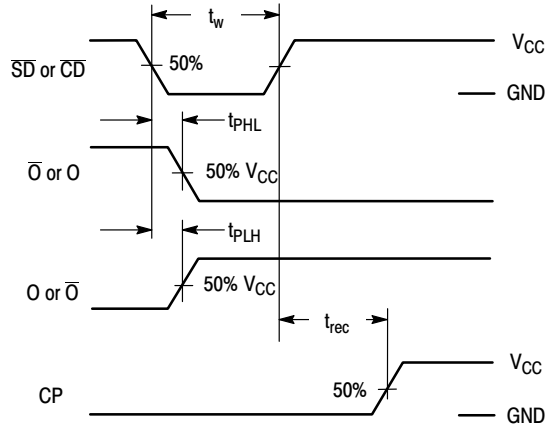


Figure 4.

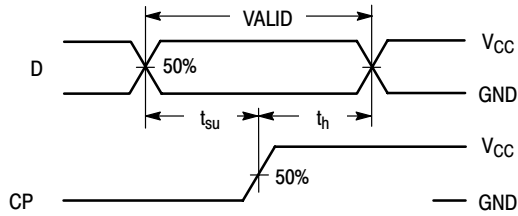
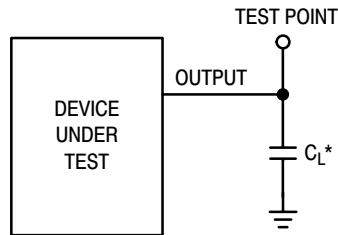


Figure 5.

## TEST CIRCUIT



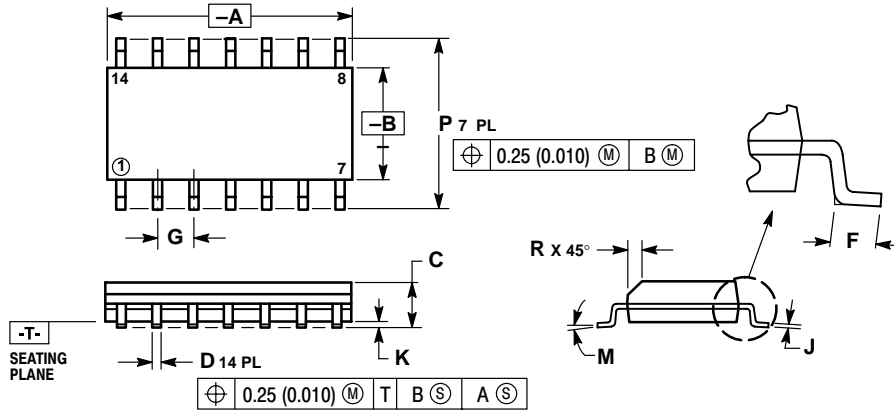
\*Includes all probe and jig capacitance

Figure 6.

# MC74LVX74

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F

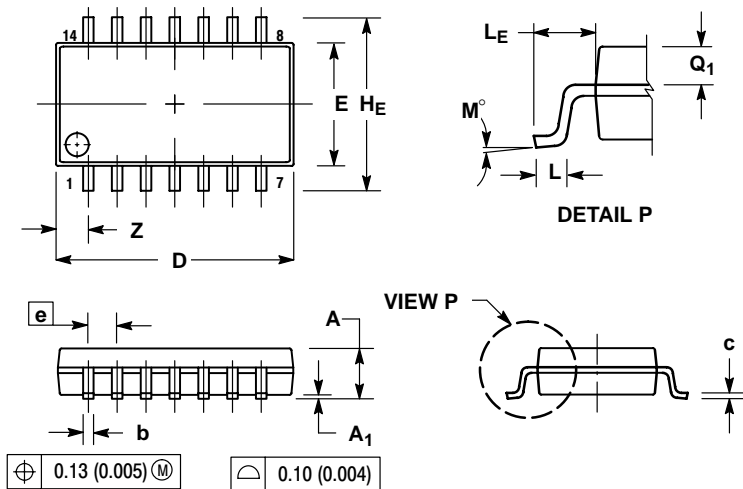


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

### M SUFFIX PLASTIC SOIC EIAJ PACKAGE CASE 965-01 ISSUE O



#### NOTES:

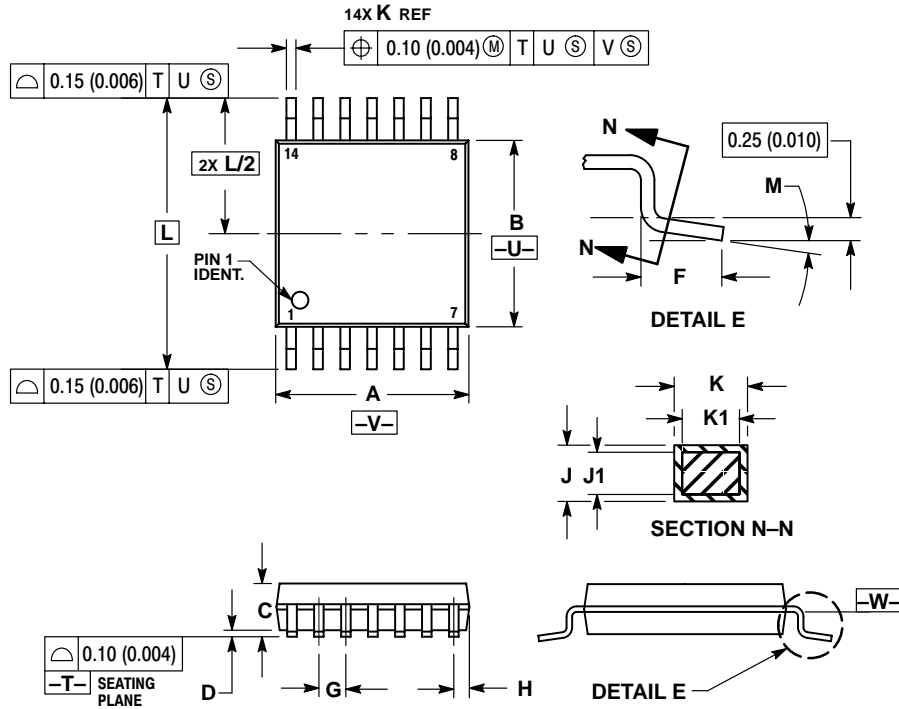
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

# MC74LVX74

## OUTLINE DIMENSIONS


DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 948G-01  
 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### **NORTH AMERICA Literature Fulfillment:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, UK, Ireland

### **CENTRAL/SOUTH AMERICA:**

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com  
**Toll-Free from Mexico:** Dial 01-800-288-2872 for Access –  
then Dial 866-297-9322

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
**Toll Free from Hong Kong & Singapore:**  
**001-800-4422-3781**

**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.