DATEL

PRODUCT DATA SHEET

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **700 KHz minimum throughput**
- **15Mohm input impedance**
- **Pin-programmable input ranges**
- **Low-power, 2.1 Watts**
- **Three-state output buffers**
- **Small 32-pin DIP**

GENERAL DESCRIPTION

DATEL's ADS-125 and ADS-126 are 12-bit, sampling A/D converters with a 700 KHz minimum throughput rate for sinusoidal inputs.

The performance of these converters is based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using unique laser trimming schemes. The ADS-125 and ADS-126 are packaged in 32-pin ceramic DIP's and consume 2.1 Watts.

Input impedance to the sample-and-hold for these devices is 15 Mohms. Both the ADS-125 and the ADS-126 have two pin programmable input voltage ranges. The ADS-125 has ranges of ±10V and 0 to 10V while the ADS-126 has ranges of ±2.5V and 0 to 5V. All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in two's complement, complementary two's complement, straight binary/offset binary or complementary binary/complementary offset binary.

The power requirements are ±15V dc and +5V dc. These parts are available in the commercial 0 degrees Celsius to +70 degrees Celsius and military -55 degrees Celsius to +125 degrees Celsius operating temperature range.

Typical applications include spectrum, transient, vibration and waveform analysis. This device is also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems. For information on high reliability screening, contact the factory.
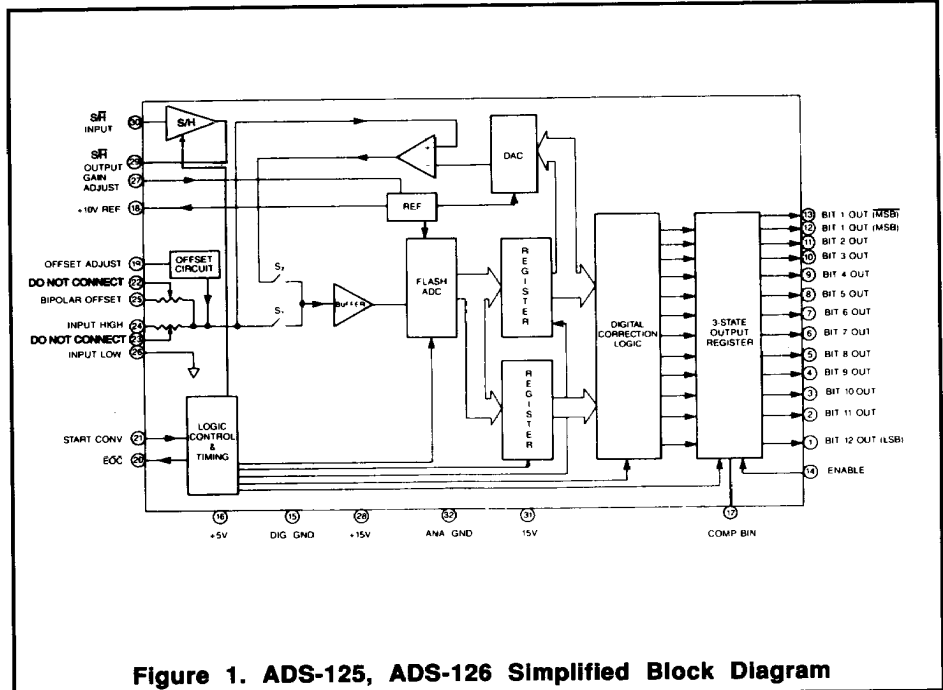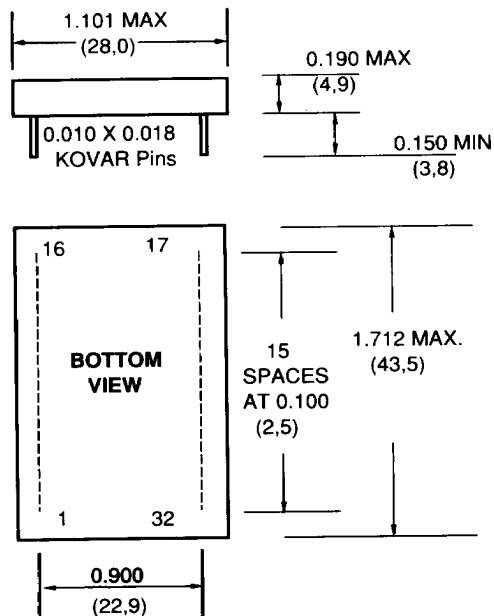
ORDERING INFORMATION
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Figure 1. ADS-125, ADS-126 Simplified Block Diagram

MECHANICAL DIMENSIONS
INCHES (mm)

NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

I/O CONNECTIONS

PIN	FUNCTION
1	Bit 12 OUT (LSB)
2	Bit 11 OUT
3	Bit 10 OUT
4	Bit 9 OUT
5	Bit 8 OUT
6	Bit 7 OUT
7	Bit 6 OUT
8	Bit 5 OUT
9	Bit 4 OUT
10	Bit 3 OUT
11	Bit 2 OUT
12	Bit 1 OUT (MSB)
13	Bit 1 OUT ($\overline{\text{MSB}}$)
14	$\overline{\text{ENABLE}}$
15	DIGITAL GND.
16	+5V
17	$\overline{\text{COMP BIN}}$
18	REF. OUT (+10V dc)
19	OFFSET ADJUST
20	$\overline{\text{EOC}}$
21	START CONVERT
22	DO NOT CONNECT
23	DO NOT CONNECT
24	INPUT HIGH
25	BIPOLAR OFFSET
26	INPUT LOW
27	GAIN ADJUST
28	+15V
29	S/H OUTPUT
30	S/H INPUT
31	-15V
32	ANALOG GND.

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 28)	0 to +18	Volts dc
-15V Supply (Pin 31)	0 to -18	Volts dc
+5V Supply (Pin 16)	-0.5 to +7.0	Volts dc
Digital Inputs		
(Pins 14,17,21)	-0.3 to +6.0	Volts dc
Analog Input (Pin 30)	-15 to +15	Volts dc
Lead Temp. (10 sec.)	300 max.	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range:				
ADS-125	–	±10	–	Volts dc
	–	0 to +10	–	Volts dc
ADS-126	–	±2.5	–	Volts dc
	–	0 to +5	–	Volts dc
Input Impedance	5.0	15.0	–	M ohms
Input Capacitance	–	3	5	pf

DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	2.5	µA
Logic Loading "0"	–	–	-100	µA

A/D PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Integral Non–Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	–	±3	LSB
Integral Non-Lin.Tempco.	–	±5	±10	ppm/ °C
Differential Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	–	±1	LSB
Differential Non-Lin.Tempco.	–	–	±2.5	ppm/ °C
Full Scale Absolute Accuracy				
+25 °C	–	±5	±10	LSB
0 °C to +70 °C	–	±6	±18	LSB
-55 °C to +125 °C	–	±10	±32	LSB
Unipolar Zero Error,				
+25 °C	–	±3	±5	LSB
Unipolar Zero Tempco	–	±15	±30	ppm/ °C
Unipolar Zero Adjust Range	±5	–	–	LSB
Bipolar Zero Error,				
+25 °C	–	±3	±5	LSB
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Zero Adjust Range	±5	–	–	LSB
Bipolar Offset Error,				
+25 °C	–	±4	±8	LSB
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Bipolar Offset Adjust Range	±5	–	–	LSB
Gain Error, +25 °C	–	±4	±8	LSB
Gain Tempco	–	±20	±40	ppm/ °C
Gain Error Adjust Range	±5	–	–	LSB
Conversion Times:				
+25 °C	–	–	800	nSec.
0 °C to +70 °C	–	–	850	nSec.
-55 °C to +125 °C	–	–	880	nSec.
No Missing Codes (12 Bits)	Over the Operating Temp. Range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Resolution		12 Bits		
Output Coding:		Straight binary/offset binary		
(Pin 17 Hi)		Complementary binary		
(Pin 17 Low)		Complementary offset binary		
		Two's complement		
(Note 4)		Complementary Two's complement		
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	9.98	10.0	10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA

SAMPLE/HOLD PERFORMANCE				
Slew Rate	–	90	–	V/µSec
Aperture Delay Time	–	20	–	nSec
Aperture Uncertainty	–	±100	–	pSec
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	–	–	715	nSec
0 °C to +70 °C	–	–	765	nSec
-55 °C to +125 °C	–	–	900	nSec
(Sinusoidal Input)	–	–	395	nSec

POWER REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+70	+82	mA
-15V dc Supply	–	-52	-61	mA
+5V dc Supply*	–	+66	+71	mA
Power Dissipation	–	2.1	2.4	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V

PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-Pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12 grams)			

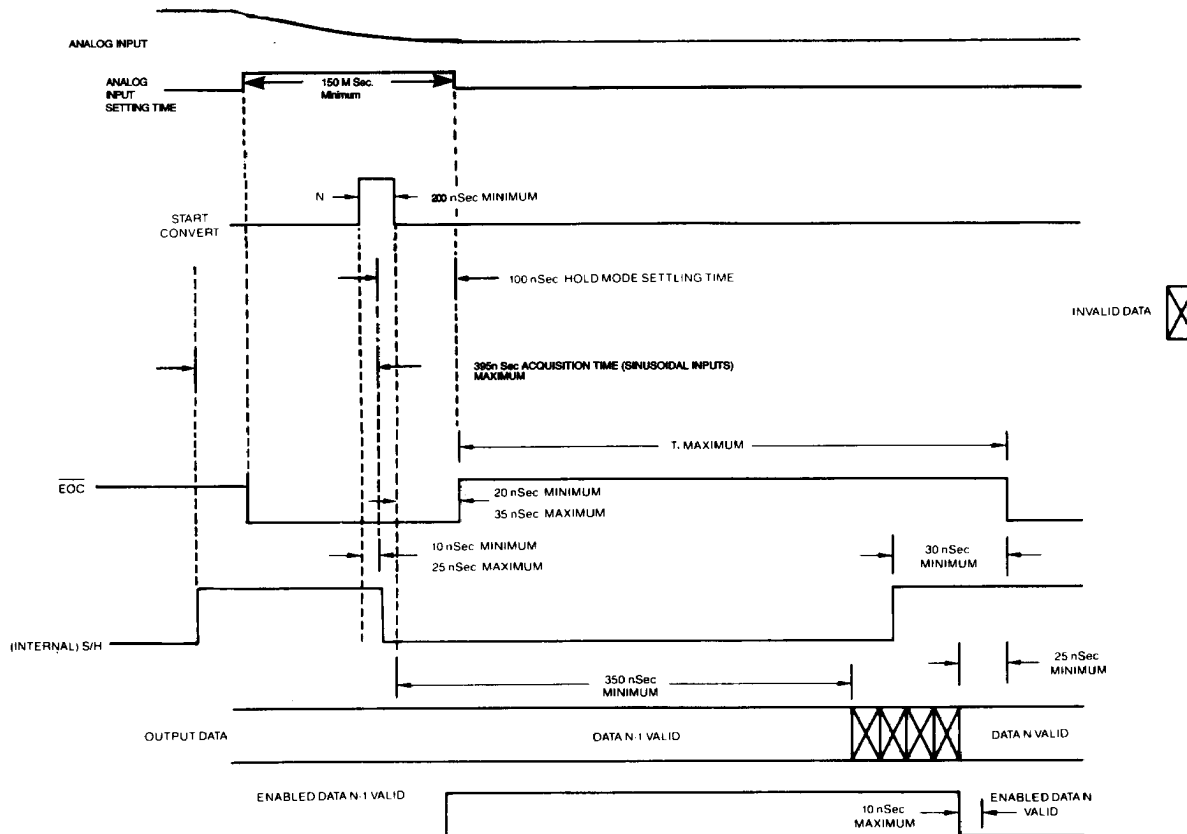* +5V power usage at 1 TTL logic loading per data output bit.

Figure 2. ADS-125, ADS-126 TIMING DIAGRAM

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K Ohm trimming potentiometer for gain adjustment with the wiper tied to pin 27 (ground pin 27 for operation without adjustments). Use a 20K Ohm trimming potentiometer with the wiper tied to pin 19 for zero/offset adjustment (leave pin 19 open for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass the analog and digital supplies and the +10V reference (pin-18) to ground with a 4.7 μF, 25V tantalum electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor. Bypass the +10V reference (pin 18) to analog ground (pin 32).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 17) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP

INPUT CONNECTIONS

Table 2a. ADS-125 Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
Bipolar ± 10Vdc	Pin 30	tie Pin 29 to Pin 24 tie Pin 18 to Pin 25
Unipolar 0 to +10V dc	Pin 30	tie Pin 29 to Pin 24 tie Pin 24 to Pin 25

Table 2b. ADS-126 Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
Bipolar ± 2.5V	Pin 30	tie Pin 29 to Pin 24, & tie Pin 25 to Pin 18
Unipolar 0 to +5V dc	Pin 30	tie Pin 29 to Pin 24 tie Pin 25 to Pin 26

Table 3a. Zero and Gain Adjust for Unipolar Operation

UNIPOLAR FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +5V dc	+0.61mV dc	+4.9982V dc
0 to +10V dc	+1.22mV dc	+9.9963V dc

Table 3b. Zero and Gain Adjust for Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±2.5V dc	+0.61mV dc	+2.4985V dc
±10V dc	+2.44mV dc	+9.9927V dc

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users desiring logic control of this function. In the bipolar mode, two's complement or complementary two's complement output coding is available by using the MSB output (pin 13). MSB (pin 13) does not have a three-state output.

5. The three-state outputs are enabled by connecting ENABLE (pin 14) to a logic "0" (low). MSB (pin 13) does not have a three-state output and therefore is not controlled by ENABLE.

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

Table 1. Signal Timing Summary

LINE	DURATION IN NANOSECONDS
START CONVERT Pulse Width	200 nSec. minimum
START CONVERT Low to EOC High Propagation Delay	35 nSec. maximum
START CONVERT Low to Previous Output Data Invalid	350 nSec. minimum
Data Valid Before EOC goes Low	25 nSec. minimum
ENABLE to Output Data Valid Propagation Delay	10 nSec. maximum
EOC Low to START CONVERT High (Sinusoidal Inputs)	355 nSec. minimum

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 21) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
Apply a precision voltage reference source between the analog input and ground, refer to Table 2 for input pin. Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+ 1/2 LSB) or the bipolar zero adjustment (zero +1/2 LSB) for the appropriate FSR. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 17) tied high (Straight Binary) or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN pin tied low (Complementary Binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 17) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN (pin 17) tied low (complementary offset binary). Two's comple-

ment and complementary two's complement requires the use of MSB versus MSB as given for offset binary or complementary offset binary respectively.

3. Full-Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+FS -1 1/2 LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 17) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN pin tied low. Two's Complement and Complementary Two's Complement respectively requires using MSB versus MSB.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

Table 6. Dynamic Performance

Throughput Rate (Sinusoidal Inputs)	MIN	TYP	MAX	UNITS
+25 °C	700	–	–	KHz
0 °C to +70 °C	670	–	–	KHz
-55 °C to +125 °C	650	–	–	KHz
A/D Conversion Time				
+25 °C	–	–	800	nSec
0 °C to +70 °C	–	–	850	nSec
-55 °C to +125 °C	–	–	880	nSec
Total Harmonic Distortion				
DC to 100 KHz at Vin = <5V p-p	-65	-70	–	dB
DC to 60 KHz at Vin = 10V p-p	-65	-70	–	dB
DC to 25 KHz at Vin = 20V p-p	-65	-70	–	dB

The performance characteristics shown in Table 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

THEORY OF OPERATION

This theory of operation describes the ADS-125/126's function in conjunction with its internal sample-and-hold amplifier for digitizing sinusoidal signals. The ADS-125/126 employs a subranging A/D conversion architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the connection diagram, block diagram, and timing diagram as needed.

The ADS-125/126 guarantees a 650 KHz throughput rate over the temperature range when the START CONVERT pulse of 200 nanoseconds is provided at a 650 KHz rate. The 650 KHz rate is based upon sinusoidal input frequencies up to those specified in the harmonic distortion specifications. The acquisition time for pulse or DC level signals is longer and listed under the acquisition specifications (10V step).

The ADS-125/126 is in the sample mode when the S/H CONTROL pin is high (S/H is in high-state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to S/H CONTROL low. This assures the sample-hold has the minimum required acquisition time for the

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particular application mode. Sinusoidal inputs being digitized by utilizing a repetitive START CONVERT pulse will automatically give the appropriate acquisition time when continuously sampling.

Upon going into the hold mode, there will be a 225 nanosecond delay before EOC goes high and the A/D conversion begins. This consists of the remaining 190 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 35 nanosecond maximum delay from START CONVERT low to EOC high. The hold mode settling time and input settling time requirements required the first pass of the A/D conversion are met when observing this time.

After conversion is initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate input range, is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

When the first pass finishes, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least seven significant bits. The outputs from the two registers are then combined by the digital correction logic to produce a 12-bit word. EOC goes low, indicating the conversion is complete, and the output passes to the three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed (EOC going low). The Sample/Hold Control output goes high shortly before EOC goes low, indicating that the S/H is back sampling the input. This feature improves the overall throughput rate of the ADS-125/126.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before EOC goes low and valid up to 350 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput rate of the ADS-125/126 for sinusoidal inputs consists of 395 nanoseconds for the acquisition time, 225 nanoseconds for the START CONVERT and min-max propagation delays, 880 nanoseconds for A/D conversion time minus 30 nanoseconds for the S/H CONTROL pin. A throughput time of 1470 nanoseconds is obtained and a 650 KHz throughput rate is realized.

Combining the A/D and S/H in one device allows the ADS-125/126 to guarantee a throughput rate of 650 KHz over the -55 °C to +125 °C temperature range for the complete system. Retriggering of the START CONVERT pulse before EOC goes low will not initiate a new conversion.
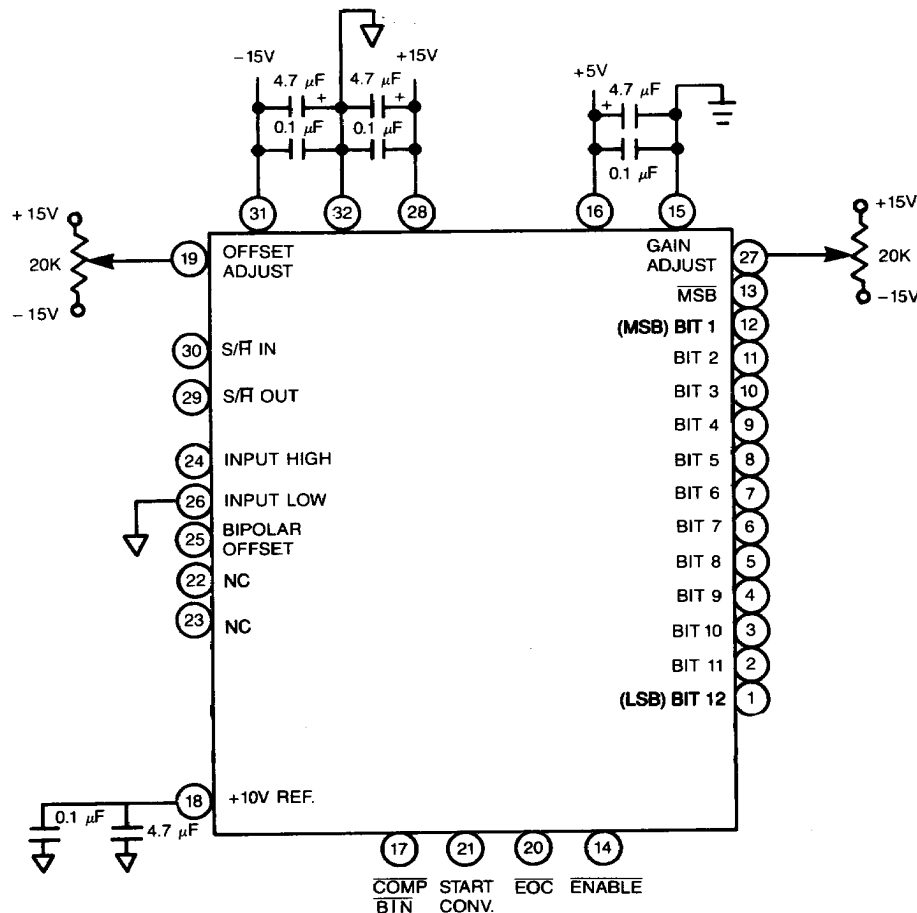

Figure 3. ADS-125, ADS-126 CALIBRATION CIRCUIT

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UNIPOLAR SCALE	INPUT RANGES, VOLTS dc		OUTPUT CODING	
	0 to +10V	0 to +5V	Straight Binary MSB ⟶ LSB	Comp. Binary MSB ⟶ LSB
+FS-1LSB	+9.9976V	+4.9988V	1111 1111 1111	0000 0000 0000
7/8 FS	+8.7500V	+4.3750V	1110 0000 0000	0001 1111 1111
3/4 FS	+7.5000V	+3.7500V	1100 0000 0000	0011 1111 1111
1/2 FS	+5.0000V	+2.5000V	1000 0000 0000	0111 1111 1111
1/4 FS	+2.5000V	+1.2500V	0100 0000 0000	1011 1111 1111
1/8 FS	+1.2500V	+0.6250V	0010 0000 0000	1101 1111 1111
1 LSB	+0.0024V	+0.0012V	0000 0000 0001	1111 1111 1110
0	0.0000V	0.0000V	0000 0000 0000	1111 1111 1111

Table 5. OUTPUT CODING FOR BIPOLAR OPERATION

BIPOLAR SCALE	INPUT RANGE ±10V dc	±2.5V dc	OUTPUT CODING			
			Offset Binary MSB ⟶ LSB	Comp Offset Binary MSB ⟶ LSB	Comp Two's Comp MSB ⟶ LSB	Two's Comp MSB ⟶ LSB
+FS -1 LSB	+9.9951V	+2.4988	1111 1111 1111	0000 0000 0000	1000 0000 0000	0111 1111 1111
+3/4 FS	+7.5000V	+1.8750	1110 0000 0000	0001 1111 1111	1001 1111 1111	0110 0000 0000
+1/2 FS	+5.0000V	+1.2500	1100 0000 0000	0011 1111 1111	1011 1111 1111	0100 0000 0000
0	0.0000V	0.0000	1000 0000 0000	0111 1111 1111	1111 1111 1111	0000 0000 0000
-1/2 FS	-5.0000V	-1.2500	0100 0000 0000	1011 1111 1111	0011 1111 1111	1100 0000 0000
-3/4 FS	-7.5000V	-1.8750	0010 000 0000	1101 1111 1111	0101 1111 1111	1010 0000 0000
-FS +1 LSB	-9.9951V	-2.4988	0000 0000 0001	1111 1111 1110	0111 1111 1110	1000 0000 0001
-FS	-10.000V	-2.5000	0000 0000 0000	1111 1111 1111	0111 1111 1111	1000 0000 0000

ORDERING INFORMATION

MODEL NO.	OPER. TEMP. RANGE	SEAL
ADS-125MC	0 °C to +70 °C	Hermetic
ADS-126MC	0 °C to +70 °C	Hermetic
ADS-125MM	-55 °C to +125 °C	Hermetic
ADS-126MM	-55 °C to +125 °C	Hermetic

ACCESSORIES

Part Number	Description
TP20K	Trimming Potentiometers (Two required)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket),32 required.

For high reliability versions of the ADS-125 and the ADS-126 contact DATEL.

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