FAST PAGE MODE DYNAMIC RAM 8M × 36 288M BIT

Type name	Max. Access time (ns)	Load memory	Outward dimensions W × H × D (mm)	Data sheet page
MH8M36AJ-6 ★	60	M5M417400AJ × 16 + M5M44100BJ × 8	107.95 × 33.85 × 8.6	3/13
MH8M36NAJ-6 ★				
MH8M36AJ-7 ★	70			
MH8M36NAJ-7 ★				
COMMON DATA				4/13

★ : New product

MH8M36AJ-6,-7/ MH8M36NAJ-6,-7

FAST PAGE MODE 301989888-BIT (8388608-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH8M36AJ/NAJ is 8388608-word × 36-bit dynamic RAM. This consists of sixteen industry standard 4M × 4 dynamic RAMs in SOJ and eight industry standard 4M × 1 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required. This is a socket-type memory module, suitable for easy interchange or addition of moudules.

FEATURES

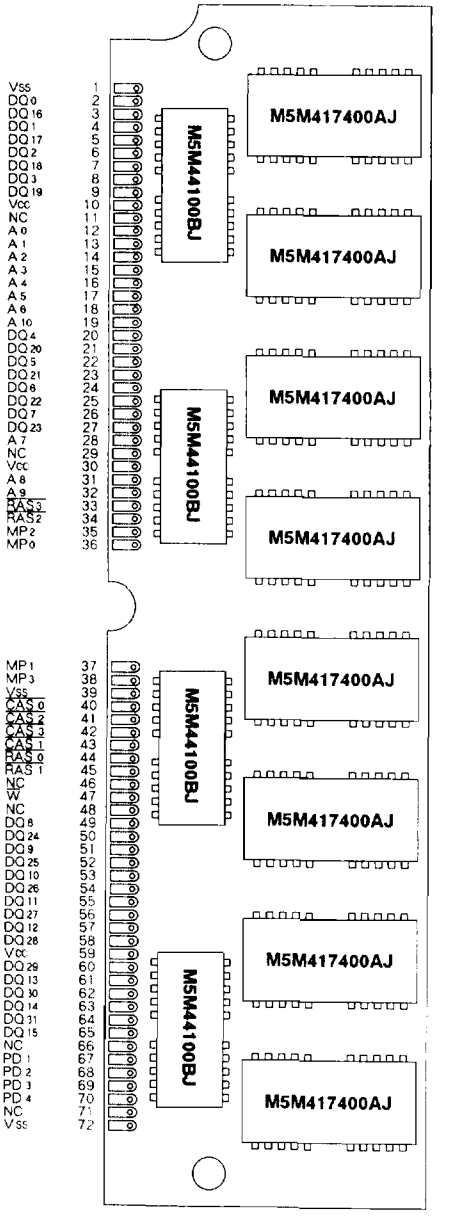
Type name	Access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
MH8M36AJ/NAJ-6	60	110	5200
MH8M36AJ/NAJ-7	70	130	4480

- Utilizes industry standard 4M × 4 RAMs in SOJ and industry standard 4M × 1 RAMs in SOJ
- 72-pins single In-line package
- Single + 5V (± 10%) supply operation
- Low stand-by power dissipation
  132mW(max) ····· CMOS input level
- Low operating power dissipation
  MH8M36AJ, NAJ-6 ····· 7.64W(max)
  MH8M36AJ, NAJ-7 ····· 6.51W(max)
- All inputs, are directly TTL compatible
- All outputs are three-state and directry TTL compatible
- Includes (0.22μF × 24) decoupling capacitors
- 2048 refresh cycles every 32ms (A_0~A_{10})
- Fast-page mode capability
- The common I/O feature dicatates the use of only early write operation to prevent contention on data-in and data-out
- MH8M36AJ is gold plating contact
  MH8M36NAJ is solder with Nickel underplating contact

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW) (Both side)



Outline 72N9U-B

	-6	-7
PD_1	NC	NC
PD_2	Vss	Vss
PD_3	NC	Vss
PD_4	NC	NC

NC : NO CONNECTION

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FUNCTION

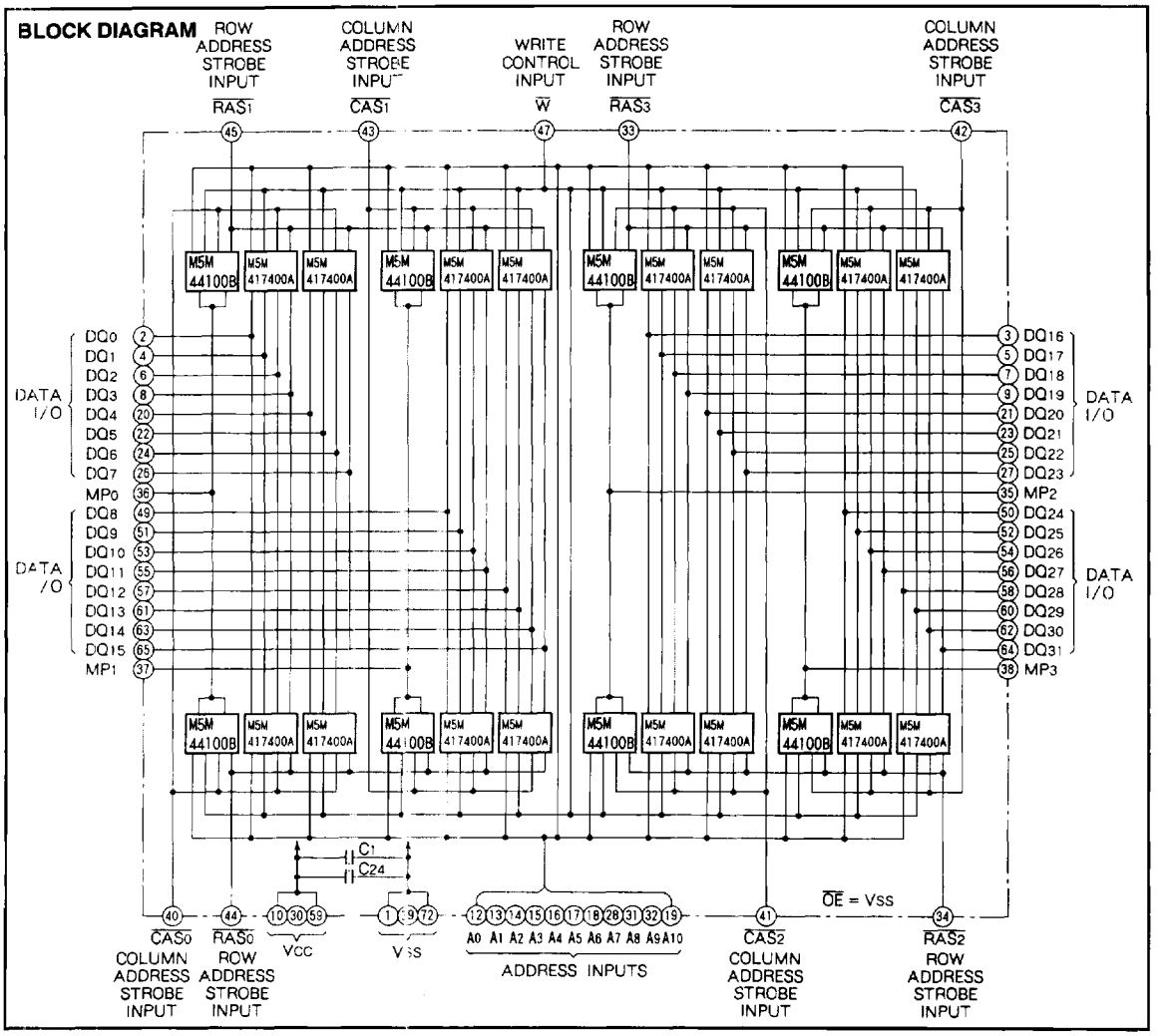
In addition to normal read,and early write operations, a rumber of other functions, e. g.,fast-page mode, $\overline{RAS}$-only refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

MH8M36AJ
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FAST PAGE MODE 301989888-BIT (8388608-WORD BY 36-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	T_a = 25℃	24	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1. All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−20		20	μA
I_I	Input current		0≦V_{IN}≦6.5V, Other inputs pins = 0V	−240		240	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	MH8M36-6	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = twc = min. output open			1624	mA
		MH8M36-7				1204	
$I_{CC2(AV)}$	Supply current from V_{CC}, stand-by		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			48	mA
			$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.5V			24	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	MH8M36-6	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min. output open			2720	mA
		MH8M36-7				2360	
$I_{CC4(AV)}$	Average supply current from V_{CC}, Fast-Page-Mode (Note 3, 4)	MH8M36-6	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min. output open			904	mA
		MH8M36-7				764	
$I_{CC5(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH8M36-6	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min. output open			2600	mA
		MH8M36-7				2280	

Note 2. Current flowing into an IC is positive, out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I = V_{SS} f = 1MHz V_i = 25mVrms			180	pF
$C_{I(DQ)}$	Data input/data output capacitance				40	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				240	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				70	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				70	pF

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SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter		Limits				Unit
			MH8M36-6		MH8M36-7		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6, 7)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6, 8)		60		70	ns
tAA	Column address access time	(Note 6, 9)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		35		40	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	20	ns

Note 5. An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6. Measured with a load circuit equivalent to 2TTL loads and 100pF.
7. Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
8. Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD or tRAD exceeds the value shown.
9. Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.
10. Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
11. $t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 20\mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Early Write, Fast-Page Mode Cycles)

(Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 12, 13)

Symbol	Parameter		Limits				Unit
			MH8M36-6		MH8M36-7		
			Min	Max	Min	Max	
tREF	Refresh cycle time			32		32	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tT	Transition time	(Note 17)	1	50	1	50	ns

Note 12. The timing requirements are assumed tT = 5ns.
13. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14. $t_{RCD(max)}$ is specified as a reference point only. If tRCD is less than $t_{RCD(max)}$, access time is tRAC. If tRCD is greater than $t_{RCD(max)}$, access time is controlled exclusively by tCAC or tAA. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$.
15. $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by tAA.
16. $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by tCAC.
17. tT is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

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Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		MH8M36-6		MH8M36-7		
		Min	Max	Min	Max	
tRC	Read cycle time	110		130		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 18)	0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 18)	10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		ns

Note 18. Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write Cycles)

Symbol	Parameter	Limits				Unit
		MH8M36-6		MH8M36-7		
		Min	Max	Min	Max	
tWC	Write cycle time	110		130		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 19)	0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	10		10		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns

Note 19. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle.

Fast-Page Mode Cycle (Read, Early Write Cycles) (Note 20)

Symbol	Parameter	Limits				Unit
		MH8M36-6		MH8M36-7		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		ns
tPRWC	Fast page mode read write cycle time	85		90		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 21)	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width (Note 22)	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		ns

Note 20. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
21. $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
22. $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 23)

Symbol	Parameter	Limits				Unit
		MH8M36-6		MH8M36-7		
		Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		15		ns

Note 23. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

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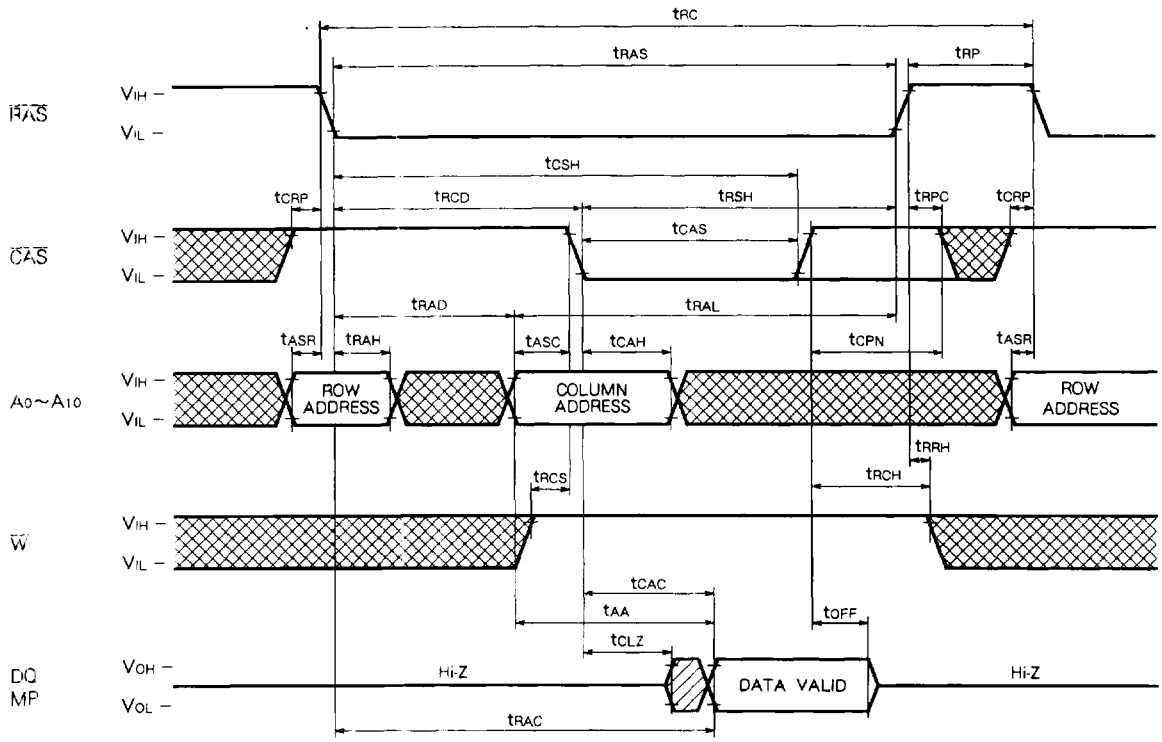
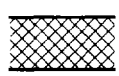
Timing Diagrams (Note 24)
Read Cycle



Note 24



Indicates the don't care input.
$V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$

Indicates the invalid output.

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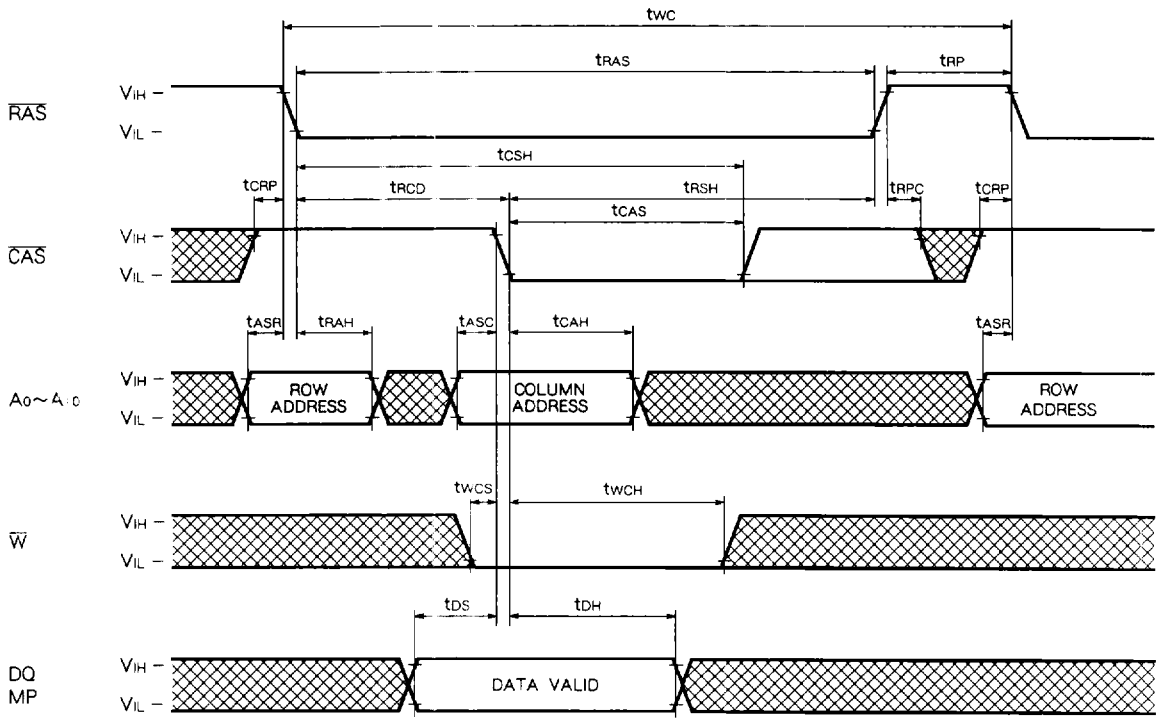
Write Cycle (Early write)



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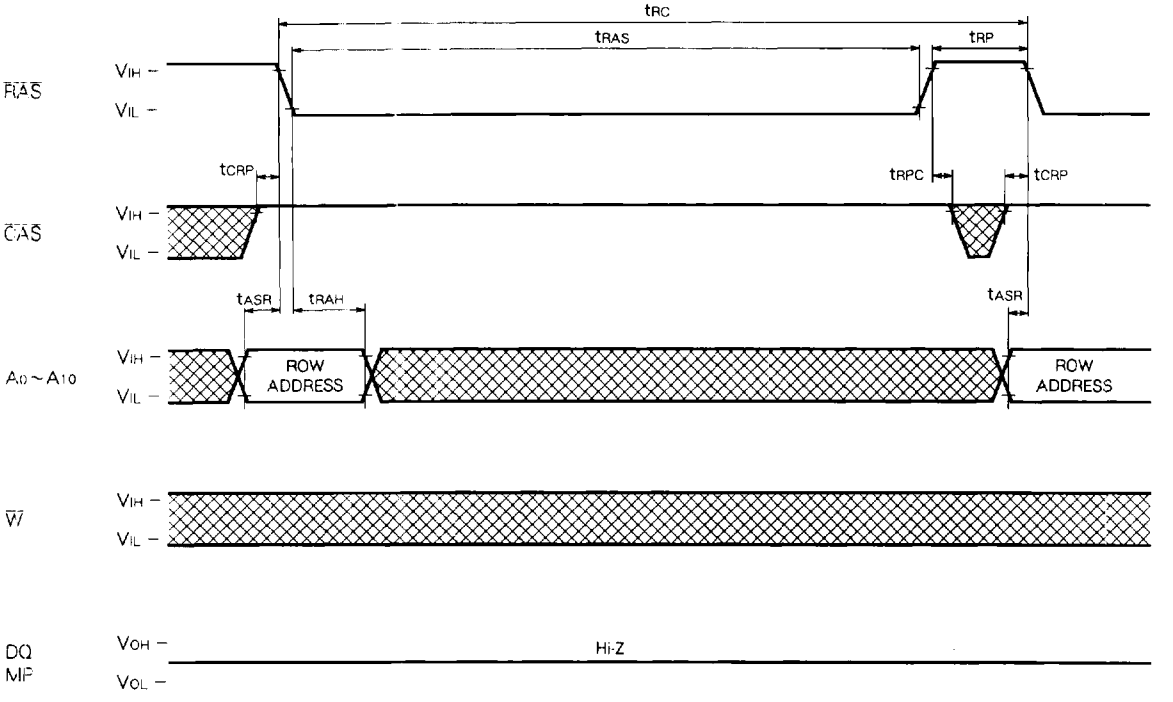
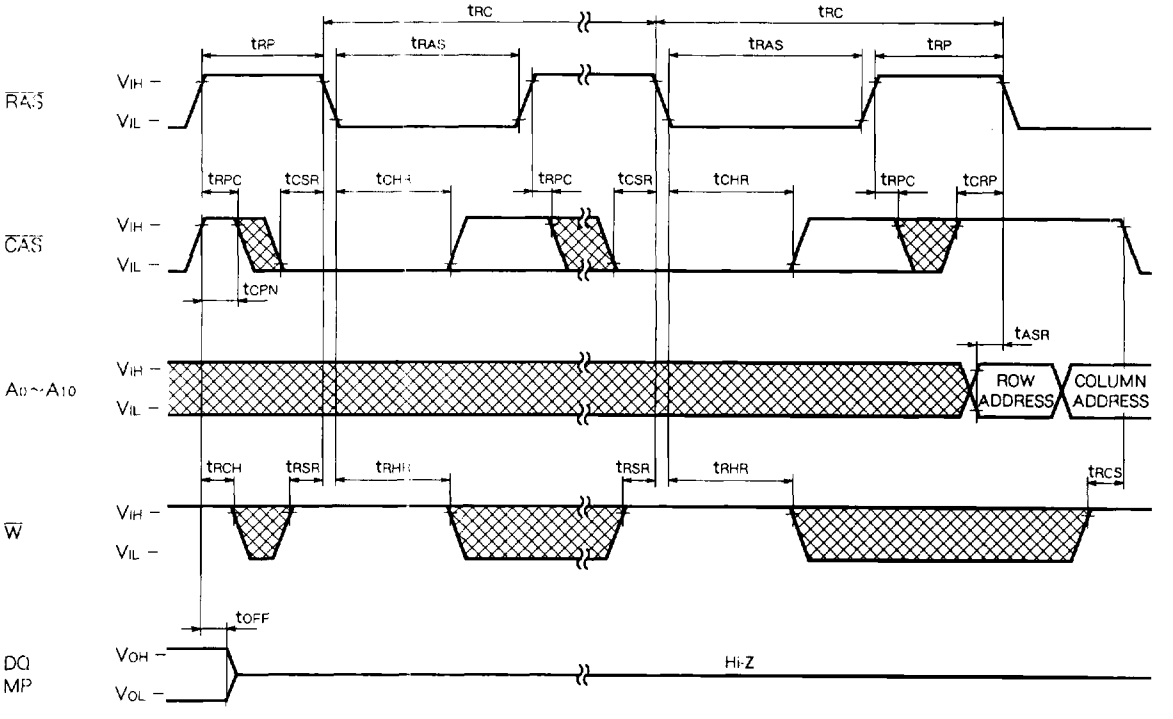
RAS-only-Refresh Cycle



CAS before RAS Refresh Cycle



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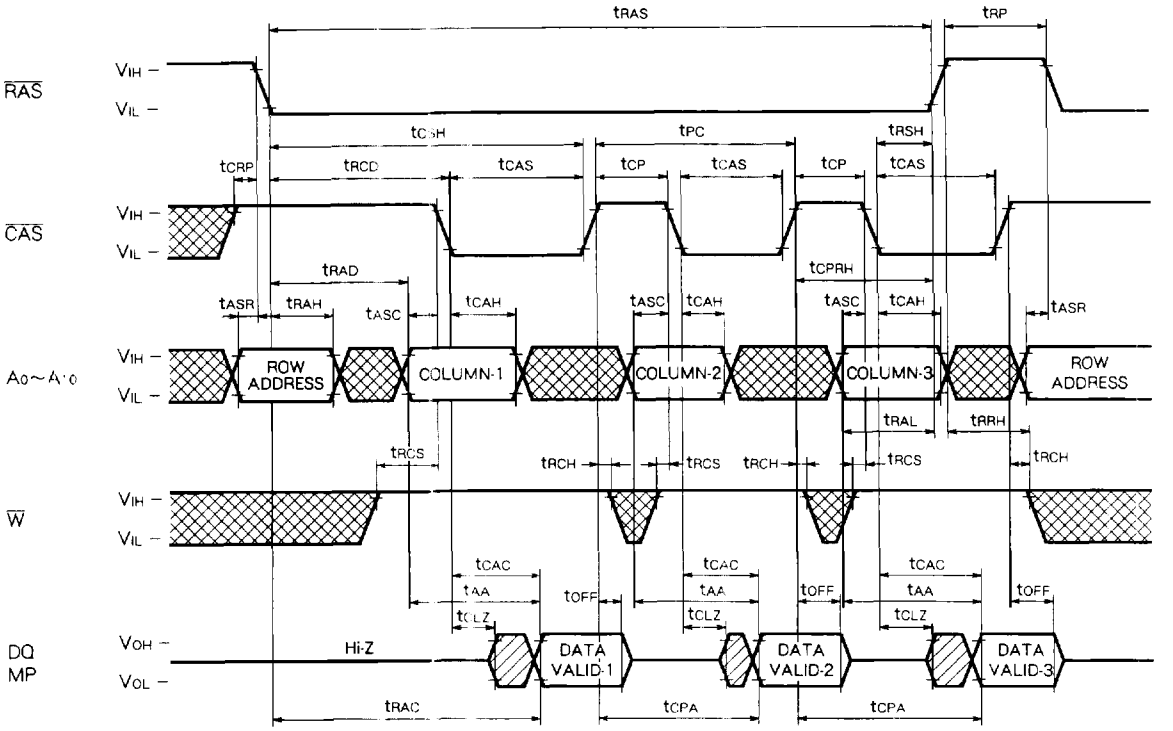
Fast-Page-Mode Read Cycle



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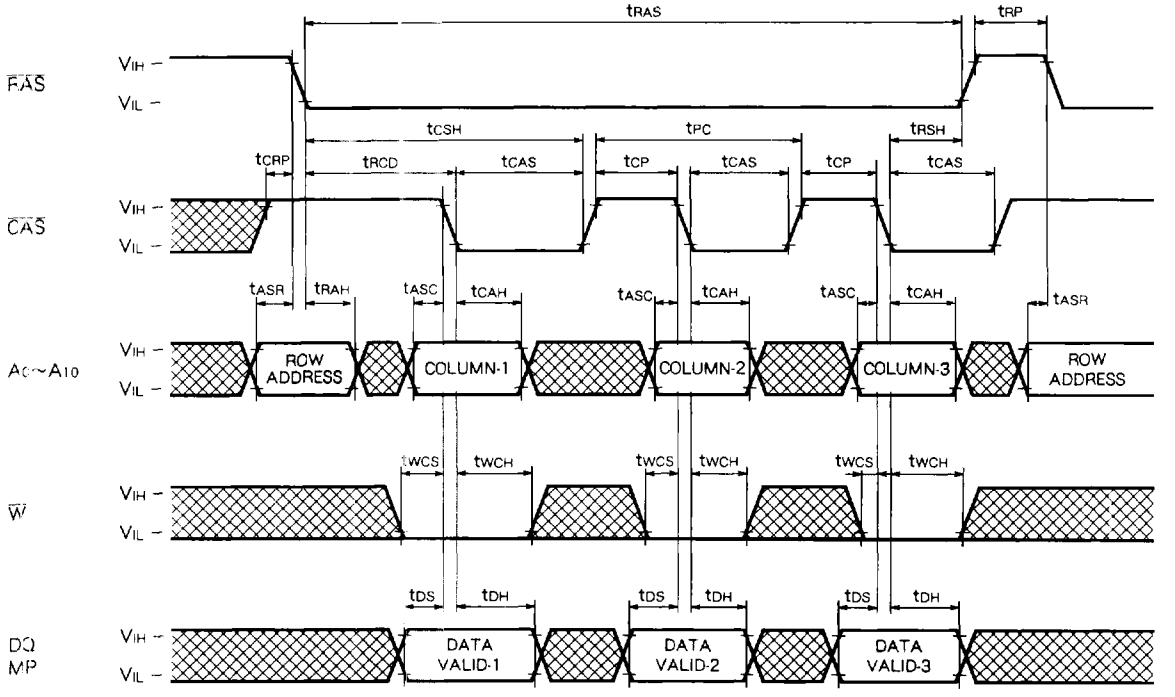
Fast-Page-Mode Write Cycle (Early Write)



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Hidden Refresh Cycle (Read)