IS71V08F32xS08
IS71V16F32xS08

ISSI®

3.0 Volt-Only Flash & SRAM COMBO with Stacked Multi-Chip Package (MCP) — 32 Mbit Simultaneous Operation Flash Memory and 8 Mbit Static RAM

PRELIMINARY INFORMATION
MAY 2002

MCP FEATURES

- Power supply voltage 2.7V to 3.3V
- High performance:
  Flash: 70ns maximum access time
  SRAM: 70ns maximum access time
- Package:
  73-ball BGA - 32 Mbit Flash/8 Mbit SRAM
- Operating Temperature: -40C to +85C

FLASH FEATURES

- Power Dissipation:
  Read Current at 1 Mhz: 7 mA maximum
  Read Current at 5 Mhz: 18 mA maximum
  Sleep Mode: 5 µA maximum
- Simultaneous Read and Write Operations:
  Zero latency between read and write operations; Data can be programmed or erased in one bank while data is simultaneously being read from the other bank
- Low-Power Mode:
  A period of no activity causes flash to enter a low-power state
- Erase Suspend/Resume:
  Suspends of erase activity to allow a read in the same bank
- Sector Erase Architecture:
  8 words of 4k size and 63 words of 32K size (32 Mbit)
  Any combination of sectors, or the entire flash can be simultaneously erased
- Erase Algorithms:
  Automatically preprograms/erases the flash memory entirely, or by sector
- Program Algorithms:
  Automatically writes and verifies data at specified address
- Hidden ROM Region:
  64KB with a Factory-serialized secure electronic serial number (ESN), which is accessible through a command sequence
- Data Polling and Toggle Bit:
  Allow for detection of program or erase cycle completion
- Ready-Busy output (RY/$\overline{BY}$): Detection of program or erase cycle completion
- Over 100,000 write/erase cycles
- Low supply voltage (Vccf ≤ 2.5V) inhibits writes
- $\overline{WP}$/ACC input pin:
  If V_{IL}, allows protection of boot sectors
  If V_{IH}, allows removal of boot sector protection
  If Vacc, program time is reduced by 40%
- Boot sector: Top or Bottom

SRAM FEATURES (8 Mb density)

- Power Dissipation:
  Operating: 25 mA maximum
  Standby: 15 µA maximum
- Chip Selects: $\overline{CE1}$s, CE2s
- Power down feature using $\overline{CE1}$s, or CE2s or $\overline{LB}$s & $\overline{UB}$s
- Data retention supply voltage: 1.0 to 3.3 volt
- Byte data control: $\overline{LB}$s (DQ0–DQ7), $\overline{UB}$s (DQ8–DQ15) — on x16 version

GENERAL DESCRIPTION

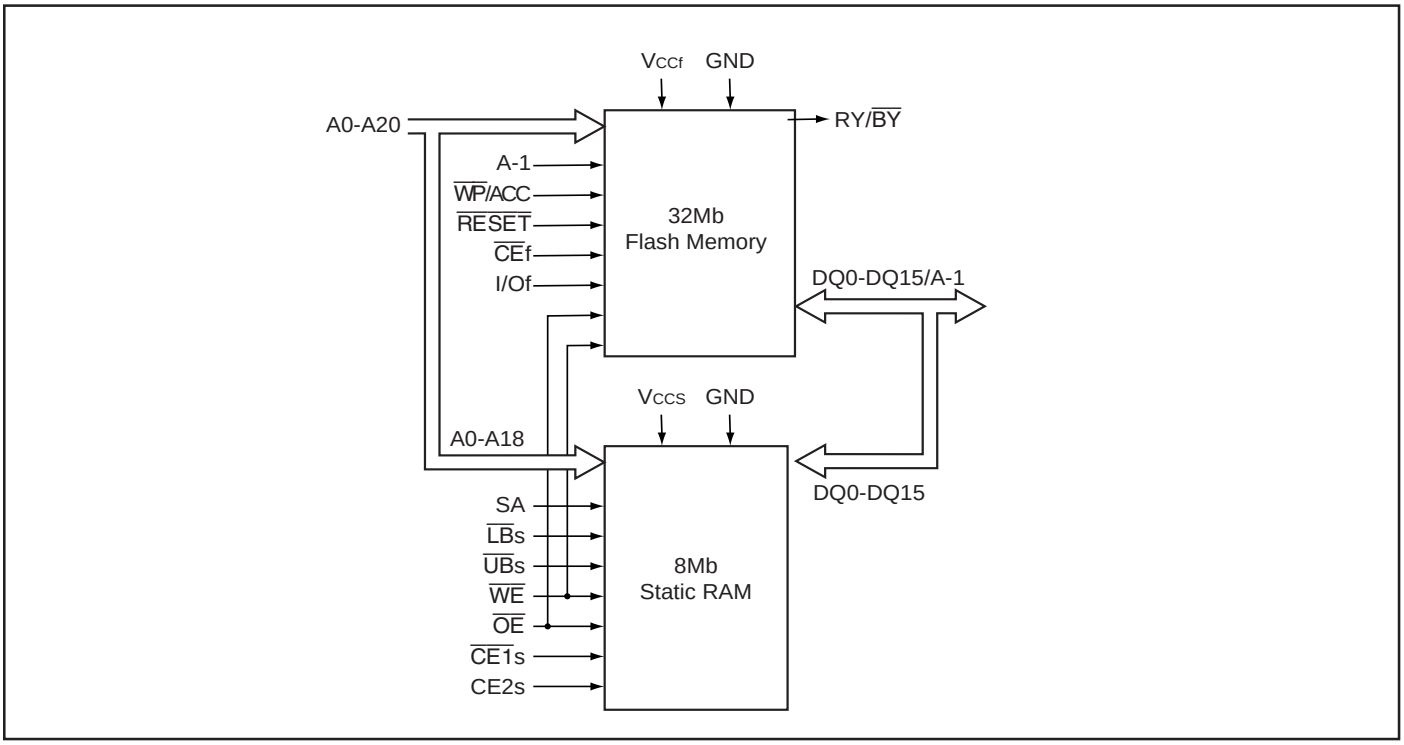
The flash and SRAM MCP is available in 32 Mbit Flash/8 Mbit SRAM having a data bus of either x8 or x16. The 32 Mbit flash is composed of 2,097,152 words of 16 bits or 4,194,304 bytes of 8 bits. Data lines DQ0-DQ7 handle the x8 format, while lines DQ0-DQ15 handle the x16 format.

The package uses a 3.0V power supply for all operations. No other source is required for program and erase operations. The flash can be programmed in system using this 3.0V supply, or can be programmed in a standard EPROM programmer.

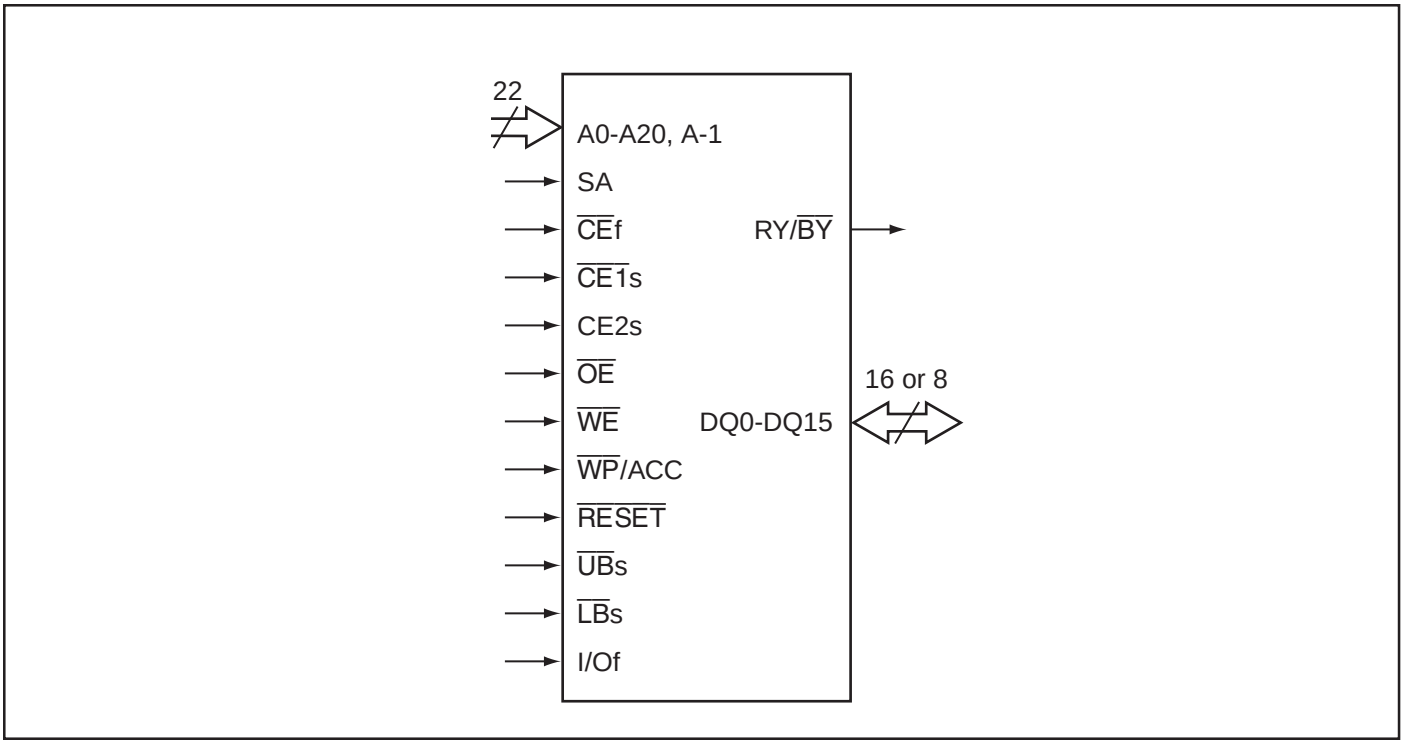
The 32 Mbit flash/8 Mbit SRAM is offered in a 73-pin BGA package. The flash is compatible with the JEDEC Flash command set standard . The flash access time is 70 ns and the SRAM access time is 70ns.

The Flash architecture is composed of two banks which allows simultaneous operation on each. Optimized performance can be achieved by first initializing a program or erase function in one bank, then immediately starting a read from the other bank. Both operations would then be operating simultaneously, with zero latency.

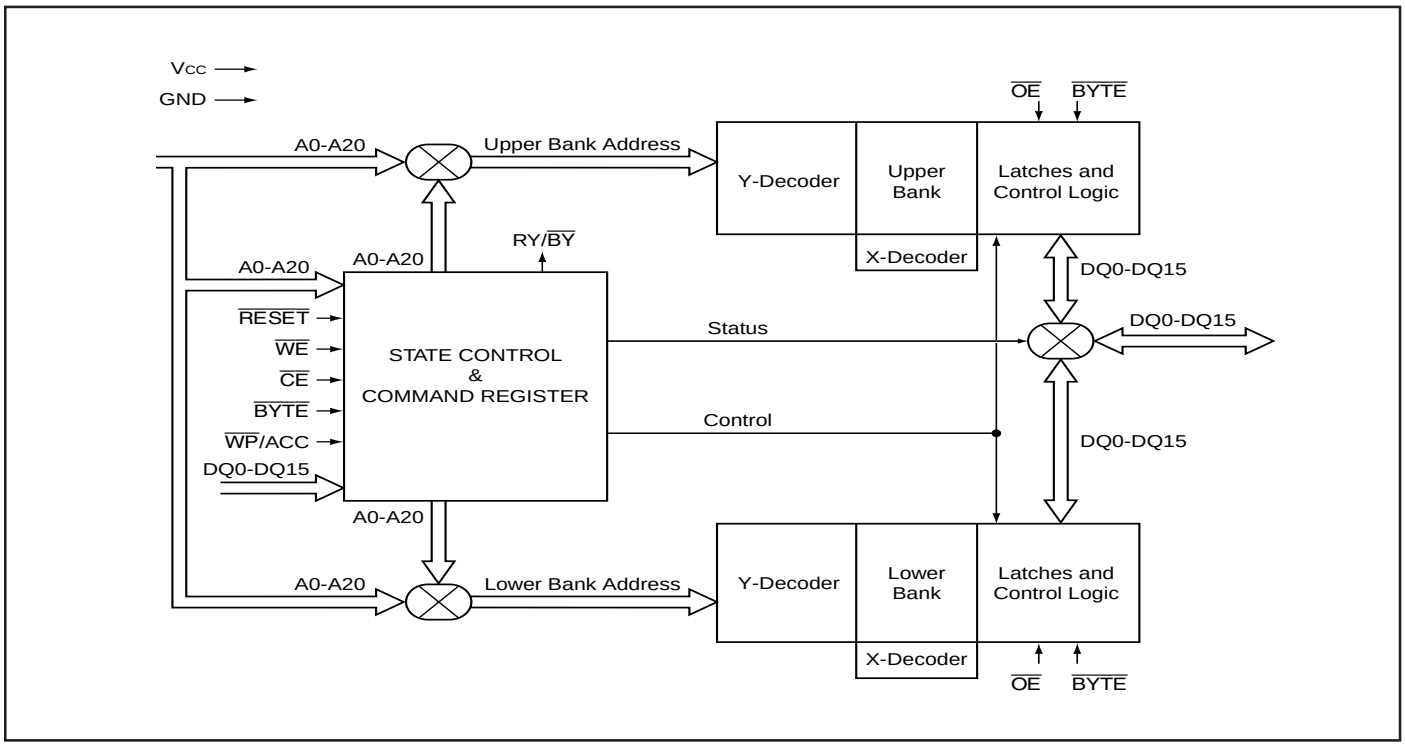
MCP BLOCK DIAGRAM



LOGIC SYMBOL



FLASH MEMORY BLOCK DIAGRAM



PIN CONFIGURATION (32 Mb Flash and 8 Mb SRAM)

73 BALL FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10
A	NC									NC
B	NC				NC	NC				NC
C	NC		A7	$\overline{LB}$	$\overline{WP}$/ACC	$\overline{WE}$	A8	A11		
D		A3	A6	$\overline{UB}$	$\overline{RESET}$	CE2s	A19	A12	A15	
E		A2	A5	A18	RY/$\overline{BY}$	A20	A9	A13	NC	
F	NC	A1	A4	A17			A10	A14	NC	NC
G	NC	A0	GND	DQ1			DQ6	SA	A16	NC
H		$\overline{CE}$f	$\overline{OE}$	DQ9	DQ3	DQ4	DQ13	DQ15/A-1	I/Of	
J		$\overline{CE1}$s	DQ0	DQ10	Vccf	Vccs	DQ12	DQ7	GND	
K			DQ8	DQ2	DQ11	NC	DQ5	DQ14		
L	NC				NC	NC				NC
M	NC									NC

Shared
Flash only
SRAM only

PIN DESCRIPTIONS

A0-A18	Address Inputs, Common
A19-A20, A-1	Address Inputs, Flash
DQ0-DQ15/A-1	Data Inputs/Outputs
$\overline{RESET}$	Reset
$\overline{CE1}$s, CE2s	Chip Selects, SRAM
I/Of	I/O Configuration, Flash
$\overline{CE}$f	Chip Enable Input, Flash
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input

$\overline{LB}$s	Lower-byte Control(DQ0-DQ7), SRAM
$\overline{UB}$s	Upper-byte Control (DQ8-DQ15), SRAM
$\overline{WP}$/ACC	Write Protect/Acceleration Pin, Flash
RY/$\overline{BY}$	Ready/Busy Output
SA	High Order Address Pin, SRAM (x8)
NC	No Connection
Vccf	Power, Flash
Vccs	Power, SRAM
GND	Ground

DEVICE BUS OPERATIONS

User Bus Operations (Flash=Word mode: I/Of = Vccf, SRAM= x16 version)

OPERATION(1,3)	$\overline{CE}$f	$\overline{CE}$1s	CE2s	$\overline{OE}$	$\overline{WE}$	SA(6)	$\overline{LB}$s	$\overline{UB}$s	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$ /ACC(5)	$\overline{WP}$	
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X	
	H	X	L	X	X	X	X	X	High-Z	High-Z	H	X	
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X	
	H	L	H	X	X	X	H	H	High-Z	High-Z	H	X	
	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X	
	L	X	L	H	H	X	X	X	High-Z	High-Z	H	X	
Read from Flash(2)	L	H	X	L	H	X	X	X	DOUT	DOUT	H	X	
	L	X	L	L	H	X	X	X	DOUT	DOUT	H	X	
Write to Flash	L	H	X	H	L	X	X	X	DIN	DIN	H	X	
	L	X	L	H	L	X	X	X	DIN	DIN	H	X	
Read from SRAM	H	L	H	L	H	X	L	L	DOUT	DOUT	H	X	
	H	L	H	L	H	X	H	L	High-Z	DOUT	H	X	
H	L	H	L	H	X	L	H	DOUT	High-Z	H	X		
Write to SRAM	H	L	H	X	L	X	L	L	DIN	DIN	H	X	
H	L	H	X	L	X	H	L	High-Z	DIN	H	X	H	L
H	X	L	X	L	H	DIN	High-Z	H	X				
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	VID	X	
Flash Hardware	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X	Re-
set	X	X	L	X	X	X	X	X	High-Z	High-Z	L	X	
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L	

Notes:

1. Any operations not indicated this column are inhibited.
2. $\overline{WE}$ can be VIL if $\overline{OE}$ is VIL, $\overline{OE}$ at VIH initiates the write operations.
3. Do not apply $\overline{CE}$f = VIL, $\overline{CE}$1s = VIL and CE2s = VIH all at once.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = VIL: protection of boot sectors.
   $\overline{WP}$/ACC = VIH: removal of boot sectors protection.
   $\overline{WP}$/ACC = VACC (9V): Program time will reduce by 40%.
6. SA: Don't care or open.
7. L = VIL, H = VIH, X = VIL or VIH.

DEVICE BUS OPERATIONS

User Bus Operations (Flash=BYTE mode: I/Of = GND, SRAM= x16 version)

OPERATION[1,3]	$\overline{CE}$f	$\overline{CE1}$s	CE2s	DQ_{15}/A-1	$\overline{OE}$	$\overline{WE}$	SA[6]	$\overline{LB}$s	$\overline{UB}$s	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$	WP/ACC[5]
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	A-1	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	A-1	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash[2]	L	H	X	A-1	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	A-1	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	A-1	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	A-1	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	X	L	H	X	L	L	DOUT	DOUT	H	X
	H	L	H	X	L	H	X	H	L	High-Z	DOUT	H	X
	H	L	H	X	L	H	X	L	H	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	X	L	L	DIN	DIN	H	X
	H	L	H	X	X	L	X	H	L	High-Z	DIN	H	X
	H	L	H	X	X	L	X	L	H	DIN	High-Z	H	X
Temporary Sector Group Unprotection[4]	X	X	X	X	X	X	X	X	X	X	X	VID	X
Flash Hardware	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
Reset	X	X	L	X	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Notes:
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5. $\overline{WP}$/ACC = VIL: protection of boot sectors.
   $\overline{WP}$/ACC = VIH: removal of boot sectors protection.
   $\overline{WP}$/ACC = VACC (9V): Program time will reduce by 40%.
6. $\overline{LB}$s, $\overline{UB}$s: Don't care or open.
7. L = VIL, H = VIH, X = VIL or VIH.

DEVICE BUS OPERATIONS

User Bus Operations (Flash=WORD mode: I/Of = Vccf, SRAM= x8 version)

OPERATION[1,3]	$\overline{CE}$f	$\overline{CE}$1s	CE2s	$\overline{OE}$	$\overline{WE}$	SA[6]	$\overline{LB}$s	$\overline{UB}$s	$DQ_{0-}DQ_7$	DQ_8-DQ_{15}	$\overline{RESET}$	$\overline{WP}$ /ACC[5]
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash[2]	L	H	X	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	L	H	SA	X	X	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	DIN	High-Z	H	X
Temporary Sector Group Unprotection[4]	X	X	X	X	X	X	X	X	X	X	VID	X
Flash Hardware	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
Reset	X	X	L	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Notes:
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DEVICE BUS OPERATIONS

User Bus Operations (Flash=Byte mode: I/Of = GND, SRAM= x8 version)

OPERATION[1,3]	$\overline{CE}f$	$\overline{CE1}s$	CE2s	DQ_{15}/A-1		$\overline{OE}$	$\overline{WE}$	SA[6]	$\overline{LB}s$	$\overline{UB}s$	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$	WP/ACC[5]	OP-
Full Standby	H	H	X	X		X	X	X	X	X	High-Z	High-Z	H	X	
	H	X	L	X		X	X	X	X	X	High-Z	High-Z	H	X	
Output Disable	H	L	H	X		H	H	X	X	X	High-Z	High-Z	H	X	
	H	L	H	X		X	X	X	H	H	High-Z	High-Z	H	X	
	L	H	X	A-1		H	H	X	X	X	High-Z	High-Z	H	X	
	L	X	L	A-1		H	H	X	X	X	High-Z	High-Z	H	X	
Read from Flash[2]	L	H	X	A-1		L	H	X	X	X	DOUT	DOUT	H	X	
	L	X	L	A-1		L	H	X	X	X	DOUT	DOUT	H	X	
Write to Flash	L	H	X	A-1		H	L	X	X	X	DIN	DIN	H	X	
	L	X	L	A-1		H	L	X	X	X	DIN	DIN	H	X	
Read from SRAM	H	L	H	X		L	H	SA	X	X	DOUT	High-Z	H	X	
Write to SRAM	H	L	H	X		X	L	SA	X	X	DIN	High-Z	H	X	
Temporary Sector Group Unprotection[4]	X	X	X	X		X	X	X	X	X	X	X	VID	X	
Flash Hardware	X	H	X	X		X	X	X	X	X	High-Z	High-Z	L	X	Re-
set	X	X	L	X		X	X	X	X	X	High-Z	High-Z	L	X	
Boot Block Sector Write Protection	X	X	X	X		X	X	X	X	X	X	X	X	L	

Notes:

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7. L = VIL, H = VIH, X = VIL or VIH.

FLASH - TOP BOOT SECTOR ADDRESS

Type C	Type B	Type A	Sector	Sector Address A20-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank2	Bank2	Bank2	SA0	000000xxx	64/32	000000h–00FFFFh	000000h–07FFFh
Bank2	Bank2	Bank2	SA1	000001xxx	64/32	010000h–01FFFFh	008000h–0FFFFh
Bank2	Bank2	Bank2	SA2	000010xxx	64/32	020000h–02FFFFh	010000h–17FFFh
Bank2	Bank2	Bank2	SA3	000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
Bank2	Bank2	Bank2	SA4	000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
Bank2	Bank2	Bank2	SA5	000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
Bank2	Bank2	Bank2	SA6	000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
Bank2	Bank2	Bank2	SA7	000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
Bank2	Bank2	Bank2	SA8	001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
Bank2	Bank2	Bank2	SA9	001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
Bank2	Bank2	Bank2	SA10	001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
Bank2	Bank2	Bank2	SA11	001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
Bank2	Bank2	Bank2	SA12	001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
Bank2	Bank2	Bank2	SA13	001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
Bank2	Bank2	Bank2	SA14	001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
Bank2	Bank2	Bank2	SA15	001111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
Bank2	Bank2	Bank2	SA16	010000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
Bank2	Bank2	Bank2	SA17	010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
Bank2	Bank2	Bank2	SA18	010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
Bank2	Bank2	Bank2	SA19	010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
Bank2	Bank2	Bank2	SA20	010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
Bank2	Bank2	Bank2	SA21	010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
Bank2	Bank2	Bank2	SA22	010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh
Bank2	Bank2	Bank2	SA23	010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
Bank2	Bank2	Bank2	SA24	011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
Bank2	Bank2	Bank2	SA25	011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
Bank2	Bank2	Bank2	SA26	011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
Bank2	Bank2	Bank2	SA27	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
Bank2	Bank2	Bank2	SA28	011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
Bank2	Bank2	Bank2	SA29	011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh

FLASH - TOP BOOT SECTOR ADDRESS Continued:

Type C	Type B	Type A	Sector	Sector Address A20-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank2	Bank2	Bank2	SA30	011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh
Bank2	Bank2	Bank2	SA31	011111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh
Bank1	Bank2	Bank2	SA32	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
Bank1	Bank2	Bank2	SA33	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
Bank1	Bank2	Bank2	SA34	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
Bank1	Bank2	Bank2	SA35	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
Bank1	Bank2	Bank2	SA36	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
Bank1	Bank2	Bank2	SA37	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
Bank1	Bank2	Bank2	SA38	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
Bank1	Bank2	Bank2	SA39	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
Bank1	Bank2	Bank2	SA40	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
Bank1	Bank2	Bank2	SA41	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
Bank1	Bank2	Bank2	SA42	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
Bank1	Bank2	Bank2	SA43	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
Bank1	Bank2	Bank2	SA44	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
Bank1	Bank2	Bank2	SA45	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
Bank1	Bank2	Bank2	SA46	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
Bank1	Bank2	Bank2	SA47	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
Bank1	Bank1	Bank2	SA48	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
Bank1	Bank1	Bank2	SA49	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
Bank1	Bank1	Bank2	SA50	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
Bank1	Bank1	Bank2	SA51	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
Bank1	Bank1	Bank2	SA52	110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
Bank1	Bank1	Bank2	SA53	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
Bank1	Bank1	Bank2	SA54	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
Bank1	Bank1	Bank2	SA55	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
Bank1	Bank1	Bank1	SA56	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
Bank1	Bank1	Bank1	SA57	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
Bank1	Bank1	Bank1	SA58	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh

FLASH - TOP BOOT SECTOR ADDRESS Continued:

Type C	Type B	Type A	Sector Sector	Sector Address A20-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
Bank1	Bank1	Bank1	SA59	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
Bank1	Bank1	Bank1	SA60	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
Bank1	Bank1	Bank1	SA61	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
Bank1	Bank1	Bank1	SA62	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
Bank1	Bank1	Bank1	SA63	111111000	8/4	3F0000h–3F1FFFh	1F8000h–1F8FFFh
Bank1	Bank1	Bank1	SA64	111111001	8/4	3F2000h–3F3FFFh	1F9000h–1F9FFFh
Bank1	Bank1	Bank1	SA65	111111010	8/4	3F4000h–3F5FFFh	1FA000h–1FAFFFh
Bank1	Bank1	Bank1	SA66	111111011	8/4	3F6000h–3F7FFFh	1FB000h–1FBFFFh
Bank1	Bank1	Bank1	SA67	111111100	8/4	3F8000h–3F9FFFh	1FC000h–1FCFFFh
Bank1	Bank1	Bank1	SA68	111111101	8/4	3FA000h–3FBFFFh	1FD000h–1FDFFFh
Bank1	Bank1	Bank1	SA69	111111110	8/4	3FC000h–3FDFFFh	1FE000h–1FEFFFh
Bank1	Bank1	Bank1	SA70	111111111	8/4	3FE000h–3FFFFFh	1FF000h–1FFFFFh

Note:
The address range is A20:A-1 in byte mode (I/Of=V IL) or A20:A0 in word mode (I/Of=V IH). The bank address bits are A20–A18 for Type A, A20 and A19 for Type B, and A20 for Type C.

FLASH - TOP BOOT SECURITY SECTOR ADDRESSES

Device			Sector Address A20-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
TypeC	Type B	Type A	111111xxx	256/128	3FE000h-3FE0FFh	1FF000h-1FF07Fh

FLASH - BOTTOM BOOT SECTOR ADDRESS

Type F	Type E	TypeD	Sector	Sector Address A20-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
Bank1	Bank1	Bank1	SA0	000000000	8/4	000000h–001FFFh	000000h–000FFFh
Bank1	Bank1	Bank1	SA1	000000001	8/4	002000h–003FFFh	001000h–001FFFh
Bank1	Bank1	Bank1	SA2	000000010	8/4	004000h–005FFFh	002000h–002FFFh
Bank1	Bank1	Bank1	SA3	000000011	8/4	006000h–007FFFh	003000h–003FFFh
Bank1	Bank1	Bank1	SA4	000000100	8/4	008000h–009FFFh	004000h–004FFFh
Bank1	Bank1	Bank1	SA5	000000101	8/4	00A000h–00BFFFh	005000h–005FFFh
Bank1	Bank1	Bank1	SA6	000000110	8/4	00C000h–00DFFFh	006000h–006FFFh
Bank1	Bank1	Bank1	SA7	000000111	8/4	00E000h–00FFFFh	007000h–007FFFh
Bank1	Bank1	Bank1	SA8	000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh
Bank1	Bank1	Bank1	SA9	000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh
Bank1	Bank1	Bank1	SA10	000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
Bank1	Bank1	Bank1	SA11	000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
Bank1	Bank1	Bank1	SA12	000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
Bank1	Bank1	Bank1	SA13	000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
Bank1	Bank1	Bank1	SA14	000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
Bank1	Bank1	Bank2	SA15	001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
Bank1	Bank1	Bank2	SA16	001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
Bank1	Bank1	Bank2	SA17	001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
Bank1	Bank1	Bank2	SA18	001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
Bank1	Bank1	Bank2	SA19	001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
Bank1	Bank1	Bank2	SA20	001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
Bank1	Bank1	Bank2	SA21	001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
Bank1	Bank1	Bank2	SA22	001111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
Bank1	Bank2	Bank2	SA23	010000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
Bank1	Bank2	Bank2	SA24	010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
Bank1	Bank2	Bank2	SA25	010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
Bank1	Bank2	Bank2	SA26	010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
Bank1	Bank2	Bank2	SA27	010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
Bank1	Bank2	Bank2	SA28	010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
Bank1	Bank2	Bank2	SA29	010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh

FLASH - BOTTOM BOOT SECTOR ADDRESS Continued:

Type F	Type E	Type D	Sector	Sector Address A20-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
Bank1	Bank2	Bank2	SA30	010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
Bank1	Bank2	Bank2	SA31	011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
Bank1	Bank2	Bank2	SA32	011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
Bank1	Bank2	Bank2	SA33	011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
Bank1	Bank2	Bank2	SA34	011011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh
Bank1	Bank2	Bank2	SA35	011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
Bank1	Bank2	Bank2	SA36	011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
Bank1	Bank2	Bank2	SA37	011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh
Bank1	Bank2	Bank2	SA38	011111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh
Bank2	Bank2	Bank2	SA39	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
Bank2	Bank2	Bank2	SA40	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
Bank2	Bank2	Bank2	SA41	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
Bank2	Bank2	Bank2	SA42	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
Bank2	Bank2	Bank2	SA43	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
Bank2	Bank2	Bank2	SA44	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
Bank2	Bank2	Bank2	SA45	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
Bank2	Bank2	Bank2	SA46	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
Bank2	Bank2	Bank2	SA47	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
Bank2	Bank2	Bank2	SA48	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
Bank2	Bank2	Bank2	SA49	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
Bank2	Bank2	Bank2	SA50	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
Bank2	Bank2	Bank2	SA51	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
Bank2	Bank2	Bank2	SA52	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
Bank2	Bank2	Bank2	SA53	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
Bank2	Bank2	Bank2	SA54	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
Bank2	Bank2	Bank2	SA55	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
Bank2	Bank2	Bank2	SA56	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
Bank2	Bank2	Bank2	SA57	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
Bank2	Bank2	Bank2	SA58	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh

FLASH - BOTTOM BOOT SECTOR ADDRESS Continued:

Type F	Type E	Type D	Sector	Sector Address A20-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
Bank2	Bank2	Bank2	SA59	110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
Bank2	Bank2	Bank2	SA60	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
Bank2	Bank2	Bank2	SA61	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
Bank2	Bank2	Bank2	SA62	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
Bank2	Bank2	Bank2	SA63	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
Bank2	Bank2	Bank2	SA64	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
Bank2	Bank2	Bank2	SA65	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
Bank2	Bank2	Bank2	SA66	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
Bank2	Bank2	Bank2	SA67	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
Bank2	Bank2	Bank2	SA68	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
Bank2	Bank2	Bank2	SA69	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
Bank2	Bank2	Bank2	SA70	111111xxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh

Note:
The address range is A20:A-1 in byte mode (I/Of=V IL) or A20:A0 in word mode (I/Of=V IH). The bank address bits are A20–A18 for Type D, A20 and A19 for Type E, and A20 for Type F.

FLASH - Bottom BOOT SECURITY SECTOR ADDRESSES

Device			Sector Address A20-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
Type F	Type E	Type D	000000xxx	256/128	000000h-0000FFh	00000h-0007Fh

SECTOR GROUP ADDRESS (TYPE A, TYPE B, TYPE C)

(Top Boot Block)

Sector Group	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	0 1 1	1 0 1	X	X	X	SA1 to SA3
SGA2	0	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	0	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	0	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	0	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	0	1	1	1	X	X	X	X	X	SA28 to SA31
SGA9	1	0	0	0	X	X	X	X	X	SA32 to SA35
SGA10	1	0	0	1	X	X	X	X	X	SA36 to SA39
SGA11	1	0	1	0	X	X	X	X	X	SA40 to SA43
SGA12	1	0	1	1	X	X	X	X	X	SA44 to SA47
SGA13	1	1	0	0	X	X	X	X	X	SA48 to SA51
SGA14	1	1	0	1	X	X	X	X	X	SA52 to SA55
SGA15	1	1	1	0	X	X	X	X	X	SA56 to SA59
SGA16	1	1	1	1	0 0 1	0 1 0	X	X	X	SA60 to SA62
SGA17	1	1	1	1	1	1	0	0	0	SA63
SGA18	1	1	1	1	1	1	0	0	1	SA64
SGA19	1	1	1	1	1	1	0	1	0	SA65
SGA20	1	1	1	1	1	1	0	1	1	SA66
SGA21	1	1	1	1	1	1	1	0	0	SA67
SGA22	1	1	1	1	1	1	1	0	1	SA68
SGA23	1	1	1	1	1	1	1	1	0	SA69
SGA24	1	1	1	1	1	1	1	1	1	SA70

SECTOR GROUP ADDRESS (TYPE D, TYPE E, TYPE F)

(Bottom Boot Block)

Sector Group	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0 1 1	1 0 1	X	X	X	SA8 to SA10
SGA9	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	1	1	1	1	0 0 1	0 1 0	X	X	X	SA67 to SA69
SGA24	1	1	1	1	1	1	X	X	X	SA70

Flash Memory Autoselect Codes

Type		A_{12} to A_{19}	A_6	A_1	A_0	$A_{-1(1)}$	Code (HEX)
Manufacturer's Code		X	VIL	VIL	VIL	VIL	04h
TYPE A	Byte	X	VIL	VIL	VIH	VIL	55h
	Word	X	VIL	VIL	VIH	X	2255h
TYPE D	Byte	X	VIL	VIL	VIH	VIL	56h
	Word	X	VIL	VIL	VIH	X	2256h
TYPE B	Byte	X	VIL	VIL	VIH	VIL	50h
	Word	X	VIL	VIL	VIH	X	2250h
TYPE E	Byte	X	VIL	VIL	VIH	VIL	53h
	Word	X	VIL	VIL	VIH	X	2253h
TYPE C	Byte	X	VIL	VIL	VIH	VIL	5Ch
	Word	X	VIL	VIL	VIH	X	225Ch
TYPE F	Byte	X	VIL	VIL	VIH	VIL	5Fh
	Word	X	VIL	VIL	VIH	X	225Fh
Sector Group Protect		Sector Group Address	VIL	VIH	VIL	VIL	01h(1)

Note:
1. A–1 is used for Byte mode.
2. Output 01h at protected sector address and output 00h at unprotected sector address.

FLASH MEMORY COMMAND DEFINITIONS

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset *1		1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset *1	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
	Byte		AAAh		555h		(BA) AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Sector Erase Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Sector Erase Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program *2	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte													
Reset from Fast Mode *2	Word	2	BA	90h	XXXh	F0h *6	—	—	—	—	—	—	—	—
	Byte													
Extended Sector Group Protection *3	Word	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
	Byte													
Query *4	Word	1	55h	98h	—	—	—	—	—	—	—	—	—	—
	Byte		AAh											
Hi-ROM Entry	Word	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Hi-ROM Program *5	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Hi-ROM Erase *5	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	HRA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Hi-ROM Exit *5	Word	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—
	Byte		AAAh		555h		(HRBA) AAAh							

Note:

*1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
*2: This command is valid during Fast Mode.
*3: This command is valid while RESET=VID.
*4: The valid Address is A0 to A6.
*5: This command is valid during Hi-ROM mode.
*6: The data "00h" is also acceptable.

Address bits A11 to A19 = X = “H” or “L” for all address commands except for Program Address (PA), Sector Address (SA),and Bank Address (BA).

Bus operations are defined in “Device Bus Operations”.
RA = Address of the memory location to be read
PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased. The combination of A19 , A18 , A17 , A16 , A15 , A14 , A13 , and A12 will uniquely
select any sector.
BA = Bank address (A15 to A20)
SPA = Sector group address to be protected. Set sector group
address (SGA) and (A6 , A1 , A0) = (0, 1, 0).

HRA= Address of the Hidden-ROM area
Type H, Type J, Type K, Type L (Top Boot Type)
Word mode: 0F8000h to 0FFFFFh
Byte mode: 1F0000h to 1FFFFFh

Type M, Type N, Type P, Type Q (Bottom Boot Type)
Word mode: 000000h to 007FFFh
Byte mode: 000000h to 00FFFFh
HRBA = Bank address of the Hidden-ROM area
Type H, Type J, Type K, Type L (Top Boot Type) :
A15 = A16 = A17 = A18 = A19 = 1
Type M, Type N, Type P, Type Q (Bottom Boot Type) :
A15 = A16 = A17 = A18 = A19 = 0

RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA.
SD = Sector protection verify data. Output 01h at protected sector addresses and output 00h at unprotected sector addresses.

The system should generate the following address patterns;
Word mode : 555h or 2AAh to addresses A0 to A10
Byte mode : AAAh or 555h to addresses A–1 and A0 to A10

MCP ABSOLUTE MAXIMUM RATINGS(1,2,3)

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for Data, Address and Control Pins	–0.3 to $V_{CC}f$ + 0.3 -0.2 to $V_{CC}s$ + 0.3	V V
V_{IN}	$\overline{RESET}$(5)	-0.5 to +13.0	V
V_{IN}	$\overline{WP}$/ACC(6)	-0.5 to +10.5	V
$V_{CC}f$/$V_{CC}s$	Voltage on Vcc Supply Relatiive to GND(4)	–0.3 to 3.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.
4. Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot VSS to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$+0.3 V or $V_{CC}s$+0.3 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$+2.0 V or $V_{CC}s$+2.0 V for periods of up to 20 ns.
5. Minimum DC input voltage on RESET pin is –0.5 V. During voltage transitions, RESET pin may undershoot VSS to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-$V_{CC}f$ or $V_{CC}s$) does not exceed 9.0 V. Maximum DC input voltage on RESET pin is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
6. Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0V for periods of up to 20 ns, when $V_{CC}f$ is applied.

MCP OPERATING RANGE

Range	Ambient Temperature	V_{CCF},V_{CCS}
Industrial	–40°C to +85°C	2.7–3.3V

Standard Voltage Range: V_{CC} = 2.7-3.3 V

	Flash Memory		SRAM	Units
Max Access Time	70	85	70	ns
$\overline{CE}$ Access	70	85	70	ns
$\overline{OE}$ Access	30	40	35	ns

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	14	pF
$C_{IN}2$	Input Capacitance	V_{IN} = 0V	12	16	pF
$C_{IN}3$	Input Capacitance	V_{IN} = 0V	14	16	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	21.5	26	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz

FLASH DC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.		Max.	Unit
I_{LI}	Input Leakage	V_{IN}=Vss to Vccf, Vccs		-1.0		1.0	µA
I_{LO}	Output Leakage	V_{OUT}=Vss to Vccf, Vccs		-1.0		1.0	µA
I_{LIT}	$\overline{RESET}$ Inputs Leakage Current	Vccf=Vccf max., Vccs=Vccs max. $\overline{RESET}$ = 12.5V		—		35	µA
I_{LIA}	ACC Inputs Leakage Current	Vccf=Vccf max., Vccs=Vccs max. $\overline{WP}$/ACC = Vacc max.		—		20	µA
$I_{CC}1f$	FLASH Vcc [1] Active Current (Read)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	tCycle = 5Mhz Byte	—		16	mA
			tCycle = 5Mhz Word	—		18	
			tCycle = 1Mhz Byte	—		7	
			tCycle = 1Mhz Word	—		7	
$I_{CC}2f$	FLASH Vcc Active[2] Current(Program/Erase)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}		—		35	mA
$I_{CC}3f$	FLASH Vcc Active[2] Current (Read-While-Program)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	Byte	—		51	mA
			Word			53	
$I_{CC}4f$	FLASH Vcc Active[5] Current (Read-While-Erase)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	Byte	—		51	mA
			Word			53	
$I_{CC}5f$	FLASH Vcc Active[5] Current (Read-While-Erase)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}		—		35	mA
$I_{SB}1f$	FLASH Vcc Standby Current	Vccf = Vcc max, $\overline{CE}$f= Vccf = ± 0.3V $\overline{RESET}$, $\overline{CE}$f, $\overline{WP}$/ACC = Vccf = ± 0.3V		—	1	5	µA
$I_{SB}2f$	FLASH Vcc Standby Current ($\overline{RESET}$)	Vccf = Vcc max, $\overline{RESET}$= Vss = ± 0.3V $\overline{WP}$/ACC = Vccf = ± 0.3V		—	1	5	µA
$I_{SB}3f$	FLASH Vcc[3] Standby Current	Vccf = Vcc max. $\overline{CE}$f, = Vss = ± 0.3V $\overline{RESET}$, $\overline{WP}$/ACC = Vccf = ± 0.3V (Auto Sleep Mode)V_{IN} = Vccf ± 0.3V or Vss ± 0.3V		—	1	5	µA

FLASH DC CHARACTERISTICS Continued:

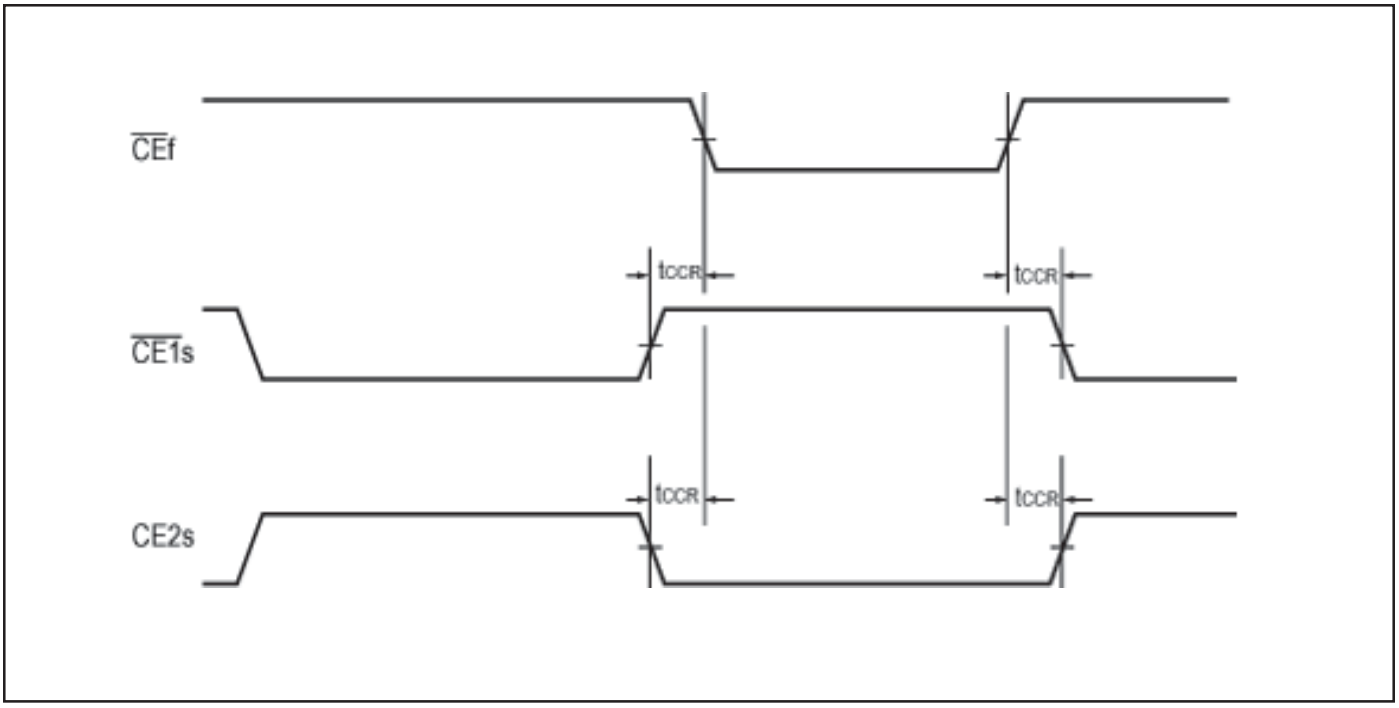
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Level		-0.2	0.5	V
V_{IH}	Input High Level		2.4	$V_{CC} \pm 0.3$(6)	V
V_{ID}	Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$)(4)		11.5	12.5	V
V_{ACC}	Voltage for Program Acceleration ($\overline{WP}$/ACC)(4)		8.5	9.5	V
V_{OL}	Output Low Level	V_{CCf} = V_{CCf} min., V_{CCS}=V_{CCS} min. I_{OL} = 1.0mA	—	0.4	V
V_{OH}	Output High Level	V_{CCf} = V_{CCf} min., V_{CCS}=V_{CCS} min. I_{OL} = 1.0mA	2.4	—	V
V_{LKO}	Flash Low Vccf		2.3	2.5	V

Notes:
1. The ICC current listed includes both the DC operating current and the frequency dependent component.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
4. Applicable for only V_{CCf} applying.
5. Embedded Algorithm (program or erase) is in progress. (@5 MHz)
6. V_{CC} indicates lower of V_{CCf} or V_{CCS}.

AC Characteristics - CE Timing

Parameter	Symbol JEDEC	Standard	Value Test Setup	Min	Unit
$\overline{CE}$ Recover Time	_	t_{CCR}	_	0	ns

Timing Diagram for Alternating SRAM to Flash



FLASH READ ONLY SWITCHING CHARACTERISTICS

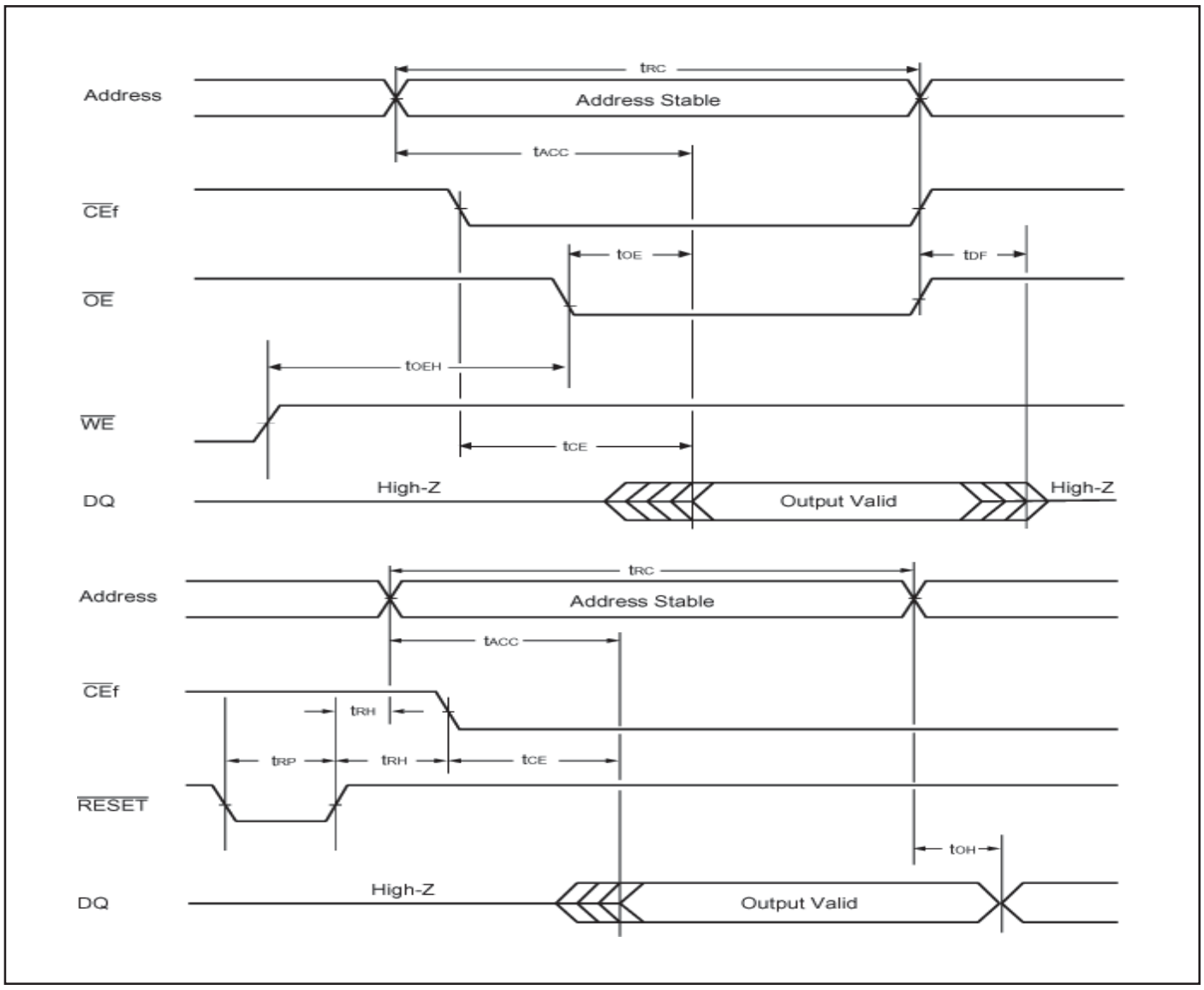
(Over Operating Range)

Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{KC}	Cycle Time	70		85	—	ns
t_{ACC}	Address to Output Delay	—	70	—	85	ns
t_{CE}	Chip Enable to Output Delay	—	70	—	85	ns
t_{OE}	Output Enable to Output Delay	—	30	—	35	ns
t_{DF}	Chip Enable to Output High-Z	—	30	—	30	ns
t_{DF}	Output Enable to Output High-Z	—	30	—	30	ns
t_{OH}	Output Hold Time from Addresses, $\overline{CE}$f or $\overline{OE}$, Whichever Occurs First	0	—	0	—	ns
t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	20	—	20	µs

FLASH AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	1 TTL gate and 30pF

FLASH READ CYCLE



FLASH Erase/Program Operation Characteristics (Over Operating Range)

Symbol	Parameter	-70 ns Min.	-70 ns Max.	-85ns Min.	-85ns Max.	Unit
t_{WC}	Write Cycle Time	70	-	85	-	ns
t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)	0	-	0	-	ns
t_{ASO}	Address Setup Time to $\overline{CE}$f Low During Toggle Bit Polling	15	-	15	-	ns
t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)	45	-	45	-	ns
t_{AHT}	Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling	0	-	0	-	ns
t_{DS}	Data Setup Time	35	-	45	-	ns
t_{DH}	Data Hold Time	0	-	0	-	ns
t_{OES}	Output Enable Setup Time	0	-	0	-	ns
t_{OEH}	Output Enable Hold Time Read	0	-	0	-	ns
t_{OEH}	Output Enable Hold Time Toggle and $\overline{Data}$ Polling	10	-	10	-	ns
t_{CEPH}	$\overline{CE}$f High During Toggle Bit Polling	20	-	20	-	ns
t_{OEPH}	$\overline{OE}$ High During Toggle Bit Polling	20	-	20	-	ns
t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)	0	-	0	-	ns
t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)	0	-	0	-	ns
t_{WS}	WE Setup Time (CEf to WE)	0	-	0	-	ns
t_{CS}	$\overline{CE}$f Setup Time (WE to CEf)	0	-	0	-	ns
t_{WH}	$\overline{WE}$ Hold Time (CEf to WE)	0	-	0	-	ns
t_{CH}	$\overline{CE}$f Hold Time (WE to CEf)	0	-	0	-	ns
t_{WP}	Write Pulse Width	30	-	35	-	ns
t_{CP}	$\overline{CE}$f Pulse Width	30	-	35	-	ns
t_{WPH}	Write Pulse Width High	30	-	30	-	ns
t_{CPH}	$\overline{CE}$f Pulse Width High	30	-	30	-	ns
t_{WHWH1}	Byte Programming Operation	-	12	-	15	µs
t_{WHWH1}	Word Programming Operation	-	15	-	20	µs
t_{WHWH2}	Sector Erase Operation (1)	-	0.7	-	1	s
t_{VCS}	V_{CC}f Setup Time	50	-	50	-	µs

Note:
1. This does not include the preprogramming time.

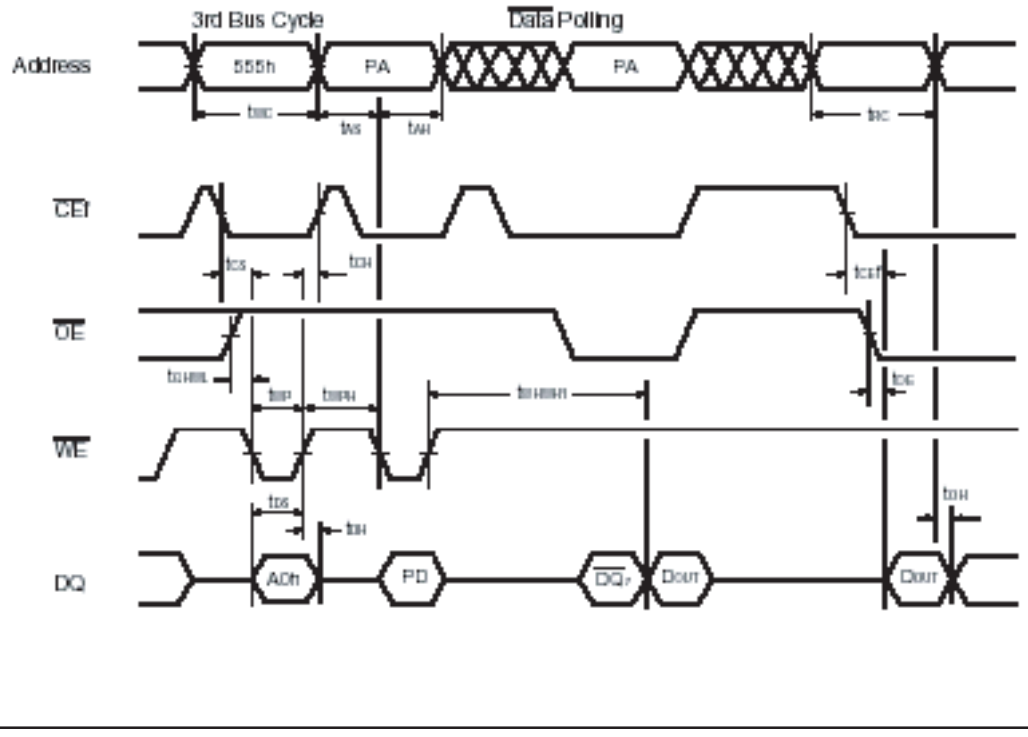
FLASH Erase/Program Operation Characteristics Continued (Over Operating Range)

Symbol	Parameter	-70 ns Min.	-70 ns Max.	-85ns Min.	-85ns Max.	Unit
t_{VLHT}	Voltage Transition Time(2)	4	-	4	-	µs
t_{VIDR}	Rise Time to V_{ID}(2)	500	-	500	-	ns
t_{VACCA}	Rise Time to V_{ACC}	500	-	500	-	ns
t_{RB}	Recovery Time from RY/$\overline{BY}$	0	-	0	-	ns
t_{RP}	$\overline{RESET}$ Pulse Width	500	-	500	-	ns
t_{EOE}	Delay Time from Embedded Output Enable	-	70	-	85	ns
t_{RH}	$\overline{RESET}$ High Level Period Before Read	100	-	200	-	ns
t_{BUSY}	Program/Erase Valid to RY/B$\overline{Y}$ Delay	-	75	-	90	ns
t_{TOW}	Erase Time-out Time (3)	50	-	50	-	µs
t_{SPD}	Erase Suspend Transition Time (4)	-	20	-	20	µs

Note:

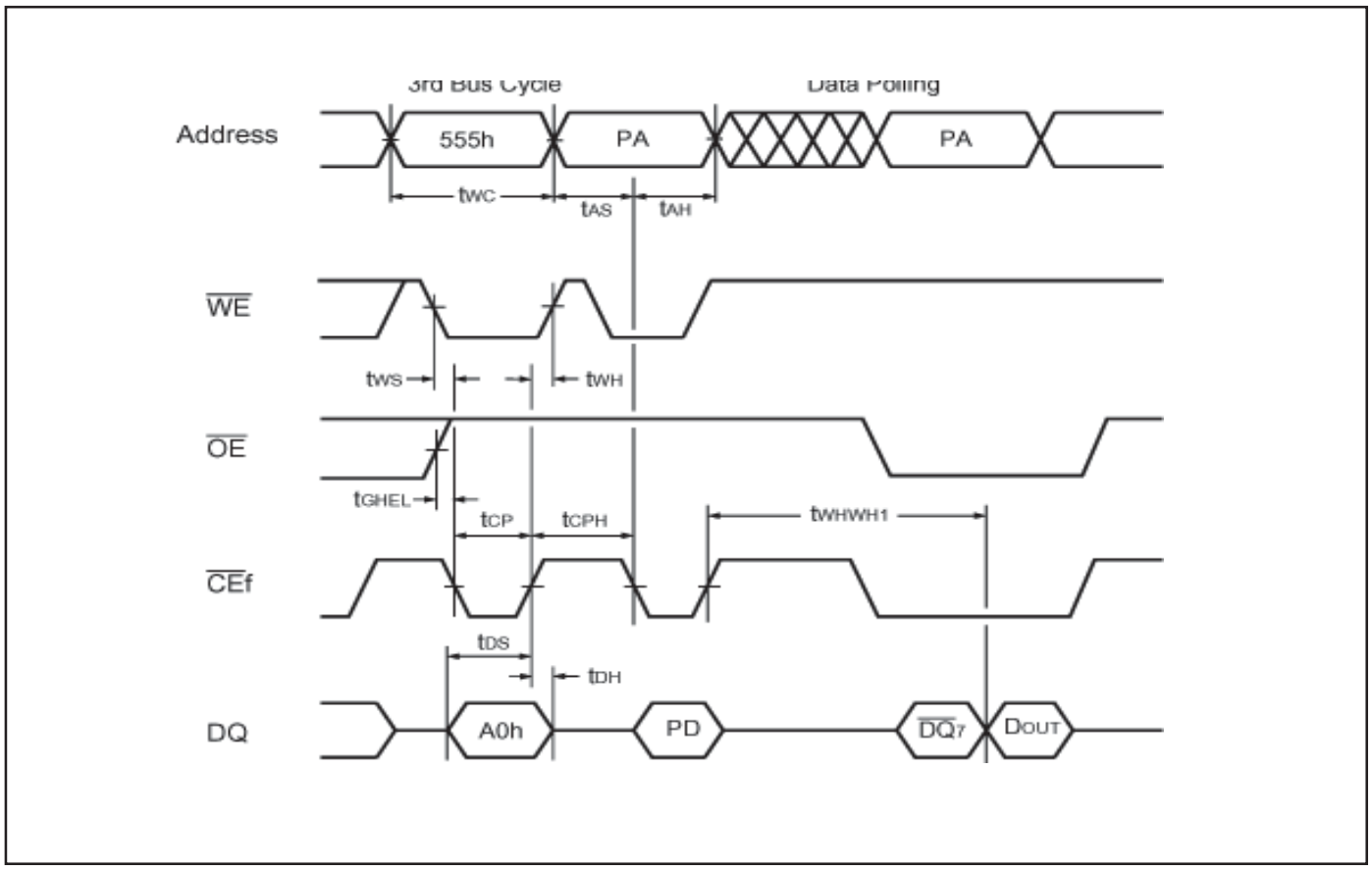
2. This timing is for Sector Protection Operation.
3. The time between writes must be less than “tTOW ” otherwise that command will not be accepted and erasure will start. A time-out or “tTOW ” from the rising edge of last $\overline{CE}$f or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s).
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “tSPD ” to suspend the erase operation.

Flash Write Cycle (WE Control)



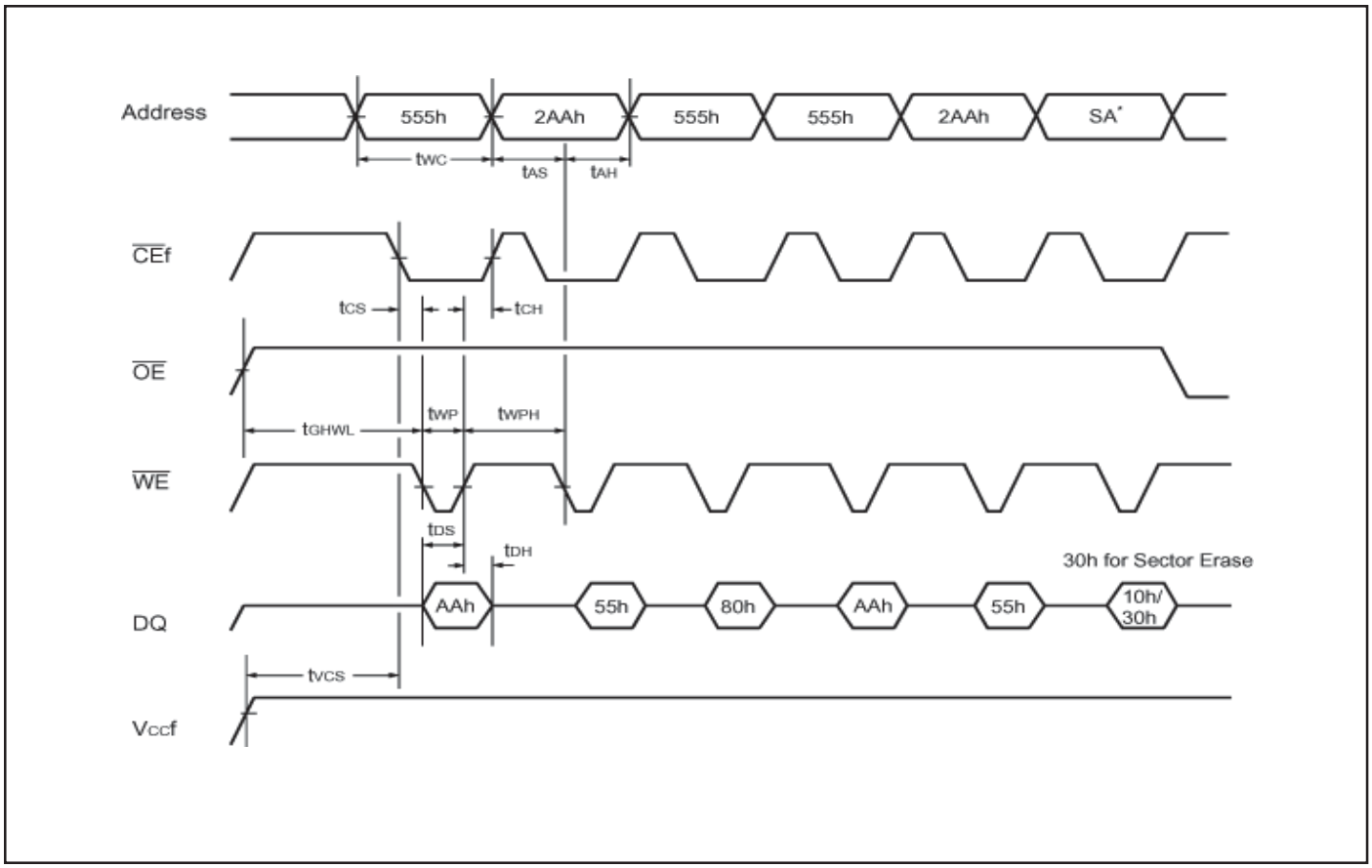
Notes:
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode (the addresses differ from ×8 mode).

Flash Write Cycle (CEf control)



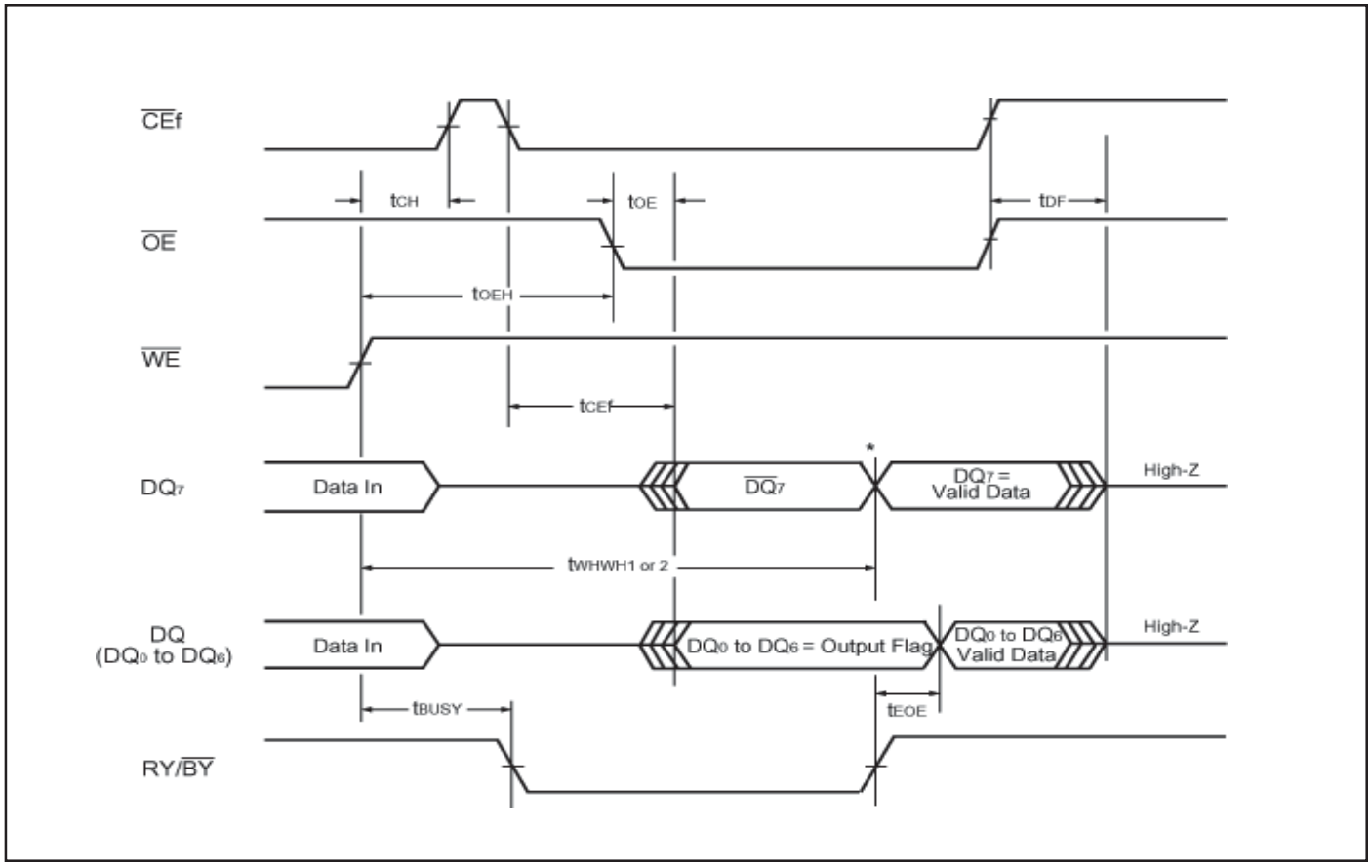
Notes:
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode (the addresses differ from ×8 mode).

FLASH AC Waveforms Chip/Sector Erase Operations



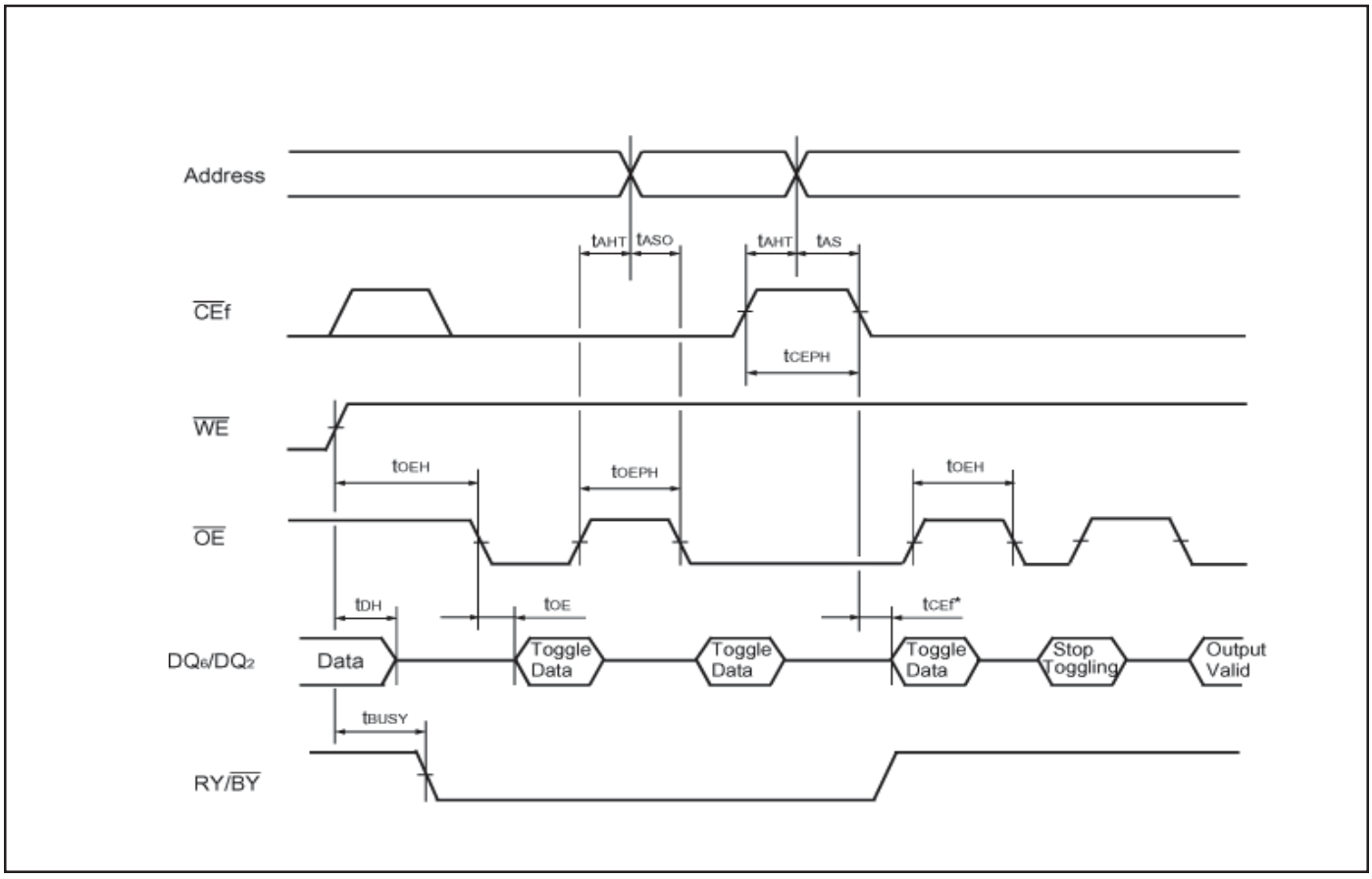
*SA is the sector address for Sector Erase. Address = 555h for Chip Erase.
Note: These waveforms are for the ×16 mode (the addresses differ from ×8 mode).

Flash AC Waveforms
for Data Poling during Embedded Alogrithm Operations



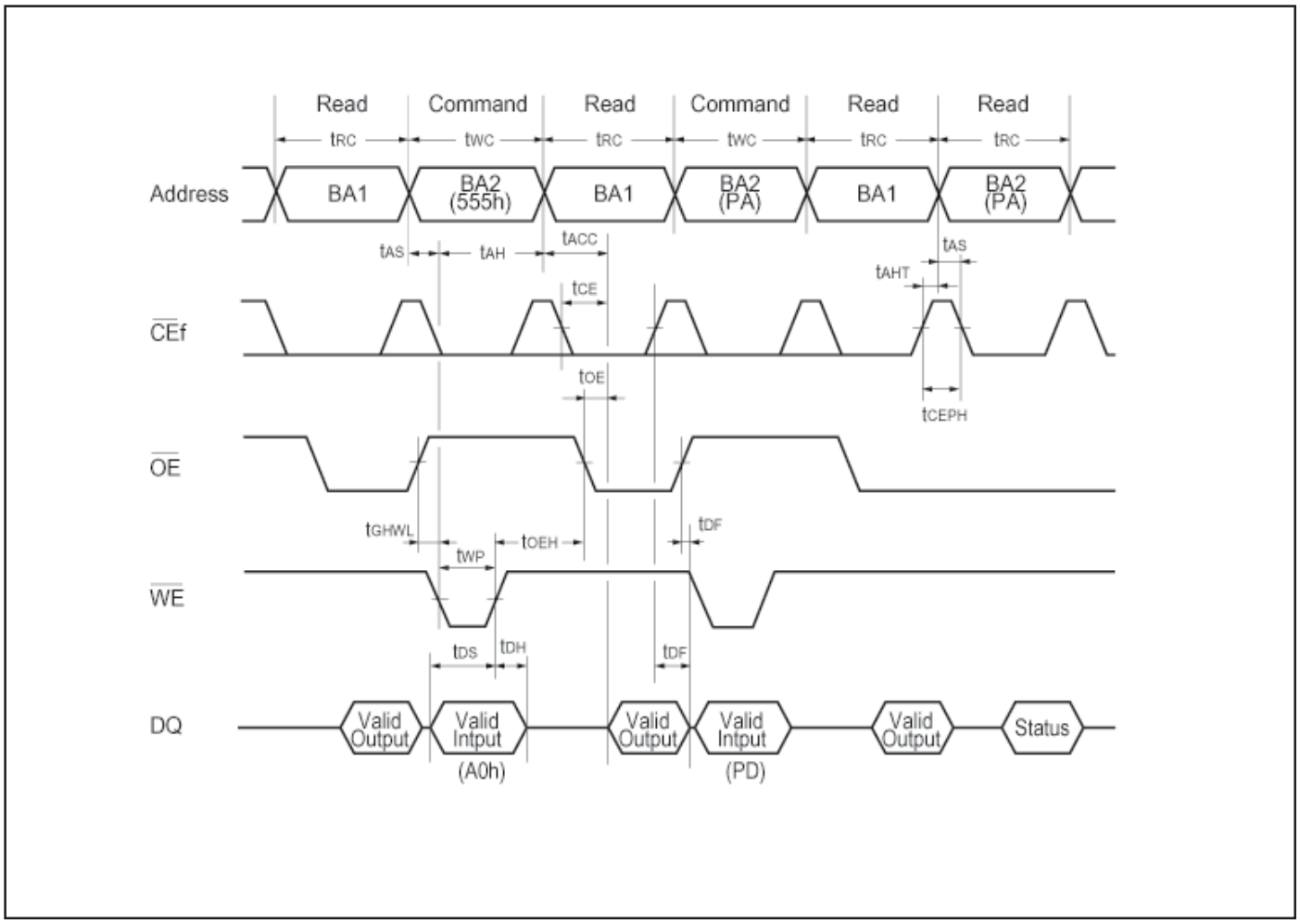
*DQ7 = Valid Data (the device has completed the Embedded operation.)

Flash AC Waveforms for Toggle Bit during Embedded Algorithm Operations



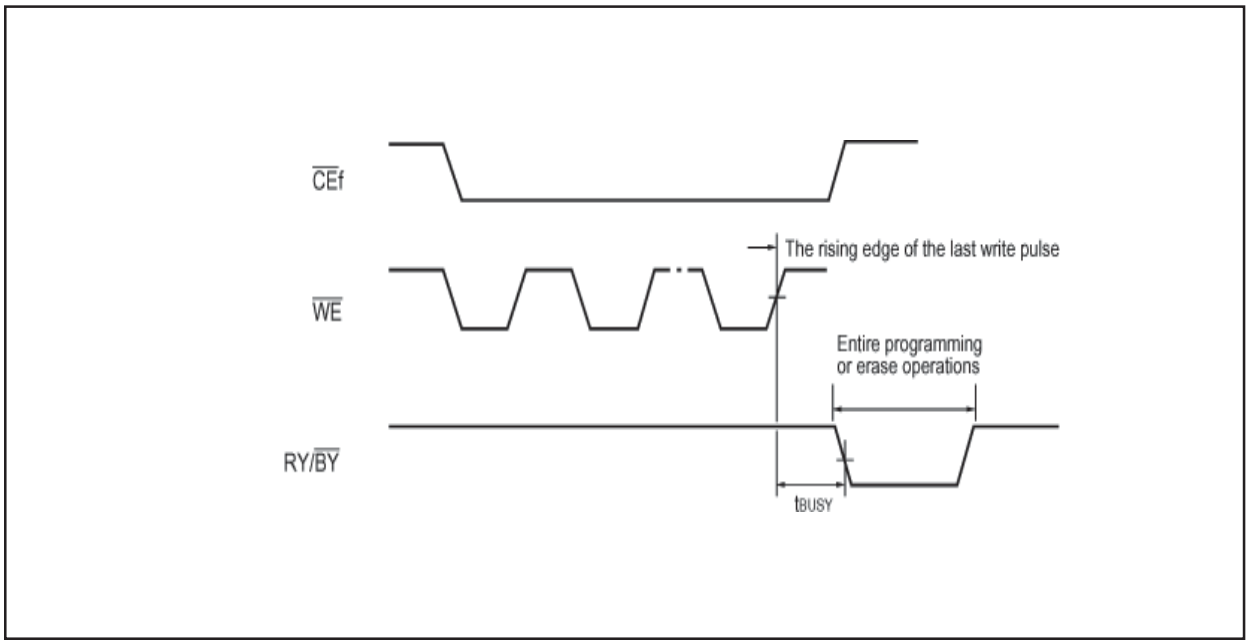
* DQ6 stops toggling (the device has completed the Embedded operation).

Flash Back-to-back Read/Write Timing Diagram

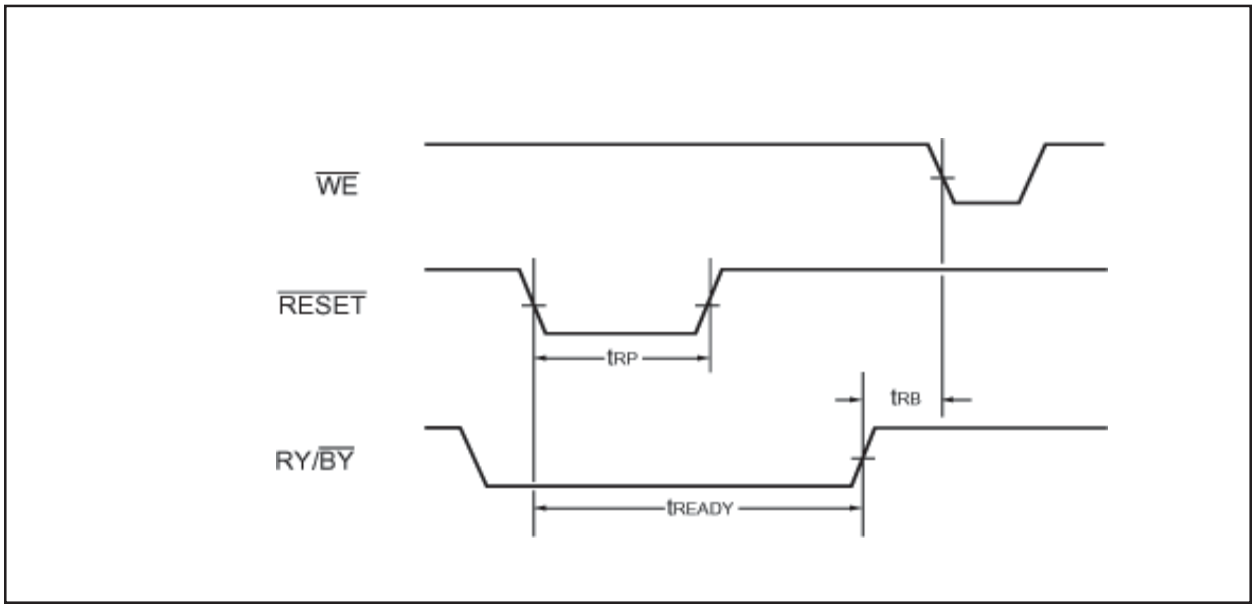


Note: This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

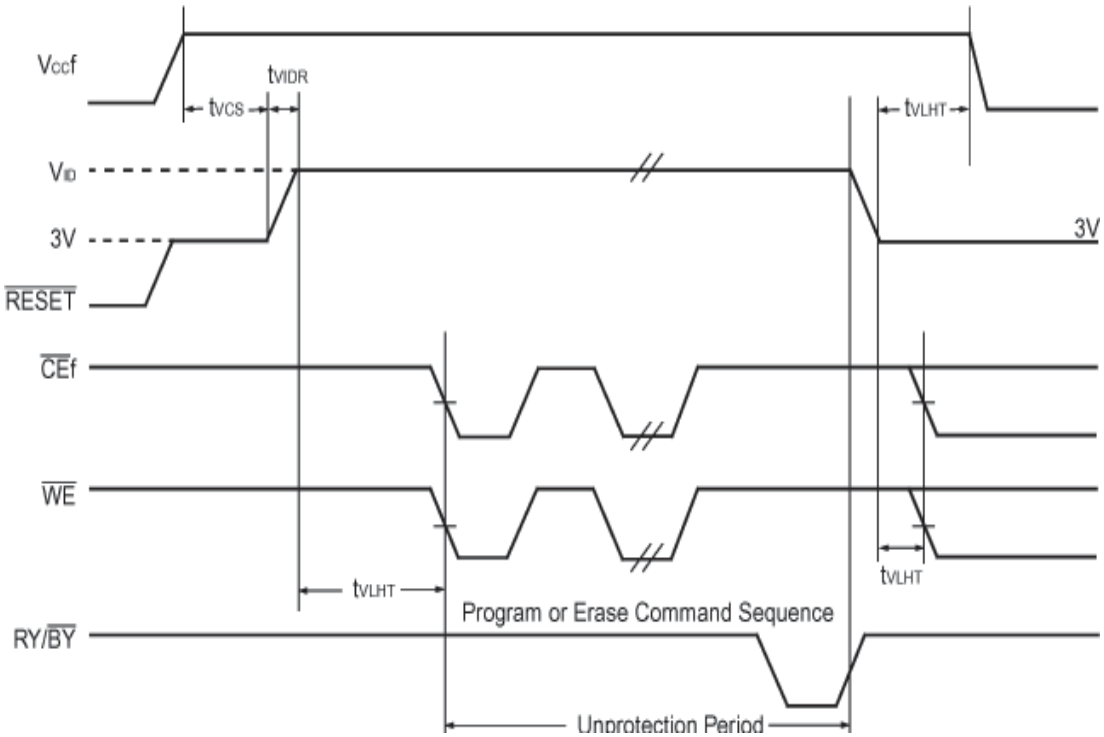
Flash RY/BY Timing Diagram during Write/Erase Operations



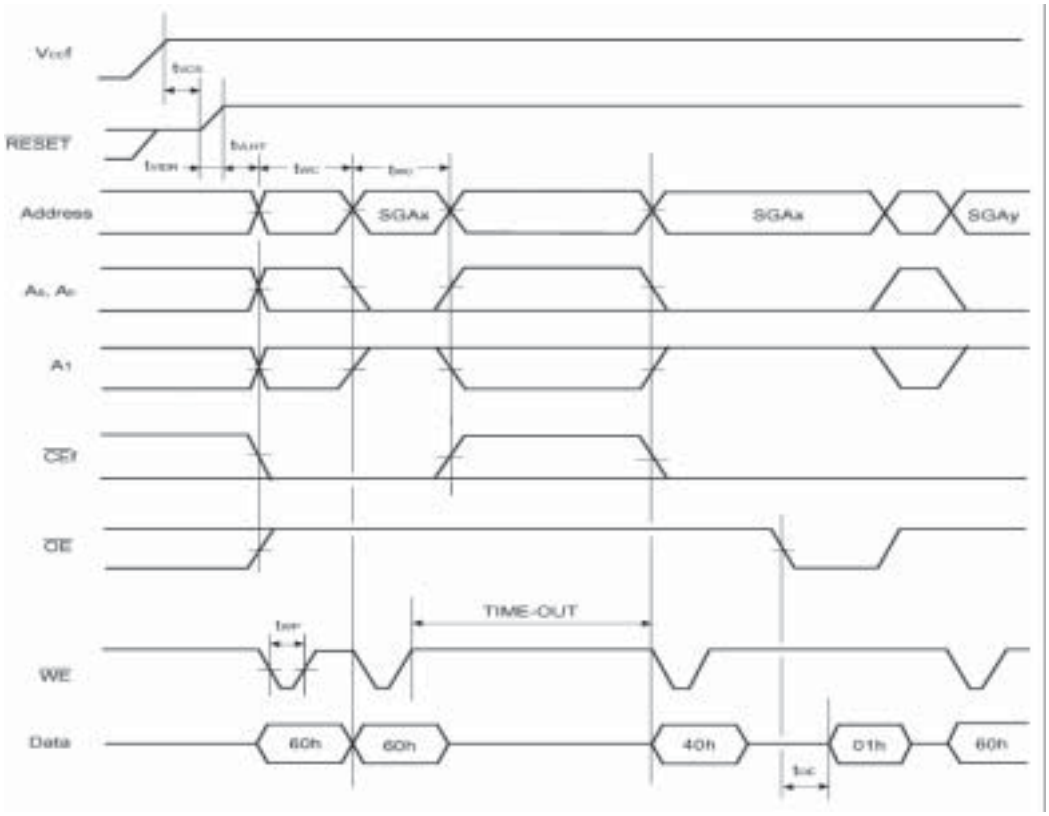
Flash RESET, RY/BY Timing Diagram



Flash Temporary Sector Group Unprotection

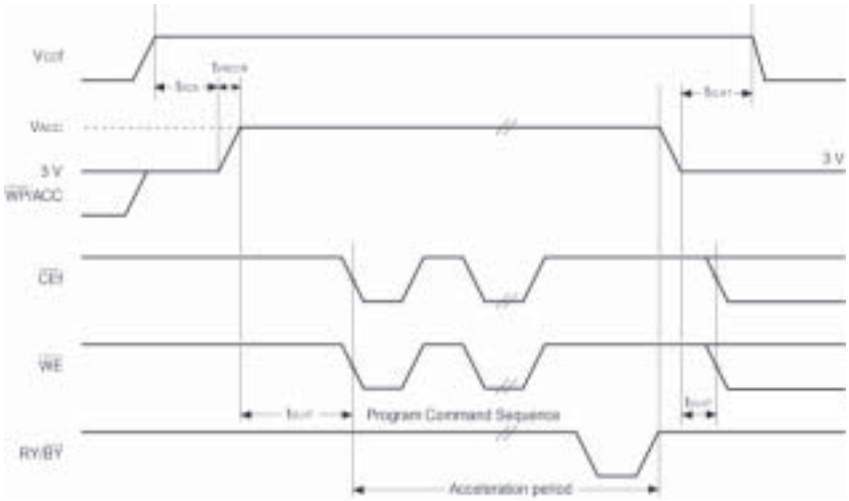


Flash Extended Sector Group Protection



SGAx: Sector Group Address to be protected
SGAy : Next Group Sector Address to be protected
TIME-OUT : Time-Out window = 250 µs (Min.)

Flash Accelerated Program



SRAM POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CCS} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	20	mA
			Ind.	—	25	
I_{CC1}	Operating Supply Current	V_{CCS} = Max., I_{OUT} = 0 mA, f = 0	Com.	—	3	mA
			Ind.	—	3	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CCS} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE1}_s$ = V_{IH}, $CE2_s$ = V_{IL}, f = 1 MHz	Com.	—	0.3	mA
			Ind.	—	0.3	
	OR					
	ULB Control	V_{CCS} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE1}_s$ = V_{IL}, f = 0, $\overline{UB}_s$ = V_{IH}, $\overline{LB}_s$ = V_{IH}				
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CCS} = Max., $\overline{CE1}_s \geq V_{CCS} - 0.2V$, $CE2_s \leq 0.2V$, $V_{IN} \geq V_{CCS} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com.	—	15	µA
			Ind.	—	15	
	OR					
	ULB Control	V_{CCS} = Max., $\overline{CE1}_s$ = V_{IL} $V_{IN} \leq 0.2V$, f = 0; $\overline{UB}_s$ / $\overline{LB}_s$ = V_{CCS} – 0.2V				

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

SRAM READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		70 ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
t_{RC}	Read Cycle Time	70	—	ns
t_{AA}	Address Access Time	—	70	ns
t_{OHA}	Output Hold Time	10	—	ns
t_{ACE1}	$\overline{CE1}_s$ Access Time	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	ns
t_{HZCE1}[2]	$\overline{CE1}_s$ to High-Z Output	0	25	ns
t_{LZCE1}[2]	$\overline{CE1}_s$ to Low-Z Output	10	—	ns
t_{BA}	$\overline{LB}_s$, $\overline{UB}_s$ Access Time	—	70	ns
t_{HZB}	$\overline{LB}_s$, $\overline{UB}_s$ to High-Z Output	0	25	ns
t_{LZB}	$\overline{LB}_s$, $\overline{UB}_s$ to Low-Z Output	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4 to 1.4V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

SRAM AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	V_{REF}
Output Load	See Figures 1 and 2

	2.7V - 3.3V
R1(Ω)	3070
R2(Ω)	3150
V_{REF}	1.5V
V_{TM}	2.8V

SRAM AC TEST LOADS

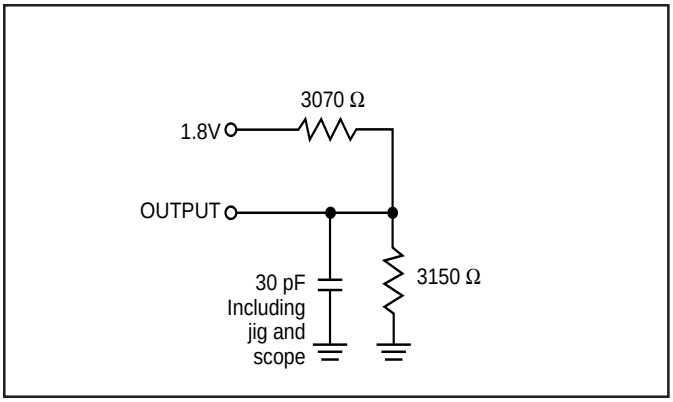


Figure 1

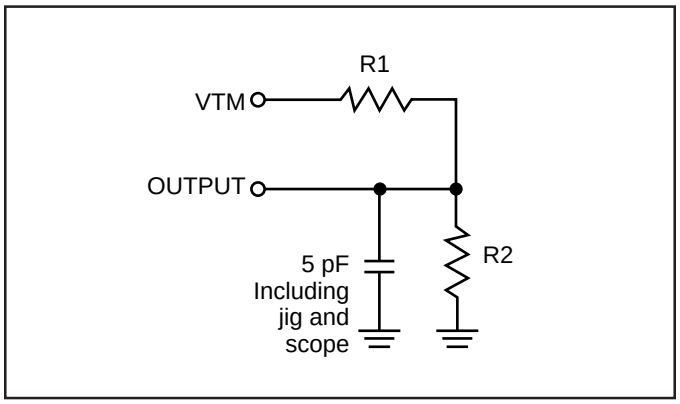
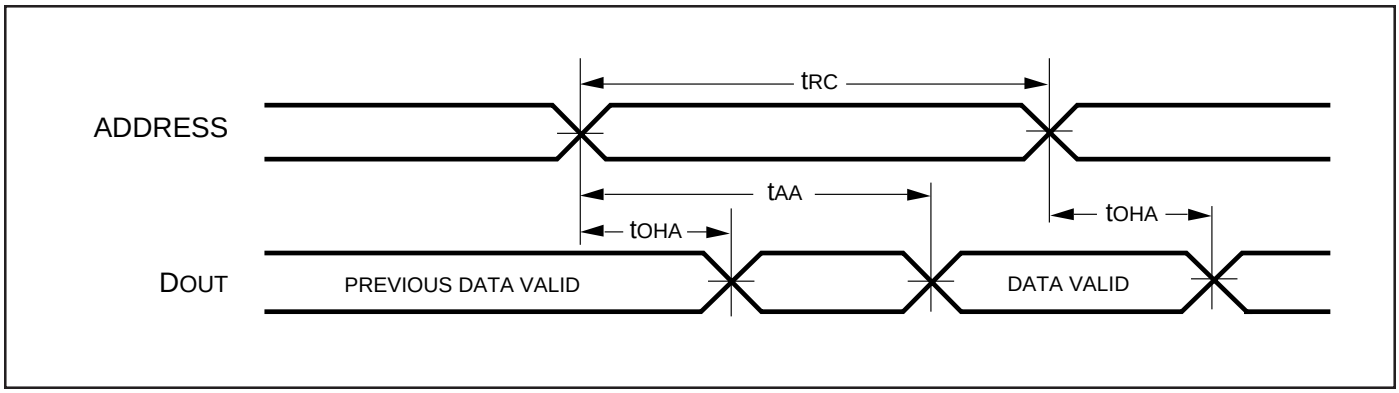


Figure 2

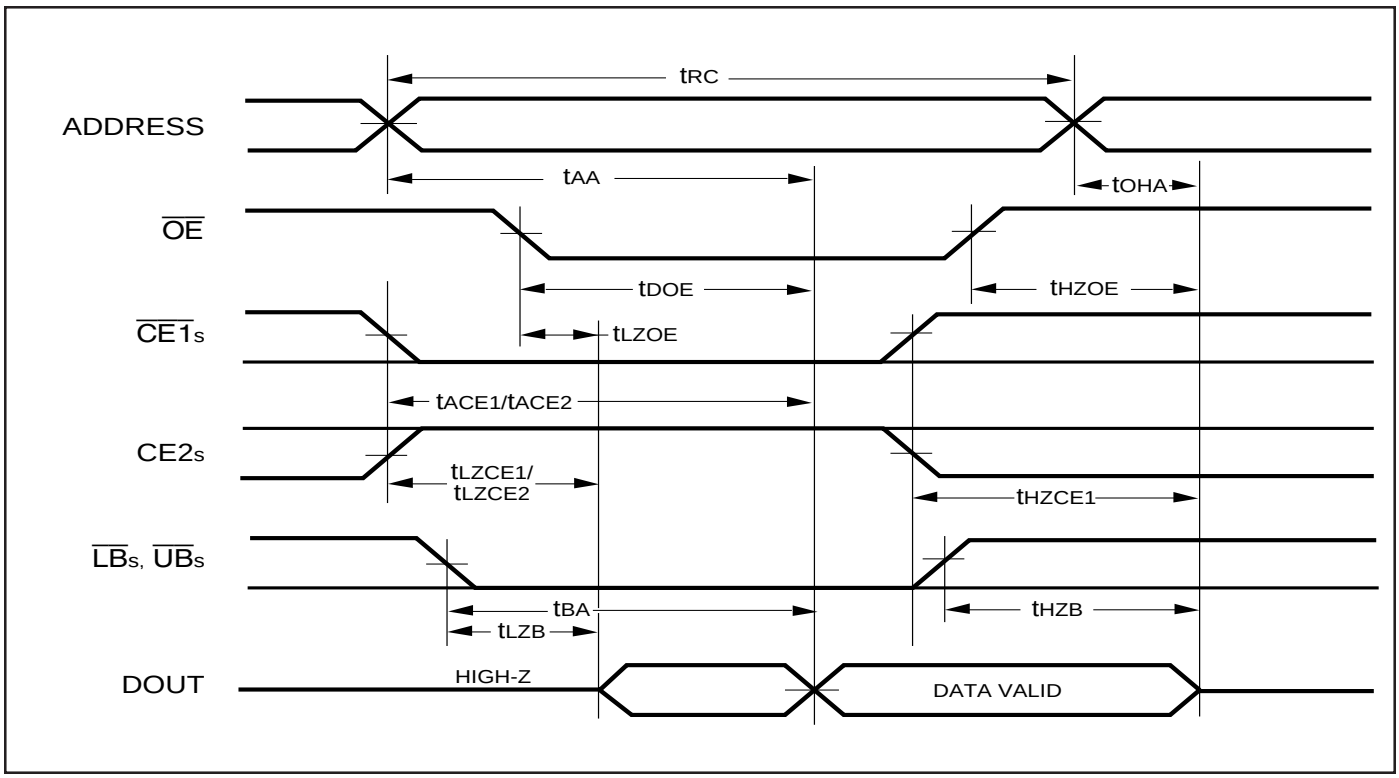
AC WAVEFORMS

SRAM READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE1}_s$ = $\overline{OE}$ = V_{IL}, $\overline{UB}_s$ or $\overline{LB}_s$ = V_{IL})



AC WAVEFORMS

SRAM READ CYCLE NO. 2[1,3] ($\overline{CE1}_s$, $\overline{OE}$, AND $\overline{UB}_s$/ $\overline{LB}_s$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$, $\overline{UB}_s$, or $\overline{LB}_s$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW transition.

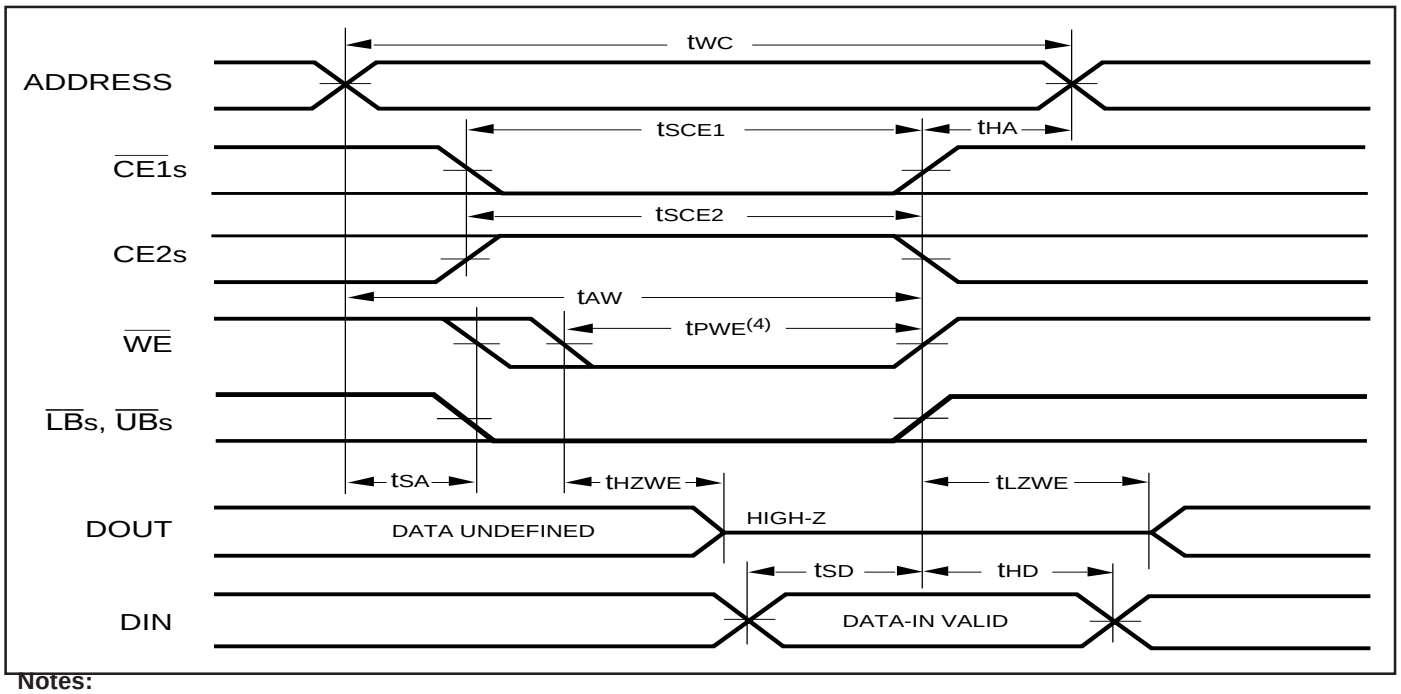
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	70 ns Min.	Max.	Unit
t_{WC}	Write Cycle Time	70	—	ns
t_{SCE1}	$\overline{CE1}_s$ to Write End	60	—	ns
t_{AW}	Address Setup Time to Write End	60	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWB}	$\overline{LB}_s$,$\overline{UB}_s$ Valid to End of Write	60	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	50	—	ns
t_{SD}	Data Setup to Write End	30	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V, input pulse levels of 0.4V to 1.4V and output loading specified in SRAM AC Test Loads: Figure 1
2. The internal write time is defined by the overlap of $\overline{CE1}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in SRAM AC Test Loads: Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

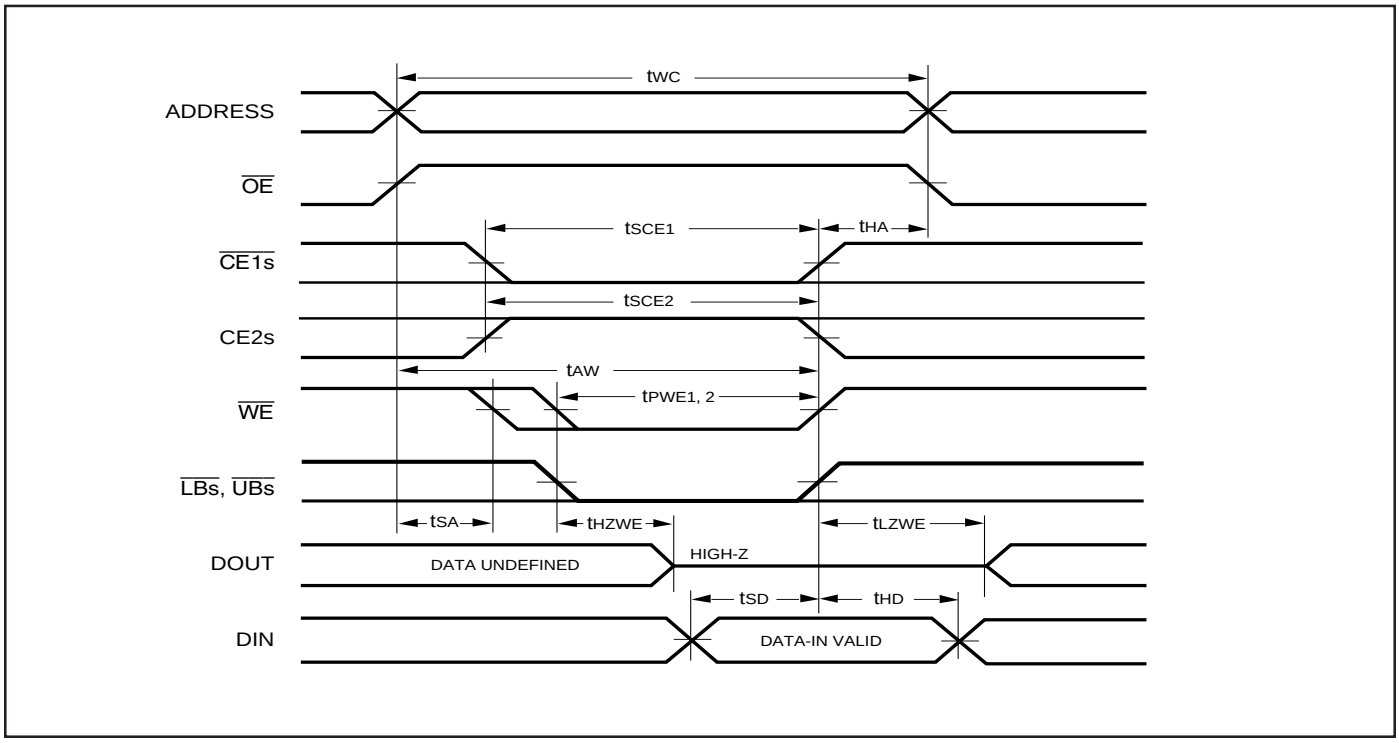
AC WAVEFORMS

SRAM WRITE CYCLE NO. 1[1,2] ($\overline{CE1}_s$ Controlled, $\overline{OE}$ = HIGH or LOW)

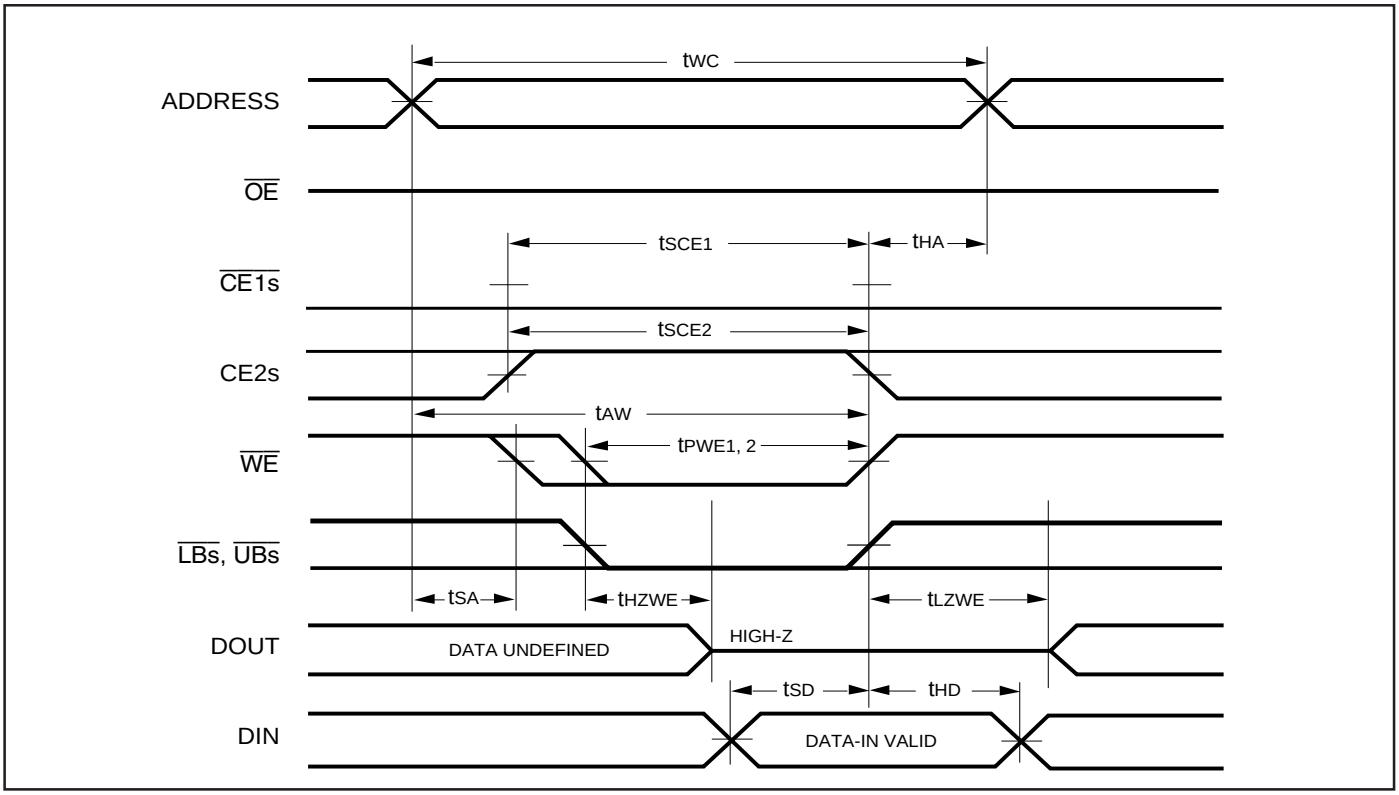


Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE1}_s$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}_s$ and $\overline{UB}_s$ inputs being in the LOW state.
2. WRITE = ($\overline{CE1}_s$) [($\overline{LB}_s$) = ($\overline{UB}_s$)] ($\overline{WE}$).

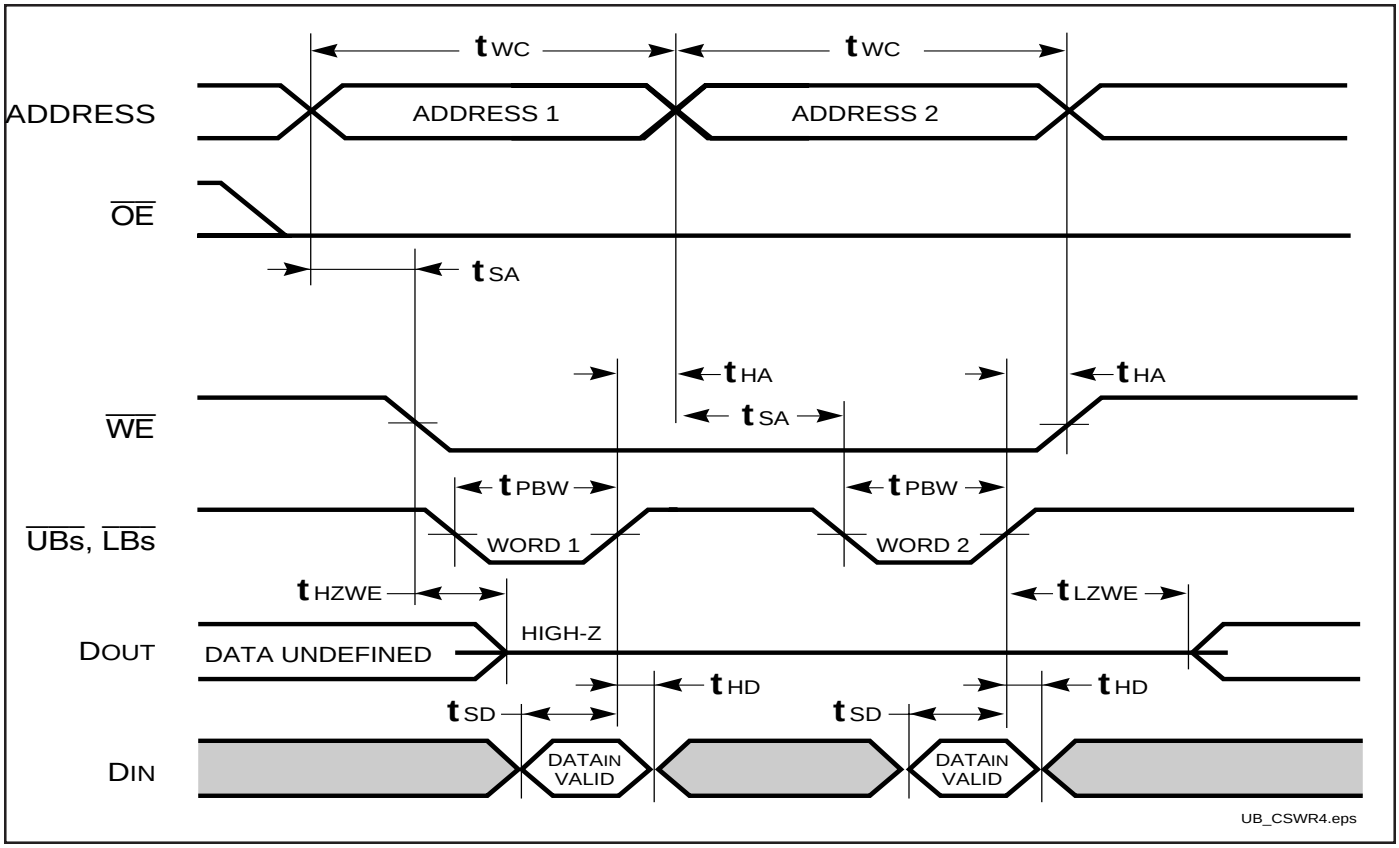
SRAM WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



SRAM WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



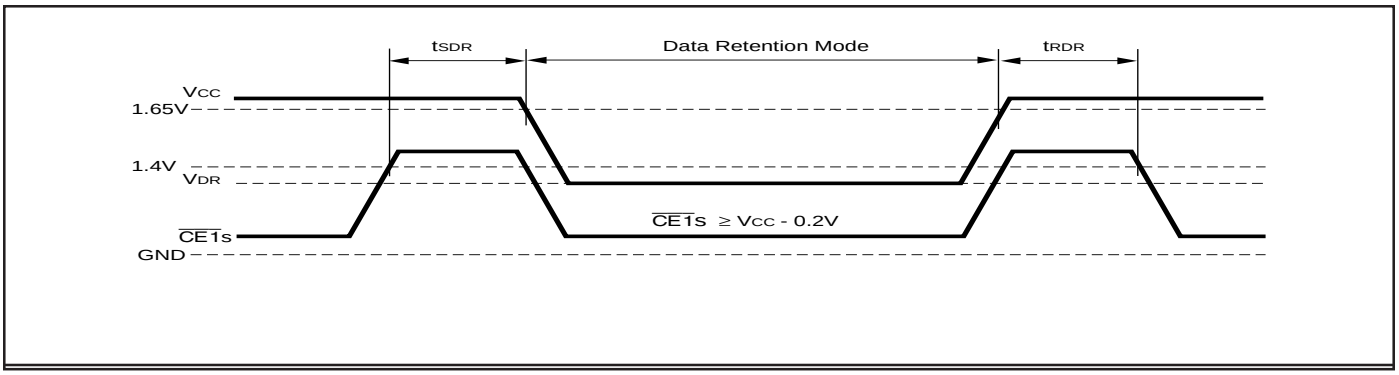
WRITE CYCLE NO. 4 ($\overline{UB}_s$/$\overline{LB}_s$ Controlled, $\overline{CE1}$s is LOW, CE2s is HIGH)



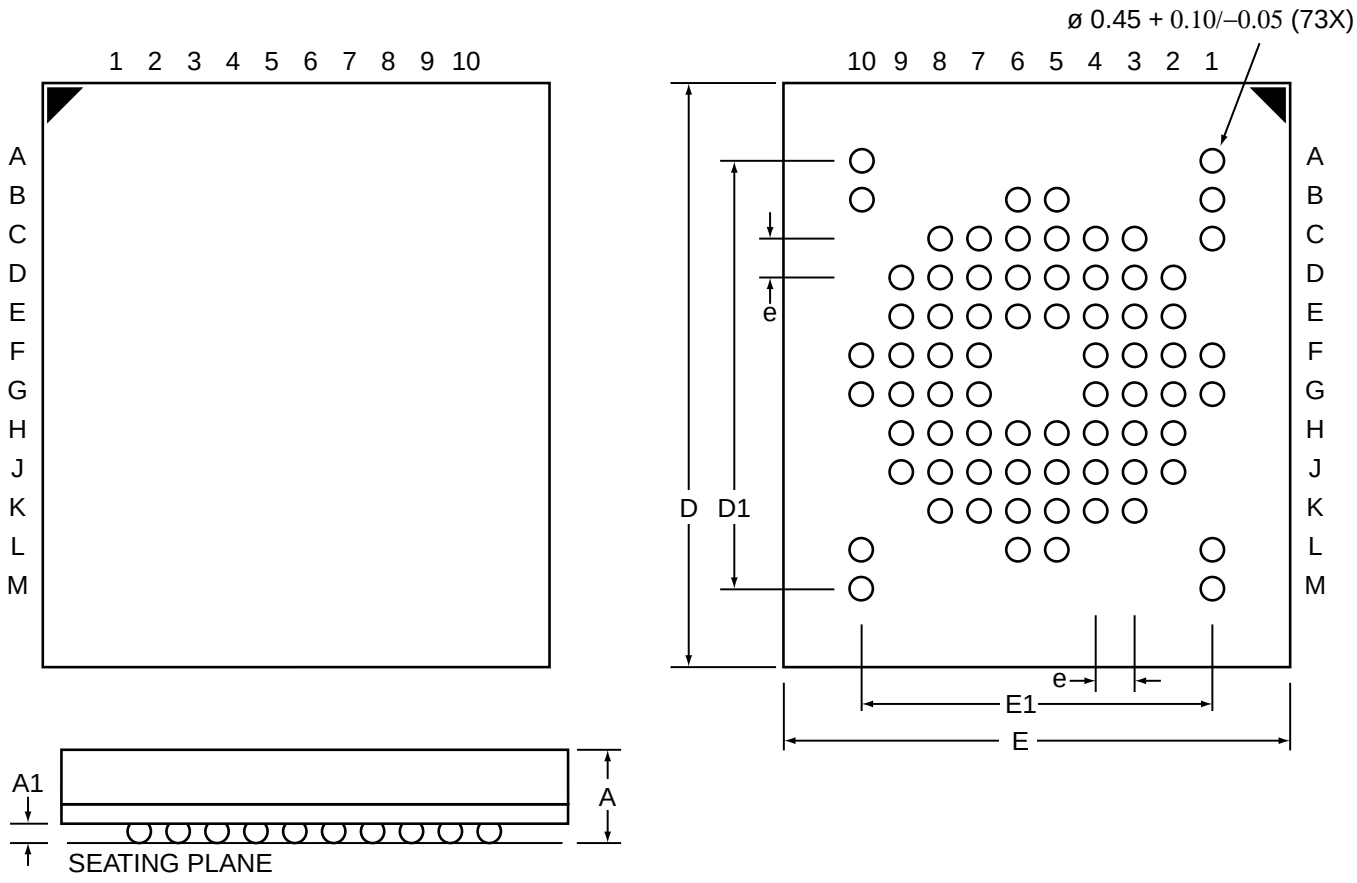
SRAM DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform	1.0	3.3	V
I_{DR}	Data Retention Current	Vcc = 1.0V, $\overline{CS1}$ ≥ Vcc – 0.2V	—	15	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

SRAM DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)

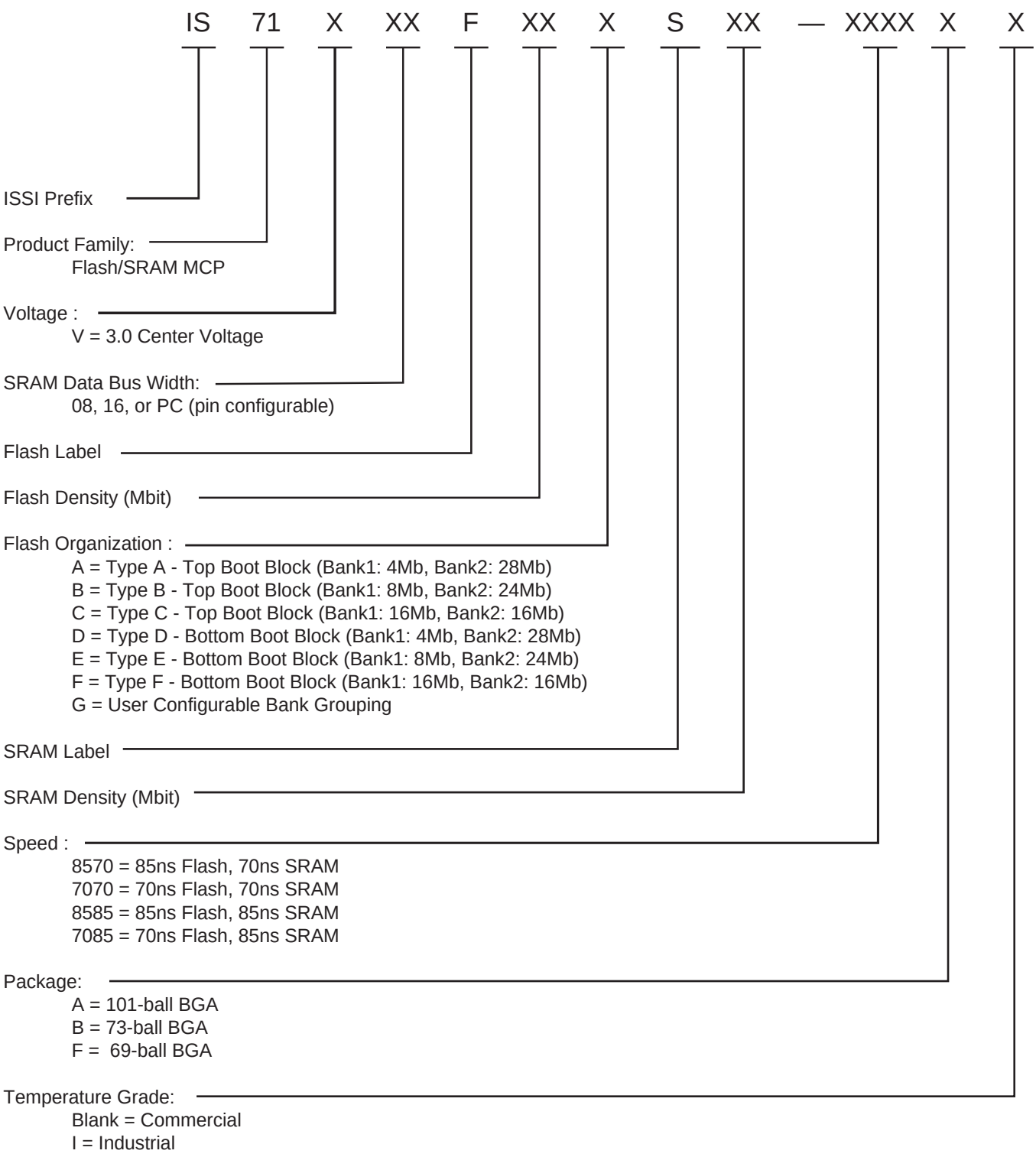


Mini Ball Grid Array – 73-Ball BGA (32 Mb Flash and 8 Mb SRAM)
Package Code: B (8 mm x 11.60 mm Body, 0.8 mm Ball Pitch**)**



Symbol	Min.	Typ.	Max.	Units
A	—	—	1.40	mm
A1	0.28	0.38	0.48	mm
D	11.50	11.60	11.70	mm
D1	—	8.80	—	mm
E	7.90	8.00	8.10	mm
E1	—	7.20	—	mm
e	—	0.80	—	mm

PART NUMBER LOGIC



Order Part No.	SRAM Data Bus	Boot Section	Flash Bank Organization	Flash Speed(ns)	SRAM Speed(ns)	Package
IS71V08F32AS08-7070BI	8	Top	4Mb, 28Mb	70	70	73-ball BGA
IS71V08F32BS08-7070BI	8	Top	8Mb, 24Mb	70	70	73-ball BGA
IS71V08F32CS08-7070BI	8	Top	16Mb, 16Mb	70	70	73-ball BGA
IS71V08F32DS08-7070BI	8	Bottom	4Mb, 28Mb	70	70	73-ball BGA
IS71V08F32ES08-7070BI	8	Bottom	8Mb, 24Mb	70	70	73-ball BGA
IS71V08F32FS08-7070BI	8	Bottom	16Mb, 16Mb	70	70	73-ball BGA
IS71V08F32AS08-7085BI	8	Top	4Mb, 28Mb	70	85	73-ball BGA
IS71V08F32BS08-7085BI	8	Top	8Mb, 24Mb	70	85	73-ball BGA
IS71V08F32CS08-7085BI	8	Top	16Mb, 16Mb	70	85	73-ball BGA
IS71V08F32DS08-7085BI	8	Bottom	4Mb, 28Mb	70	85	73-ball BGA
IS71V08F32ES08-7085BI	8	Bottom	8Mb, 24Mb	70	85	73-ball BGA
IS71V08F32FS08-7085BI	8	Bottom	16Mb, 16Mb	70	85	73-ball BGA
IS71V08F32AS08-8570BI	8	Top	4Mb, 28Mb	85	70	73-ball BGA
IS71V08F32BS08-8570BI	8	Top	8Mb, 24Mb	85	70	73-ball BGA
IS71V08F32CS08-8570BI	8	Top	16Mb, 16Mb	85	70	73-ball BGA
IS71V08F32DS08-8570BI	8	Bottom	4Mb, 28Mb	85	70	73-ball BGA
IS71V08F32ES08-8570BI	8	Bottom	8Mb, 24Mb	85	70	73-ball BGA
IS71V08F32FS08-8570BI	8	Bottom	16Mb, 16Mb	85	70	73-ball BGA
IS71V08F32AS08-8585BI	8	Top	4Mb, 28Mb	85	85	73-ball BGA
IS71V08F32BS08-8585BI	8	Top	8Mb, 24Mb	85	85	73-ball BGA
IS71V08F32CS08-8585BI	8	Top	16Mb, 16Mb	85	85	73-ball BGA
IS71V08F32DS08-8585BI	8	Bottom	4Mb, 28Mb	85	85	73-ball BGA
IS71V08F32ES08-8585BI	8	Bottom	8Mb, 24Mb	85	85	73-ball BGA
IS71V08F32FS08-8585BI	8	Bottom	16Mb, 16Mb	85	85	73-ball BGA
IS71V16F32AS08-7070BI	16	Top	4Mb, 28Mb	70	70	73-ball BGA
IS71V16F32BS08-7070BI	16	Top	8Mb, 24Mb	70	70	73-ball BGA
IS71V16F32CS08-7070BI	16	Top	16Mb, 16Mb	70	70	73-ball BGA
IS71V16F32DS08-7070BI	16	Bottom	4Mb, 28Mb	70	70	73-ball BGA
IS71V16F32ES08-7070BI	16	Bottom	8Mb, 24Mb	70	70	73-ball BGA
IS71V16F32FS08-7070BI	16	Bottom	16Mb, 16Mb	70	70	73-ball BGA

ORDERING INFORMATION

Industrial Range: -40ºC to +85ºC

Order Part No.	SRAM Data Bus	Boot Section	Flash Bank Organization	Flash Speed(ns)	SRAM Speed(ns)	Package
IS71V16F32AS08-7085BI	16	Top	4Mb, 28Mb	70	85	73-ball BGA
IS71V16F32BS08-7085BI	16	Top	8Mb, 24Mb	70	85	73-ball BGA
IS71V16F32CS08-7085BI	16	Top	16Mb, 16Mb	70	85	73-ball BGA
IS71V16F32DS08-7085BI	16	Bottom	4Mb, 28Mb	70	85	73-ball BGA
IS71V16F32ES08-7085BI	16	Bottom	8Mb, 24Mb	70	85	73-ball BGA
IS71V16F32FS08-7085BI	16	Bottom	16Mb, 16Mb	70	85	73-ball BGA
IS71V16F32AS08-8570BI	16	Top	4Mb, 28Mb	85	70	73-ball BGA
IS71V16F32BS08-8570BI	16	Top	8Mb, 24Mb	85	70	73-ball BGA
IS71V16F32CS08-8570BI	16	Top	16Mb, 16Mb	85	70	73-ball BGA
IS71V16F32DS08-8570BI	16	Bottom	4Mb, 28Mb	85	70	73-ball BGA
IS71V16F32ES08-8570BI	16	Bottom	8Mb, 24Mb	85	70	73-ball BGA
IS71V16F32FS08-8570BI	16	Bottom	16Mb, 16Mb	85	70	73-ball BGA
IS71V16F32AS08-8585BI	16	Top	4Mb, 28Mb	85	85	73-ball BGA
IS71V16F32BS08-8585BI	16	Top	8Mb, 24Mb	85	85	73-ball BGA
IS71V16F32CS08-8585BI	16	Top	16Mb, 16Mb	85	85	73-ball BGA
IS71V16F32DS08-8585BI	16	Bottom	4Mb, 28Mb	85	85	73-ball BGA
IS71V16F32ES08-8585BI	16	Bottom	8Mb, 24Mb	85	85	73-ball BGA
IS71V16F32FS08-8585BI	16	Bottom	16Mb, 16Mb	85	85	73-ball BGA