AT&T Microelectronics

41MGA and 41MPA Quad Differential Line Drivers

Features

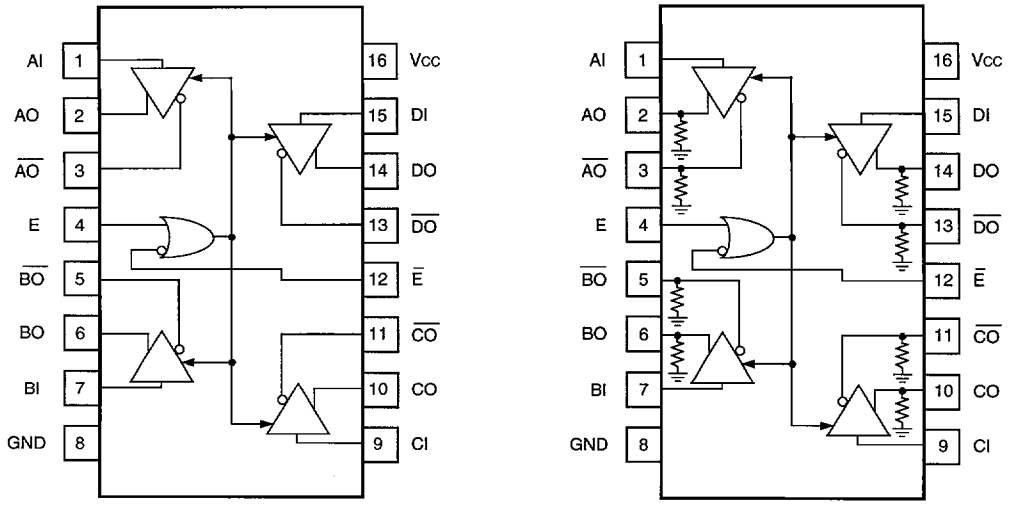
- Pin-equivalent to the general-trade 26LS31 device, with improved speed, reduced power consumption, and significantly lower levels of EMI
- Four line drivers per package
- Meets ESDI standards
- 2.5 ns maximum propagation delay
- Single 5.0 V supply
- Operating temperature range: 0 °C to 85 °C (See Section 9.)
- 200 Mbits/s or 400 Mbits/s maximum data rates when used with the 41L*x* and 41M*x* receivers respectively
- Logic to convert TTL input logic levels to differential, pseudo-ECL output logic levels
- No line loading when V_{CC} = 0 V
- High output driver for 50 Ω loads
- 250 mA short-circuit current (typical)
- <0.2 ns output skew (typical)

Description

The 41MGA and 41MPA Quad Differential Line Driver integrated circuits are TTL-input-to-pseudo-ECL-differential-output line drivers used for digital data transmission over balanced transmission lines. The 41MGA requires that the customer provide a terminating resistor on their board while the 41MPA incorporates the terminating resistor on-chip. The 41MGA/41MPA devices are improved versions of the 41MG/41MP devices, resulting in reduced complementary output skew, reduced sensitivity into the inputs, and hence an improved, more symmetrical output signal and lower EMI. To accomplish these improvements, a gate was added between the input and output stages. This change results in an increase in propagation delay of 0.5 ns. The 41MGA/41MPA line drivers are pin equivalent to the general-trade 26LS31, but offer increased speed, decreased power consumption, and significantly lower levels of electromagnetic interference (EMI).

The packaging options that are available for the quad differential line drivers include a 16-pin DIP (41MGA, 41MPA), a 16-pin J-lead SOJ (1041MGA, 1041MPA), a 16-pin gull-wing SOIC (1141MGA, 1141MPA), and a 16-pin narrow-body gull-wing SOIC (1241MGA).

Pin Information



Note: The device is disabled when E = 0 and $\overline{E}$ = 1.

Figure 3-4. 41MGA and 41MPA Logic Diagrams

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	7.0	V
Ambient Operating Temperature	T_A	0	85	°C
Storage Temperature	T_{stg}	–40	125	°C

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. The standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is used. The HBM ESD threshold voltage presented here was obtained using this circuit.

Device	Rating
41MGA/41MPA Drivers	>1000 V

Electrical Characteristics

Table 3-10. 41MGA and 41MPA Power Supply Current Characteristics

T_A = 0 °C to 85 °C, V_{CC} = 5 V ± 0.5 V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current:					
41MGA*					
All Outputs Disabled	I_{CC}	—	55	80	mA
All Outputs Enabled	I_{CC}	—	35	50	mA
41MPA†					
All Outputs Disabled	I_{CC}	—	130	180	mA
All Outputs Enabled	I_{CC}	—	160	220	mA

* Measured with no load.

† The additional power dissipation is the result of integrating the termination resistors into the device. I_{CC} is measured with a 100 Ω resistor across the driver outputs.

Table 3-11. 41MGA and 41MPA Voltage and Current Characteristics

T_A = 0 °C to 85 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages, V_{CC} = 4.5 V:					
Low, I_{OL} = –8.0 mA*	V_{OL}	—	3.0	V_{OH} – 0.8†	V
High, I_{OH} = –40.0 mA*	V_{OH}	3.0	4.0	—	V
High Z, I_{OH} = –1.0 mA, V_{CC} = 4.75 V	V_{OZ}	—	2.0	V_{OH} – 0.02	V
Input Voltages:					
Low, V_{CC} = 5.5 V	V_{IL}‡	—	—	0.8	V
High, V_{CC} = 4.5 V	V_{IH}‡	2.0	—	—	V
Clamp, V_{CC} = 4.5 V, I_I = –5.0 mA	V_{IK}	—	—	–1.5	V
Short-circuit Output Current, V_{CC} = 5.5 V	I_{OS}§	–100	–250	–350	mA
Input Currents, V_{CC} = 5.5 V:					
Low, V_I = 0.4 V	I_{IL}	—	—	–400	µA
High, V_I = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_I = 5.5 V	I_{IH}	—	—	100	µA
Output Resistors, 41MPA	R_O	—	220	—	Ω

* Typical value of the output current with load for the 41MGA and the 41MPA when terminated per Figure 6-5.

† V_{OL} must be a minimum of 0.8 V less than its complementary output.

‡ The input levels provide zero noise immunity and should be tested only in a static, noise-free environment.

§ Test must be performed one lead at a time to prevent damage to the device.

Timing Characteristics

Table 3-12. 41MGA and 41MPA Timing Characteristics (See Figures 6-1 and 6-2.)

Propagation-delay test circuit connected to output (see Figure 6-6).

T_A = 25 °C, V_{CC} = 5 V ± 0.5 V.

Symbol	Parameter	Typ	Max	Unit
	Propagation Delay:			
t_{P1}	Input High to Output	1.5	2.5	ns
t_{P2}	Input Low to Output	1.5	2.5	ns
	Disable Time:			
t_{PHZ}	High to High Impedance	8	12	ns
t_{PLZ}	Low to Low Impedance	8	12	ns
	Enable Time:			
t_{PZH}	High Impedance to High	8	12	ns
t_{PZL}	High Impedance to Low	8	12	ns
t_{skew}	Output Skew, $\lvert t_{P1} - t_{P2} \rvert$	0.1	0.3	ns
Δt_{skew}	Difference Between Drivers	0.2	0.5	ns
t_{tLH}	Rise Time	—	2.0	ns
t_{tHL}	Fall Time	—	2.0	ns