

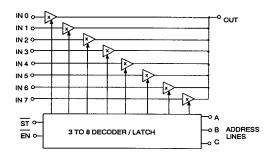
# GM8108 Wideband 8x1 Video Multiplexer Module

DATA SHEET

## **FEATURES**

- single 32 lead SIP
- on board decoding and latching
- minimal external parts required
- · convenient 8 x 1 configuration
- · wideband for HDTV applications

# **FUNCTIONAL BLOCK DIAGRAM**



#### TRUTH TABLE

СВ		Α	EN	ST	OUTPUT		
Х	Х	Х	1	Х	HI-Z		
X	Х	Х	X	0	HI-Z		
0	0	0	0	Ţ	IN 0		
0	0	1	0	<u></u> F	IN 1		
0	1	0	0	J.	IN 2		
0	1	1	0	Ā	IN 3		
1	0	0	O	<u>_</u>	IN 4		
1	0	1	0	Ł	IN 5		
1	1	0	0	Ţ	IN 6		
1	1	1	0	Ţ	IN 7		

X = don't care

### CIRCUIT DESCRIPTION

The GM8108 module is a complete 8 x 1 wideband video multiplexer fabricated on a single miniature PCB. The circuitry consists of eight 1 x 1 video crosspoint ICs multiplexed to form an 8 input by 1 output expandable multiplexer. Included on the board is a three to eight decoder with latches. Separate STROBE and ENABLE logic inputs along with the three address lines A, B and C control crosspoint selection.

The PCB assembly uses eight GX4201 surface mount devices and is only 0.55 inches high. The overall length is 3.2 inches. These small dimensions mean that high density matrices can be made using several modules. Also, a convenient SIP format pin out makes PCB layout of large N by M matrices simple and straightforward.

The entire module may be disabled by applying a logic ONE to the ENABLE input. Crosspoint selection is made by applying the correct address code to the address inputs and applying a logic ZERO to the STROBE input. Returning this level to logic ONE latches ON the crosspoints.

All logic inputs are TTL and 5 volt CMOS compatible. The supply voltage range for the GM8108 module is  $\pm$  4.8 to  $\pm$ 5.2 volts.

#### **APPLICATIONS**

- · broadcast and wideband video switching
- · building block for large video routers
- · very high density video matrices
- stand alone 8 x 1 video multiplexers

#### ORDERING INFORMATION

Part Number	Package Type	Temperature Range			
GM8108 - CSG	32 pin SIP	0° to 70° C			

Revision Date: January 1994.

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# ABSOLUTE MAXIMUM RATINGS

Parameter	Value		
Power Supply Voltage	±5.5 V		
Operating Temperature Range	0° C ≤ T <sub>A</sub> ≤ 70°C		
Storage Temperature Range	-65° C ≤ T <sub>S</sub> ≤ 150°C		
Lead Temperature (soldering 10 Sec)	260°C		
Analog Input Range	$-5.5~\text{V} \leq \text{V}_{\text{S}} \leq +5.5~\text{V}$		
Logic Input Voltage Range	-0.5 V ≤ V <sub>L</sub> ≤ 5.5 V		
Output Load Current	12 mA		

# **ELECTRICAL CHARACTERISTICS**

 $\rm V_S=\pm5V$  DC,  $\rm \, 0^{\circ}C < T_A < 70^{\circ}C, \, R_L=10 \, k\Omega, \, C_L=10 \, pF,$  (ON) means one crosspoint on, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Тур	Max	Units
Supply Voltage	±V		4.8	5.0	5.2	٧
	I+	Enable = 0 (ON)	-	20	23	mA
Supply Current		Enable = 1 (OFF)	-	4.4	5.5	mA
(does not include R <sub>EXT</sub> I)	I-	Enable = 0 (ON)	-	12	15	mA
		Enable = 1 (OFF)	-	3.2	4.5	mA
Analog Output Voltage Swing	V <sub>OUT</sub>	Extremes before clipping occurs	-2	-	+3	v
Output Offset Voltage	V <sub>os</sub>	$T_A = 25$ °C 75 Ω resistance-20 on each input to GND	-5	+10	-	mV
Crosspoint selection Turn-On Time	t <sub>ON</sub>	Control input to appearance of signal	-	200	400	ns
Crosspoint selection Turn-Off Time	t <sub>OFF</sub>	Control input to appearance of signal	500	1000	-	ns
Insertion Loss	I.L.	1V p-p at 100 kHz	-	0.025	-	dB
Bandwidth (-3dB)B.W.	B.W.		-	250	-	MHz
Input Resistance R <sub>IN</sub>		Enable = 0 (ON)	1	-	-	МΩ
Input Capacitance	C <sub>IN</sub>	Enable = 0 (ON)	-	1.05	-	ρF
		Enable = 1 (OFF)	-	1.1	-	pF
Output Resistance	R <sub>OUT</sub>	Enable = 0 (ON)	-	7	~	Ω
Output Capacitance	C <sub>OUT</sub>	Enable = 1 (OFF)	-	12	-	pF
Differential Gain	dg	at colorburst 40 IRE, f=3.58MHz	-	0.035	0.04	%
Differential Phase	dp	at colorburst 40 IRE, f=3.58MHz	-	-	0.01	degrees
Off Isolation	XTLK CD	f = 10 MHz (Note 2)	90	94	-	dB
Crosstalk (All hostile)	XTLK AH	f = 10 MHz (Note 1) $R_S = 10 \Omega$	80	85	-	dB

Note 1: Sweep on 7 inputs 1 volt p-p, 8th input has 75  $\Omega$  to ground

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<sup>2:</sup> Output is loaded with one enabled module whose ON input has 37.5  $\Omega$  resistor to ground or a resistor R = 8  $\Omega$ 

<sup>3:</sup> Differential phase and gain are measured with an active 6 mA current source

#### **DETAILED DESCRIPTION**

Figure 1 is a functional block diagram of the 8x1 module. The 1x1 crosspoint ICs are multiplexed to form the desired circuit configuration.

A single CMOS device performs 3 to 8 line decoding as well as latching using a STROBE input. The ENABLE input allows the entire module to be selected or disabled in order to facilitate the multiplexing of other modules.

Each GX4201 device is a 1x1 video crosspoint characterized by a low distortion, unilateral signal path consisting of emitter followers at the input and output with level shifting circuits in between.

Extemely high off-isolation in the order of 80 dB at 100 MHz is achieved by internal clamping in the signal path. The input impedance is extremely high and constant, allowing for multi-input bussing.

The input may be directly driven from cables if a terminating resistor, equal to the characteristic impedance of the cable, is connected from input to ground.

The output requires a high impedance load of at least 10 k $\Omega$  to maintain the high degree of differential gain and phase, characteristic of the crosspoint devices.

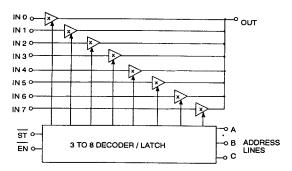


Fig. 1 Functional Block Diagram

Figure 2 shows the circuit details of the module which uses a CMOS74HC237 combination 3 to 8 decoder/latch for crosspoint selection.

The eight GX4201 devices with their outputs tied together effectively form an 8x1 multiplexer. Pin 1 of each device is an ENABLE input requiring a logic HIGH level in order to turn on the crosspoint. The logic level is provided by the 74HC237 device. The GX4201 data sheet is available from Gennum Corporation by ordering document number 510-74. It fully describes the operation of the device along with electrical characteristics and performance curves.

Address lines A, B and C control the decoder so that only one output goes HIGH for any of the eight address possibilities.

An ENABLE input on the 74HC237 is used to disable the decoder inputs resulting in all the outputs going to a logic LOW state. This causes all the GX4201 outputs to go to their high impedance state, effectively disabling the module, simplifying the multiplexing of additional modules.

All address bits are internally latched by the 74HC237. The STROBE input is used as the clock for the latches and operates on the transition from logic LOW to HIGH.

Video is applied to pin 7 of each crosspoint. The adjacent pins are connected to ground in order to maintain a high degree of channel to channel isolation. The output of each device (pin 4) is connected to the corresponding output of the other seven switches.

Both positive and negative supply voltages are routed to each device. Capacitors C1, C2 and C3 function as supply rail decoupling capacitors.

Ground pins separate each video input, and the video inputs are situated to one end and in the middle of each module. It is therefore straightforward to parallel additional module inputs.

All power supply and logic functions are brought out at one end of each module. This allows for simplified multiplexing of additional modules. The module is enabled with a logic LOW on the ENABLE input, the output reflects the latched input selected by ADDRESS BITS A, B and C when the STROBE input is returned from a logic LOW to a logic HIGH.

Since each video input is represented by a high impedance, several inputs may be bussed to form multi-input matrices. It is important in these situations to follow careful motherboard layout, and to use ample groundplane. The bussed inputs should be driven from a stable, low impedance buffer amplifier. In some cases, a small value series resistor at each video input will prevent unwanted R.F. oscillations.

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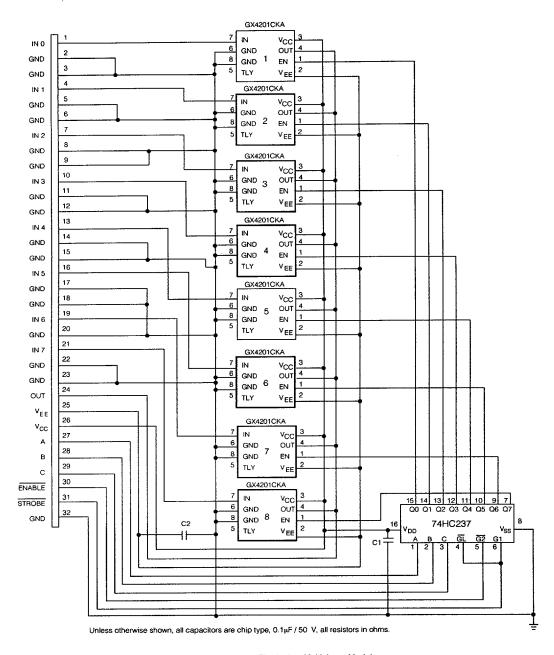
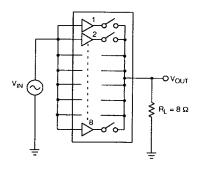
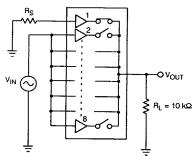


Fig. 2 8x1 Multiplexer Module

# **GM8108 TEST CIRCUITS**



Disabled Crosstalk



All Hostile Crosstalk

# TYPICAL PERFORMANCE CURVES

V<sub>S</sub> = 5V, T<sub>A</sub> = 25°C unless otherwise shown

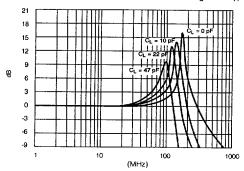


Fig. 3 Frequency Response \*

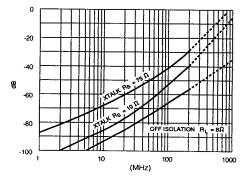


Fig. 4 Off-isolation and All Hostile Crosstalk

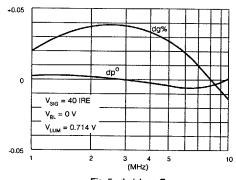
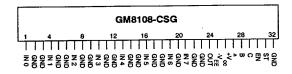


Fig. 5 dg / dp vs Frequency

\* The frequency response may be flattened by inserting a small R-C low pass filter in series with the output. An application note (Document 510 - 39) describes the compensation technique in detail.

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Pin Connections 32 Pin SIP

Key: INx = Video input x

GND = Ground

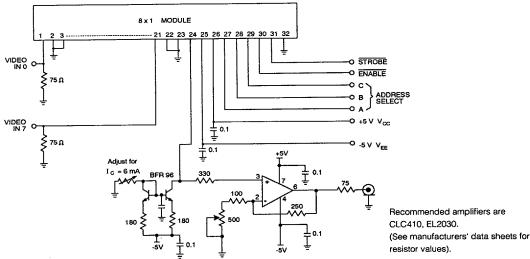
VCC = Positive supply voltage

VEE = Negative supply voltage

OUT = Video Output

EN = Enable ST = Strobe

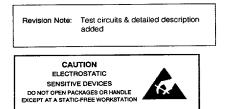
A,B C = Address input



#### NOTES:

- 1. All logic inputs require a 10 kΩ pull-up resistor.
- The BFR 96 current source circuit may be replaced with an 820 Ω resistor to V<sub>EE</sub>. This will result in a slight increase in insertion loss and differential gain and differential phase.
- 3. All capacitors are chip type, 0.1  $\mu F$  / 50 V.

Typical Application Circuit



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