HARRIS

CDP68EM05D2
CDP68EM05D2N

CMOS High Performance Silicon Gate 8-Bit Microcontroller Emulator

January 1991

Features

- CDP68HC05D2 Microcontroller Emulation
  - All CDP68HC05D2 Hardware and Software Features, Except as Noted in this Data Sheet
- Full 8K Byte Address Space Available (8064 Bytes Available Externally)
- 96 Bytes of On Chip RAM, No ROM
- Un-Multiplexed External Address and Data Lines
- Available In Two Package Types
  - CDP68EM05D2 - 40 Lead Piggyback Package with 2764 EPROM Socket Capability
  - CDP68EM05D2N - 68 Lead Plastic Chip Carrier (PLCC)

Description

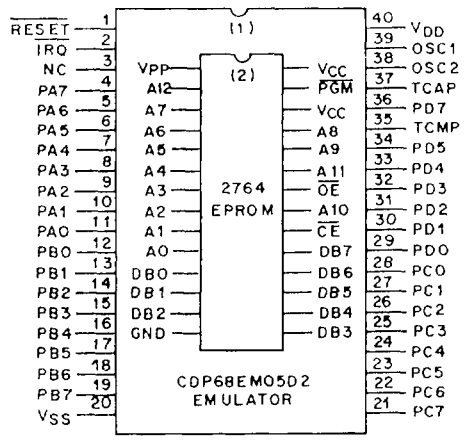
The CDP68EM05D2 and CDP68EM05D2N Emulator devices are functionally equivalent to the CDP68HC05D2 microcomputer, and are designed to permit prototype development and preproduction of systems for mask programmed applications. Data bus, address bus and control signals are externally available to provide off chip address capability.

In addition to this feature, the Emulator devices differ from the CDP68HC05D2 microcomputer as follows: 1) Memory locations which are occupied as ROM on the CDP68HC05D2 are accessed as external locations with the Emulators. 2) Mask programmable options available on the microcomputer (i.e., CPU oscillator type, external interrupt sense and timeout delay for power on Reset or exit from STOP mode) are fixed in hardware in the Emulator devices, and are available as separate Emulator types identified with suffix letters. See "Customer Ordering Information" in this data sheet for a description of available emulator types.

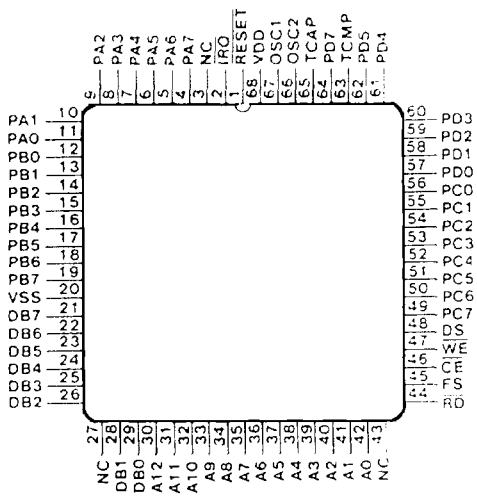
The CDP68EM05D2 and CDP68EM05D2N represent two different package types. The CDP68EM05D2 is available in a piggyback package having the footprint of the 40 lead dual-in-line package of the CDP68HC05D2 microcomputer. The top of the piggyback package has socket capability for a 28 lead EPROM. The CDP68EM05D2N is available in a 68 lead Plastic Chip Carrier (PLCC).

Pinouts

CDP68EM05D2
40 LEAD PIGGYBACK PACKAGE
TOP VIEW



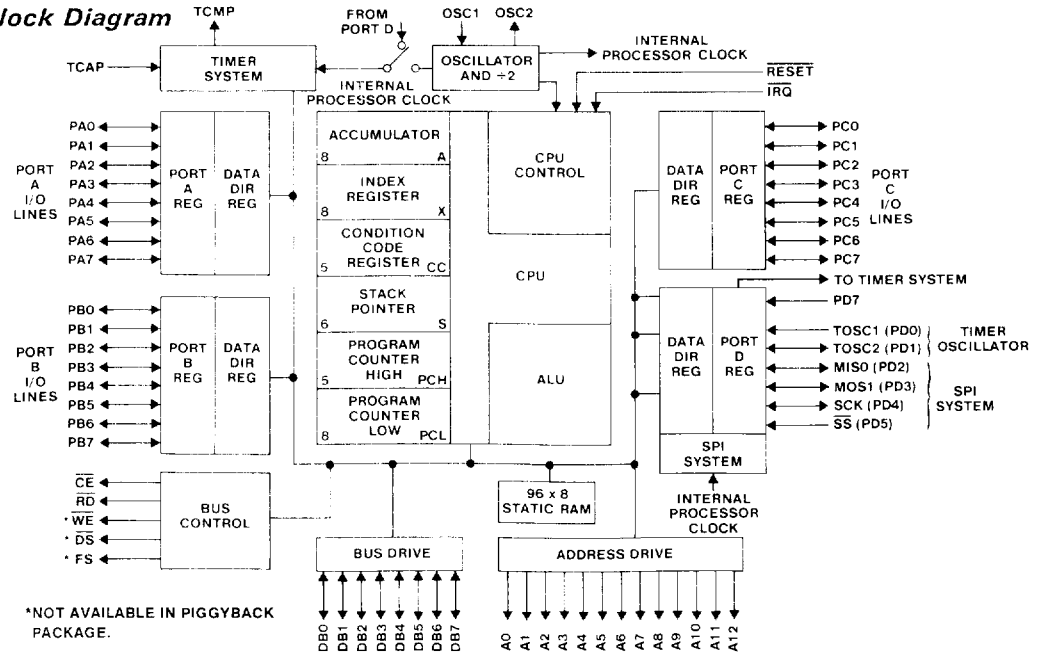
CDP68EM05D2N
68 LEAD PLASTIC CHIP CARRIER
TOP VIEW



3 MICRO-PROCESSORS

File Number 2755

Block Diagram



Memory

The CDP68EM05D2 and CDP68EM05D2N Emulators each have a total address space of 8192 bytes. The Emulators have implemented 128 bytes of the address locations for I/O and internal RAM. The remainder is available for external memory. The first 256 bytes of memory (page zero) are comprised of the I/O port locations, timer locations, 128 bytes of external address space and 96 bytes of RAM. The next 7936 bytes are available to address external memory. The address map is shown in Figure 1. A description of the remaining internal addressable functions can be found in the CDP68HC05D2 data sheet, File No. 1557.1, see Section 2 of this Data Book.

Signal Descriptions

The following list includes only those additional signals that are not available on the CDP68HC05D2 microcomputer. See the CDP68HC05D2 data sheet for a description of the remaining signals which are common to the Emulators and the CDP68HC05D2 microcomputer.

A0-A12 - Address lines 0 through 12.

DB0-DB7 - Bidirectional 8-bit non-multiplexed data bus with TTL inputs.

$\overline{CE}$, ($\overline{OE}$*) - Chip Enable: An output signal used for selecting external memory or I/O. A low level indicates when external RAM or I/O is being accessed. The Chip Enable signal will not go true, however, when addressing the 10 unused locations in the 32 bytes of I/O space even though the address lines will be valid.

$\overline{RD}$, ($\overline{CE}$*) - Read: A status output which indicates direction of data flow with respect to external or internal memory (a low level indicates a read from memory space). A read from internal memory or I/O will place data on the external data bus.

$\overline{WE}$** - Write Enable: An active low strobe pulse output for use in writing data to external RAM memory. A low level indicates valid data on the data bus.

DS** - Data Strobe: An output signal for use as a strobe pulse when address and data are valid. This output is used to transfer data to or from a peripheral or memory and occurs any time the Emulator reads or writes. DS is a continuous signal at fosc ÷ 2 when the Emulator is not in the WAIT or STOP mode.

FS** - Fetch Status: An output which indicates an op code fetch cycle

* $\overline{CE}$ and $\overline{RD}$ are used as $\overline{OE}$ (Output Enable) and $\overline{CE}$ (Chip Enable) signals, respectively in the Piggyback package.

** Not available in the Piggyback package.

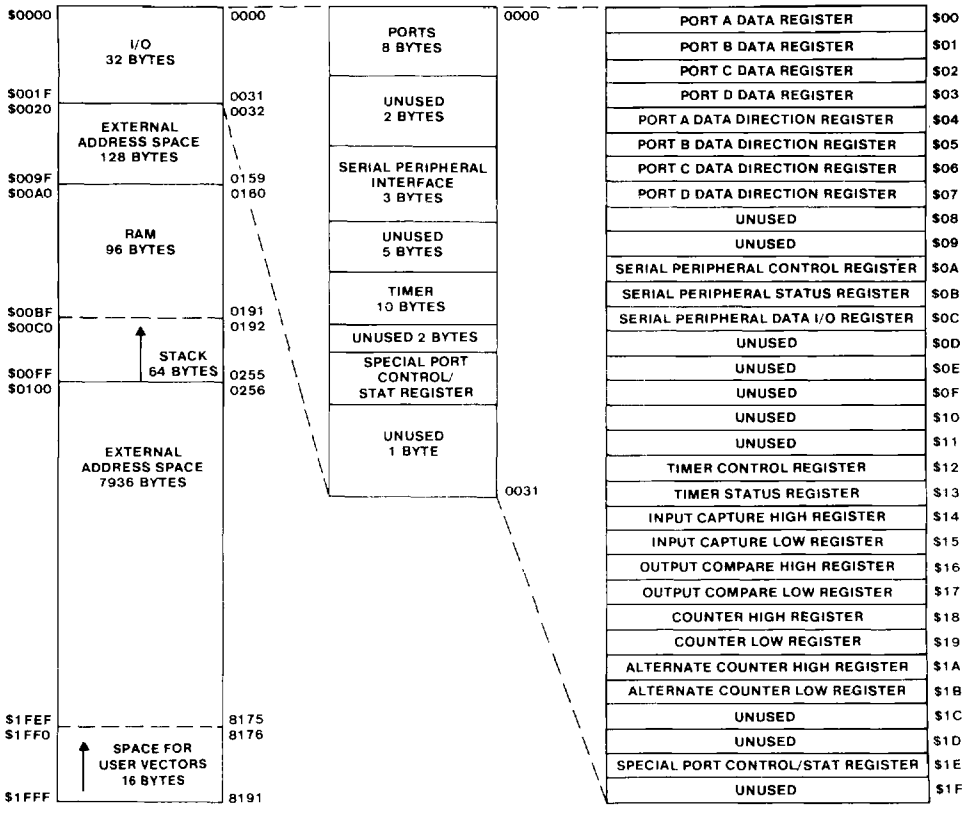


FIGURE 1. ADDRESS MAP.

$\overline{IRQ}$ (Maskable Interrupt Request)

Interrupt input trigger sensitivity is available as either 1) negative edge sensitive only, or 2) both negative edge sensitive and level sensitive triggering. In the latter case, either type of input to the $\overline{IRQ}$ pin will produce the interrupt. The Emulator completes the current instruction before it responds to the interrupt request. When the $\overline{IRQ}$ pin goes low for at least one tILIH as defined in the CDP68HC05D2 data sheet, a logic one is latched internally to signify that an interrupt has been requested. When the Emulator completes it's current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the Emulator then begins the interrupt sequence. The $\overline{IRQ}$ input requires an external resistor to VDD for "wire-OR" operation.

OSC1,OSC2

Oscillator (f_{OSC}) connections. Depending on the Emulator CPU oscillator type, which is fixed in hardware, the pins can be configured for either a crystal or ceramic resonator oscillator, or for an RC oscillator. Alternatively, with either CPU oscillator type*, an external clock may be used by applying the external clock signal to the OSC1 input with the OSC2 pin not connected. The internal clocks are derived by a divide by 2 of the oscillator frequency (f_{OSC}).

* The crystal/ceramic resonator CPU oscillator type is recommended to reduce loading on the external clock source.

READ CYCLE TIMING CDP68EM05D2 (Piggyback Emulator)
VDD = 5.0V ± 10%, VSS = 0V, T_A = 25°C

PARAMETER		LIMITS MIN	LIMITS MAX	UNITS
External Input Oscillator Pulse Width, Low or High	TCPL, TCPH	90	—	ns
Read Cycle	TRC	476	—	ns
Address Before $\overline{OE}$	TOA	50	—	ns
Access Time From $\overline{OE}$	TAO	—	200	ns
Access Time From Stable Address	TAA	—	350	ns
Access Time From $\overline{CE}$	TAA	—	350	ns
Data Bus Driven From $\overline{OE}$	TEX	0	—	ns
Address Hold Time After $\overline{OE}$	TAH	0	—	ns
Data Hold Time After Address	TOH	0	—	ns
Data Hold Time After $\overline{OE}$	TDH	0	—	ns
$\overline{OE}$ High to Data Bus not Driven	THZ	0	60	ns

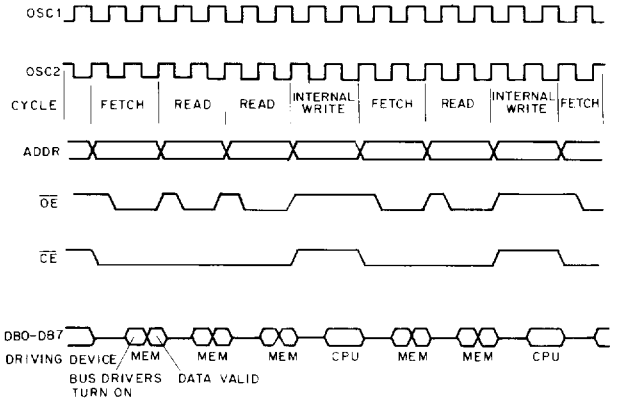


FIGURE 2. TYPICAL CYCLE TIMING FOR THE CDP68EM05D2 EMULATOR.

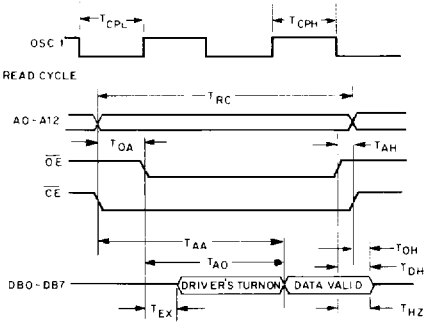


FIGURE 3. CONTROL TIMING DIAGRAM FOR THE CDP68EM05D2 EMULATOR.

READ CYCLE TIMING CDP68EM05D2N (PLCC Emulator)
VDD = 5.0V ± 10%, VSS = 0V, TA = 25°C

PARAMETER		LIMITS MIN	LIMITS MAX	UNITS
External Input Oscillator Pulse Width, Low or High	TCPL, TCPH	90	—	ns
Read Cycle	TRC	476	—	ns
Address Before Chip Enable	TCA	50	—	ns
Access Time From Chip Enable	TAC	—	200	ns
Access Time From Address	TAA	—	350	ns
Access Time From $\overline{RD}$	TAA	—	350	ns
Data Bus Driven From $\overline{CE}$	TEX	0	—	ns
Address Hold Time After $\overline{CE}$	TAH	0	—	ns
Data Hold Time After Address	TOH	0	—	ns
Data Hold Time After $\overline{CE}$	TDH	0	—	ns
$\overline{CE}$ High to Data Bus Not Driven	THZ	0	60	ns

WRITE CYCLE TIMING CDP68EM05D2N (PLCC Emulator)
VDD = 5.0V ± 10%, VSS = 0V, TA = 25°C

PARAMETER		LIMITS MIN	LIMITS MAX	UNITS
External Input Oscillator Pulse Width, Low or High	TCPL, TCPH	90	—	ns
Write Cycle	TWC	476	—	ns
Address Before $\overline{CE}$, $\overline{WE}$	TAS	50	—	ns
DS, $\overline{WE}$ Pulse Width	TDSP, TWP	200	—	ns
$\overline{WE}$ = L to CPU Driving Bus	TWHZ	0	—	ns
Data Set-Up Time	TDS	150	—	ns
Data Hold Time After $\overline{WE}$	TDH	50	—	ns
Address Valid After $\overline{WE}$	TWR	50	—	ns
$\overline{WE}$ High to Bus Not Driven	TDOZ	50	—	ns

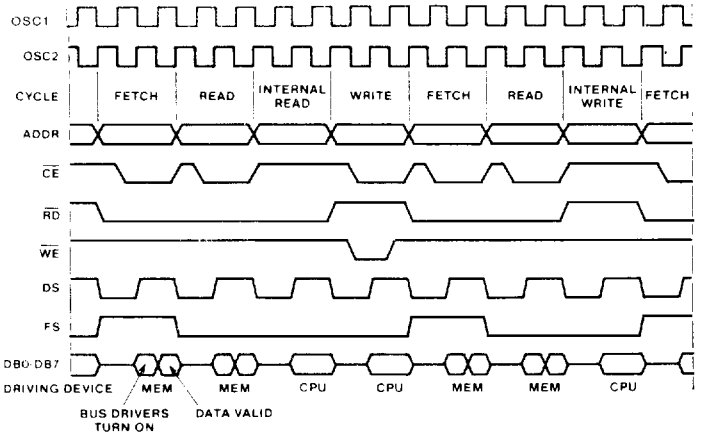


FIGURE 4. CDP68EM05D2N EMULATOR TYPICAL CYCLE TIMING.

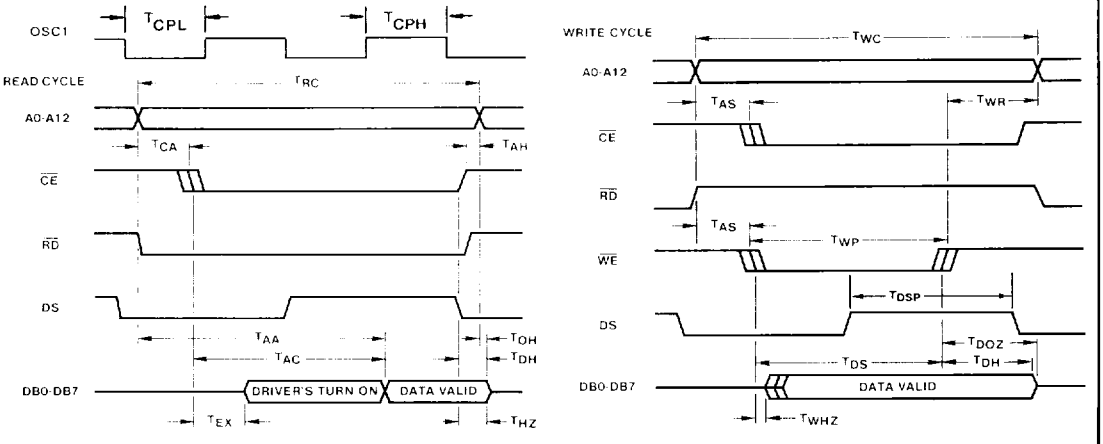


FIGURE 5. CDP68EM05D2N EMULATOR CONTROL TIMING DIAGRAMS.

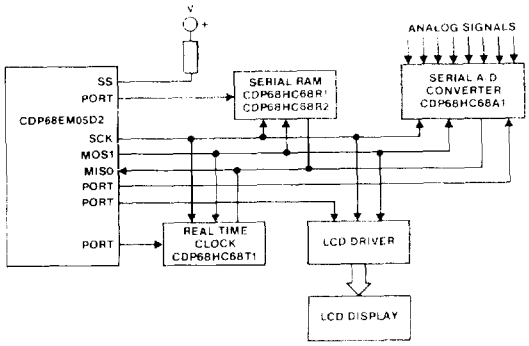


FIGURE 6. SERIAL PERIPHERAL INTERFACE (SPI) BUS SYSTEM.

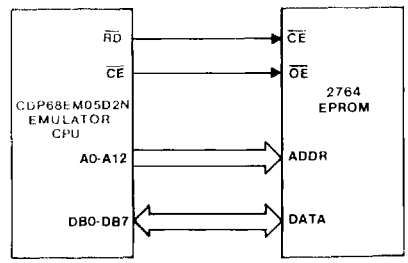


FIGURE 7. CDP68EM05D2N EMULATOR CONTROL TIMING DIAGRAMS.

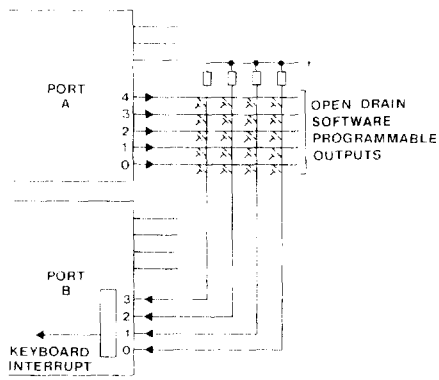


FIGURE 8. KEYBOARD INTERFACE TO ILLUSTRATE USE OF OPEN DRAIN OUTPUT PORT.

Customer Ordering Information

The eight available variations should be ordered by the following part number designations:

CDP68EM05D2EC, CDP68EM05D2NEC	Edge only sensitive interrupts with crystal or ceramic resonator oscillator network.
CDP68EM05D2ECF, CDP68EM05D2NECF	Edge only sensitive interrupts with external clock source, 2 Tcycle startup delay.
CDP68EM05D2ELC, CDP68EM05D2NELC	Edge and level sensitive interrupts with crystal or ceramic resonator oscillator network.
CDP68EM05D2ER, CDP68EM05D2NER	Edge only sensitive interrupts with resistor oscillator network.
CDP68EM05D2ERF, CDP68EM05D2NERF	Edge only sensitive interrupts with resistor oscillator, 2 Tcycle startup delay.
CDP68EM05D2LCF, CDP68EM05D2NLCF	Edge and level sensitive interrupts with external clock source, 2 Tcycle startup delay.
CDP68EM05D2LR, CDP68EM05D2NLR	Edge and level sensitive interrupts with resistor oscillator network.
CDP68EM05D2LRF, CDP68EM05D2NLRF	Edge and level sensitive interrupts with resistor oscillator, 2 Tcycle startup delay.