AT&T
Microelectronics

WE® DSP16A Digital Signal Processor

Features

- Pin- and instruction-compatible with the WE DSP16 Digital Signal Processor

- Low-power CMOS technology

- 25 ns, 33 ns, or 55 ns minimum instruction cycle

- 16-bit x 16-bit multiplication and 36-bit accumulation in one instruction cycle

- Two 36-bit accumulators

- Instruction cache for high-speed, ROM-efficient, repetitive operations

- A sleep state, awakened by interrupts, for low-power waiting

- Up to 24,576 words of program ROM and 2,048 words of data RAM (on-chip)

- Off-chip ROM expansion to 64K word

- Serial and parallel I/O ports with multiprocessor capability

- Maskable interrupts

- Single 5 V power supply

- Supported by WE DSP16A-SL Support Software Library and WE DSP16A-DS Digital Signal Processor Development System

Description

The WE DSP16A Digital Signal Processor is a 16-bit, high-speed, programmable integrated circuit. The device is fabricated in low-power CMOS technology and is packaged in an 84-pin, plastic leaded chip carrier (PLCC) or an 84-pin, fine pitch plastic quad flat pack (PQFP). The DSP16A device is a general-purpose building block that can be programmed to perform a wide variety of signal processing functions. It achieves high throughput without programming restrictions or latencies due to its parallel pipelined architecture. The processor has an arithmetic unit capable of a 16-bit x 16-bit multiplication and 36-bit accumulation or a 32-bit ALU operation in one instruction cycle. Data is supplied by two independent addressing units. The DSP16A device can function in a stand-alone manner, requiring only an external clock.
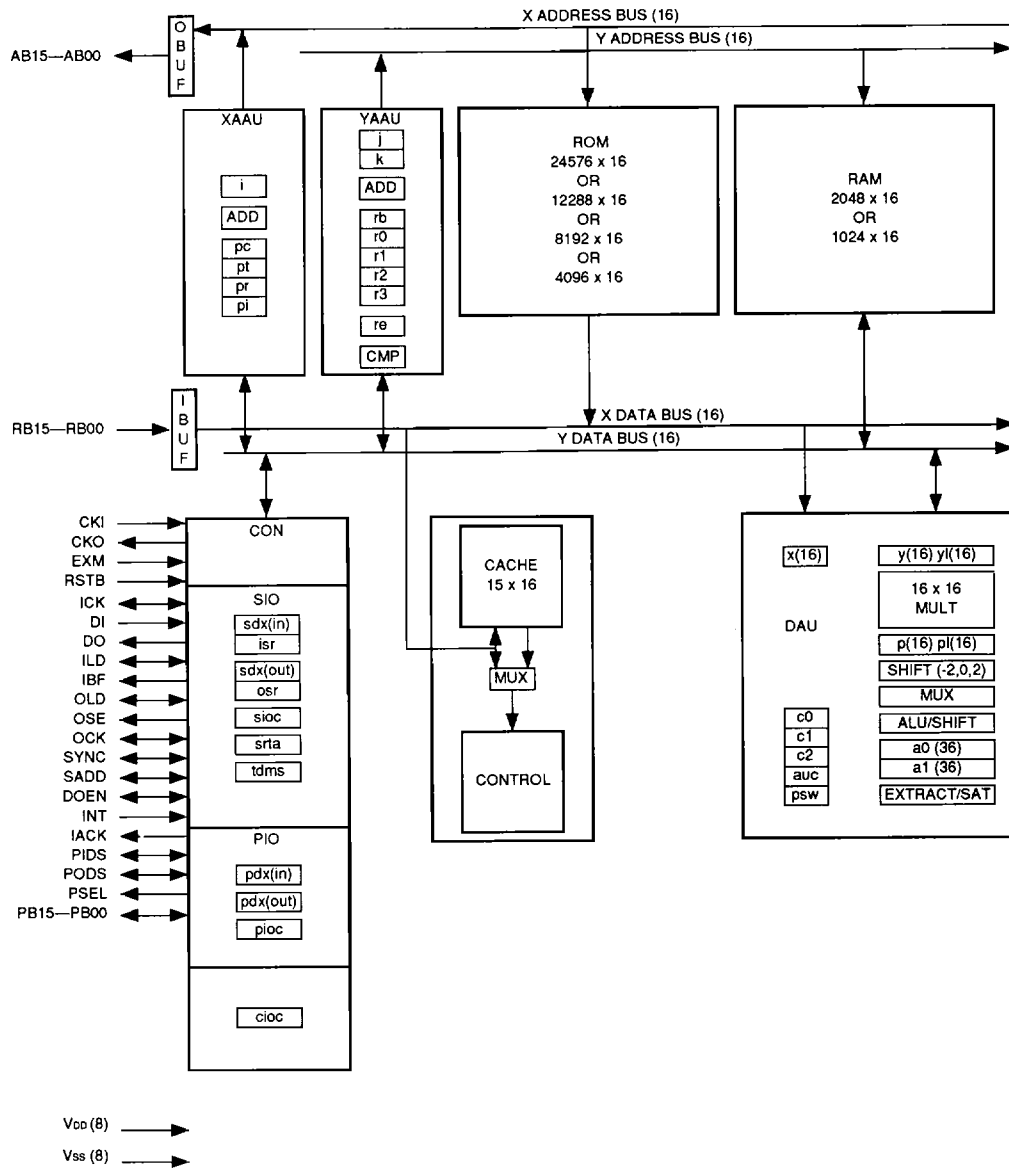
The DSP16A now contains up to 2 Kwords of data RAM and up to 24 Kwords of program ROM, much more than the DSP16 device's 512 word RAM and 2 Kword ROM. This allows larger programs that can fully utilize the high performance of the device, reducing the need for high-speed external memory. Pin, source code, and object code compatibility with the DSP16 device is maintained.

The newest issue of the DSP16A contains a SLEEP mode for low-power waiting, awakened by interrupts. In addition, the product register in the data arithmetic unit (DAU) is now directly readable and writeable with data move instructions.

Table of Contents

Contents   **Page**

Description (continued)

Legend:

Term	Definition	Term	Definition	Term	Definition
16 x 16 Mult	16-bit by 16-bit Multiplier	osr	Output Shift Register	rb	Modulo Addressing Register
a0—a1	Accumulators 0—1	p	p(High) DAU Register	re	Modulo Addressing Register
ADD	Adder	pc	Program Counter	ROM	Read-Only Memory
ALU/SHIFT	Arithmetic Logic Unit/Shifter	pdx(in)	Parallel I/O Data Transmit Input Register	sdx(in)	Serial Data Transmit Input Register
auc	Arithmetic Unit Control Register	pdx(out)	Parallel I/O Data Transmit Output Register	sdx(out)	Serial Data Transmit Output Register
c0—c2	Counters 0—2	pi	Program Interrupt Register	SIO	Serial I/O Unit
cioc	Sleep Control Register	PIO	Parallel I/O Unit	sioc	Serial I/O Control Register
CMP	Comparator	pioc	Parallel I/O Control Register	srta	Serial Receive/Transmit Address Register
DAU	Data Arithmetic Unit	pl	p(Low) DAU Register	tdms	Serial I/O Time-Division Multiplex Signal Control Register
i	Increment Register	pr	Program Return Register	x	Multiplier Input Register
isr	Input Shift Register	psw	Processor Status Word Register	XAAU	ROM Address Arithmetic Unit
j	Increment Register	pt	ROM Table Pointer	YAAU	RAM Address Arithmetic Unit
k	Increment Register	r0—r3	RAM Pointer Registers 0—3	yh	y(High) DAU Register
MUX	Multiplexer	RAM	Read/Write Memory	yl	y(Low) DAU Register

Note: See Table 3 for memory options and Table 2 for signal name definitions.

Figure 1. Block Diagram of the DSP16A

Pin Information
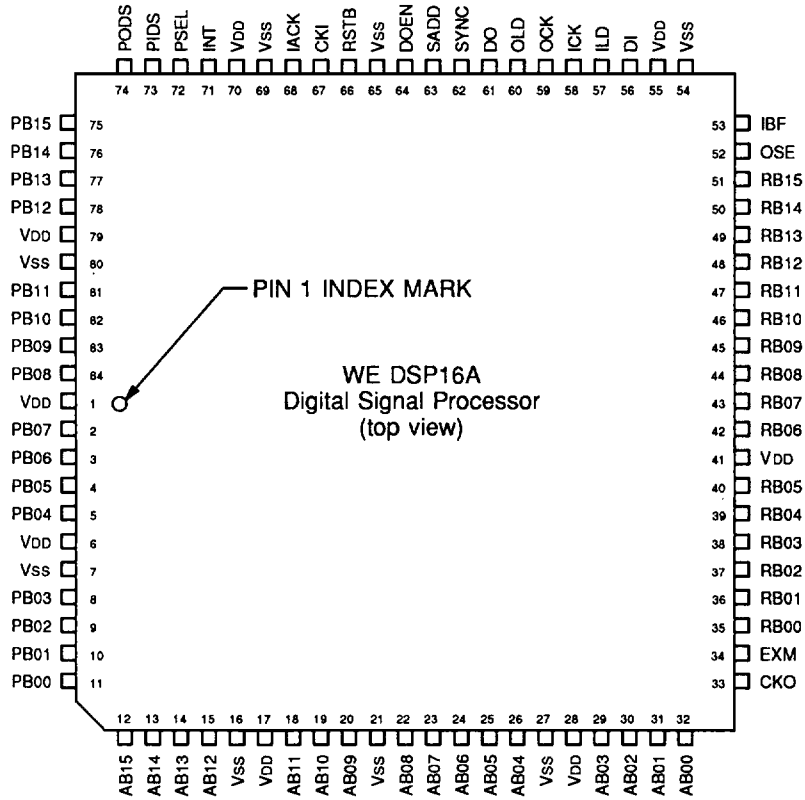
Figure 2. 84-pin PLCC Pin Diagram

Pin Information (continued)
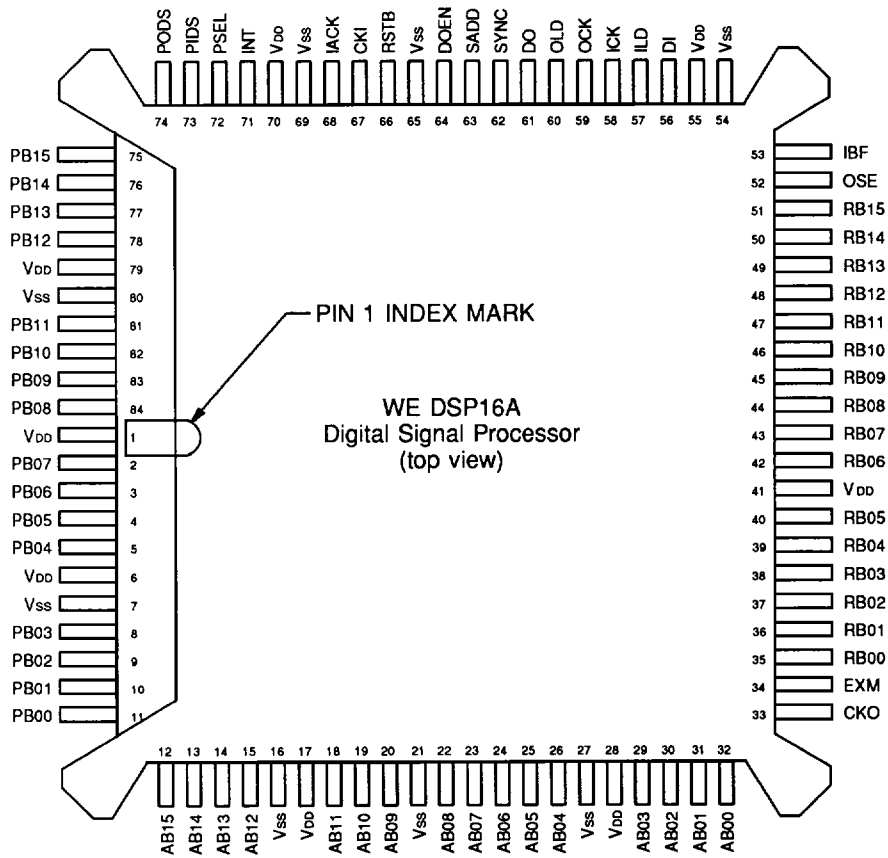
Figure 3. 84-pin PQFP Pin Diagram

Pin Information (continued)

Table 1. Pin Names in Alphabetical Order

Symbol	Pin	Symbol	Pin
AB00—AB15	32—29, 26—22, 20—18, 15—12	OLD	60
		OSE	52
CKI	67	PB00—PB15	11—8, 5—2, 84—81, 78—75
CKO	33		
DI	56		
DO	61	PIDS	73
DOEN	64	PODS	74
EXM	34	PSEL	72
IACK	68	RB00—RB15	35—40, 42—51
IBF	53	RSTB	66
ICK	58	SADD	63
ILD	57	SYNC	62
INT	71	VDD	1, 6, 17, 28, 41, 55, 70, 79
OCK	59	VSS	7, 16, 21, 27, 54, 65, 69, 80

Table 2. Pin Descriptions Grouped Functionally

Pin	Symbol	Type*	Name/Description
67	CKI	I	**Clock In.** Input clock at twice the frequency of internal operations.
66	RSTB	I	**Reset.** A high-to-low transition causes entry into the reset state. The sioc, pioc (except bit 3, which is set), tdms, rb, and re register bits are cleared. Reset clears external flags IACK and IBF and sets external flag OSE. DAU condition flags and the DAUC register are not affected by reset. All output and bidirectional pins are 3-stated during reset. A low-to-high transition causes execution to begin at ROM location 0.
12	AB15	O†	**ROM Address Bus — Bit 15.**
13	AB14		**ROM Address Bus — Bit 14.**
14	AB13		**ROM Address Bus — Bit 13.**
15	AB12		**ROM Address Bus — Bit 12.**
18	AB11		**ROM Address Bus — Bit 11.**
19	AB10		**ROM Address Bus — Bit 10.**
20	AB09		**ROM Address Bus — Bit 9.**
22	AB08		**ROM Address Bus — Bit 8.**
23	AB07		**ROM Address Bus — Bit 7.**
24	AB06		**ROM Address Bus — Bit 6.**
25	AB05		**ROM Address Bus — Bit 5.**
26	AB04		**ROM Address Bus — Bit 4.**
29	AB03		**ROM Address Bus — Bit 3.**

* I = Input; O = Output.
† Indicates 3-state condition.

Pin Information (continued)

Table 2. Pin Descriptions Grouped Functionally (continued)

Pin	Symbol	Type*	Name/Description
30	AB02	O†	ROM Address Bus — Bit 2.
31	AB01		ROM Address Bus — Bit 1.
32	AB00		ROM Address Bus — Bit 0.
35	RB00	I	ROM Data Bus — Bit 0.
36	RB01		ROM Data Bus — Bit 1.
37	RB02		ROM Data Bus — Bit 2.
38	RB03		ROM Data Bus — Bit 3.
39	RB04		ROM Data Bus — Bit 4.
40	RB05		ROM Data Bus — Bit 5.
42	RB06		ROM Data Bus — Bit 6.
43	RB07		ROM Data Bus — Bit 7.
44	RB08		ROM Data Bus — Bit 8.
45	RB09		ROM Data Bus — Bit 9.
46	RB10		ROM Data Bus — Bit 10.
47	RB11		ROM Data Bus — Bit 11.
48	RB12		ROM Data Bus — Bit 12.
49	RB13		ROM Data Bus — Bit 13.
50	RB14		ROM Data Bus — Bit 14.
51	RB15		ROM Data Bus — Bit 15.
34	EXM	I	**External Memory.** When EXM is high, instructions and coefficients are fetched from external ROM (internal ROM disabled). If EXM is low, internal ROM is accessed; only for addresses outside of the internal ROM is the external memory interface selected.
33	CKO	O†	**Clock Out.** Buffered clock at half the frequency of CKI.
71	INT	I	**Processor Interrupt.** Interrupt to DSP16A. INT is acknowledged when the interrupt is enabled by the pioc register.
68	IACK	O†	**Interrupt Acknowledge.** Interrupt acknowledge signals when an interrupt is being serviced by the DSP16A. The IACK remains high until normal instruction operation resumes.
73	PIDS	I/O†	**Parallel Input Data Strobe (Active-Low).** In active mode, PIDS is an output. When PIDS is asserted, data may be placed onto the PDB. Upon negation of PIDS, data should be removed from the PDB. PIDS is asserted by the DSP16A device during an active mode read transaction. In passive mode, PIDS is an input. When asserted by an external device, this signal indicates that data is available on the PDB. In both active and passive modes, the trailing edge (low-to-high transition) of PIDS is the sampling point.
74	PODS	I/O†	**Parallel Output Data Strobe (Active-Low).** In active mode, PODS is an output. When PODS is asserted, data is available on the PDB. PODS is asserted by the DSP16A device during an active mode write transaction. In passive mode, PODS is an input. When PODS is asserted by an external device, the DSP16A device places the contents of its parallel output register (pdx0 or pdx1) onto the PDB. When the Parallel I/O is in the status/control mode (pioc bit 10), only PB07—PB00 are enabled upon a PODS assertion (active or passive) and PB15—PB08 remain 3-stated.

* I = Input; O = Output.
† Indicates 3-state condition.

Pin Information (continued)

Table 2. Pin Descriptions Grouped Functionally (continued)

Pin	Symbol	Type*	Name/Description
72	PSEL	O†	**Peripheral Select.** PSEL is used to specify the logical port to/from which data is to be conveyed. PSEL is high (1) when pdx1 is the register specified in the I/O instruction and low when pdx0 is the register specified.
75	PB15	I/O†	**Parallel I/O Data Bus — Bit 15.**
76	PB14		**Parallel I/O Data Bus — Bit 14.**
77	PB13		**Parallel I/O Data Bus — Bit 13.**
78	PB12		**Parallel I/O Data Bus — Bit 12.**
81	PB11		**Parallel I/O Data Bus — Bit 11.**
82	PB10		**Parallel I/O Data Bus — Bit 10.**
83	PB09		**Parallel I/O Data Bus — Bit 9.**
84	PB08		**Parallel I/O Data Bus — Bit 8.**
2	PB07		**Parallel I/O Data Bus — Bit 7.**
3	PB06		**Parallel I/O Data Bus — Bit 6.**
4	PB05		**Parallel I/O Data Bus — Bit 5.**
5	PB04		**Parallel I/O Data Bus — Bit 4.**
8	PB03		**Parallel I/O Data Bus — Bit 3.**
9	PB02		**Parallel I/O Data Bus — Bit 2.**
10	PB01		**Parallel I/O Data Bus — Bit 1.**
11	PB00		**Parallel I/O Data Bus — Bit 0.**
56	DI	I	**Data Input.** Serial data input latched on rising edge of ICK, either LSB or MSB first, according to the sioc register MSB field.
58	ICK	I/O†	**Input Clock.** Clock for serial input data. In active mode, ICK is an output; in passive mode, ICK is an input, according to the sioc ICK field.
57	ILD	I/O†	**Input Load.** Falling edge of ILD indicates the beginning of a serial input word. In active mode, ILD is an output; in passive mode, ILD is an input, according to the sioc register ILD field.
53	IBF	O†	**Input Buffer Full.** IBF is asserted when the input buffer is filled and is then negated by a read of the buffer. IBF is also negated by asserting RSTB.
61	DO	O†	**Data Output.** Serial data output from the output shift register (osr), either LSB or MSB first, according to the sioc register MSB field. DO changes on the rising edges of OCK. DO is 3-stated when DOEN is high.
59	OCK	I/O†	**Output Clock.** Clock for serial output data. In active mode, OCK is an output; in passive mode, OCK is an input, according to the sioc register OCK field.
60	OLD	I/O†	**Output Load.** Clock for loading the parallel-to-serial converter from the output buffer (obuf). A falling edge of OLD indicates the beginning of a serial output word. In active mode, OLD is an output; in passive mode, OLD is an input, according to the sioc register OLD field.
52	OSE	O†	**Output Shift Register Empty.** Indicates the end of a serial transmission. OSE is set either by emptying the output shift register or by asserting RSTB. OSE is reset by the DSP16A writing a word (two clock cycles after the falling edge of OLD) to the output shift register. If no new word is written by the DSP16A, OSE remains high regardless of activity on OLD.

* I = Input; O = Output.
† Indicates 3-state condition.

Pin Information (continued)

Table 2. Pin Descriptions Grouped Functionally (continued)

Pin	Symbol	Type*	Name/Description
64	DOEN	I/O†	**Data Output Enable (Active-Low).** An input, when not in the multiprocessor mode. DO and SADD are enabled only if DOEN is low. DOEN is an output when in the multiprocessor mode (tdms register MODE field set). In the multiprocessor mode, DOEN indicates a valid time slot for a serial output.
62	SYNC	I/O†	**Multiprocessor Synchronization.** Typically used in the multiprocessor mode. A falling edge of SYNC indicates the first word of a TDM I/O stream and causes the resynchronization of the active ILD and OLD generators. SYNC is an output when the tdms register SYNC field is set; otherwise, it is an input. SYNC must be tied low if it is not used as an output. When used as an output, SYNC = ILD/OLD + 8 or 16, depending on the setting of the SYNCSP field of the tdms register. This procedure can be used to generate a slow clock for SIO operation.
63	SADD	I/O†	**Serial Address.** When not in multiprocessor mode, SADD is the inverted 8-bit serial transmit address output from the serial receive/transmit address (srta) register, LSB first. SADD changes on the rising edges of ICK or OCK (see sioc, LD field). SADD is 3-stated when DOEN is high. In multiprocessor mode, SADD is an output when the tdms time slot dictates a serial output transmission; otherwise, it is an input. While an output, SADD is the inverted 8-bit serial transmit address output from the srta register, LSB first. SADD changes on the rising edges of ICK or OCK (see sioc, LD field). While an input, SADD is inverted and latched on the rising edge of ICK or OCK (see sioc, LD field) and compared against the serial receive address in the srta register to determine if input data on DI is loaded from the input shift register (isr) into sdx(in).
1	V$_{DD}$	P	**5 V Supply.**
6	V$_{DD}$		**5 V Supply.**
17	V$_{DD}$		**5 V Supply.**
28	V$_{DD}$		**5 V Supply.**
41	V$_{DD}$		**5 V Supply.**
55	V$_{DD}$		**5 V Supply.**
70	V$_{DD}$		**5 V Supply.**
79	V$_{DD}$		**5 V Supply.**
7	V$_{SS}$	P	**Ground.**
16	V$_{SS}$		**Ground.**
21	V$_{SS}$		**Ground.**
27	V$_{SS}$		**Ground.**
54	V$_{SS}$		**Ground.**
65	V$_{SS}$		**Ground.**
69	V$_{SS}$		**Ground.**
80	V$_{SS}$		**Ground.**

* I = Input; O = Output; P = Power Supply.
† Indicates 3-state condition.

Architectural Information

Overview

The DSP16A device contains a data arithmetic unit (DAU) that performs signal processing arithmetic, a ROM address arithmetic unit (XAAU), a RAM address arithmetic unit (YAAU), up to a 24,576 x 16-bit ROM that contains program instructions and fixed data, up to a 2,048 x 16-bit RAM for variable data, an instruction cache (CACHE), a serial I/O unit (SIO), and a 16-bit parallel I/O unit (PIO).

Arithmetic Unit

The arithmetic unit contains a 16-bit x 16-bit parallel multiplier that generates a full 32-bit product in one instruction cycle. The product can be accumulated with one of two 36-bit accumulators. The data in these accumulators can be directly loaded from or stored to memory in two 16-bit words with automatic saturation on overflow. The ALU supports a full set of arithmetic and logical operations on either 16-bit or 32-bit data. A standard set of ALU conditions can be tested for conditional ALU operations, branches, and subroutine calls. This procedure allows the processor to perform as a powerful 16-bit or 32-bit microprocessor for logical and control applications.

Addressing Units

Two addressing units support high-speed, register-indirect memory addressing with postmodification of the register. Direct and immediate addressing is supported at the cost of only one additional instruction cycle and ROM location. Four address registers in the YAAU (r0—r3) can be used for either read or write addresses to the RAM without restrictions. Registers j and k provide user-defined post-increments for the addresses. Fixed increments of +1, −1, and +2 are also available. The YAAU also supports a flexible modulo addressing mode for efficient filter implementations. Registers rb and re are used to define the beginning and end of the modulo. Four compound addressing modes are provided to make read/write operations more efficient. In the XAAU, the register pt is used for ROM table look-up, and register i is used to hold a user-defined post-increment. A fixed post-increment of +1 is also available. Register pc is the program counter. Registers pr and pi hold the return address for subroutine calls and interrupts, respectively.

On-Chip Memory

The on-chip memory includes up to 24,576 x 16-bit words of ROM and up to 2,048 x 16-bit words of RAM. The on-chip ROM can be augmented with up to 60 Kwords of external memory or can be replaced by up to 64 Kwords of external memory for prototyping or for applications that require a large program space or frequent modification. When the internal ROM is selected by the EXM pin and a memory location outside of the internal ROM is accessed, the external memory interface is automatically selected.

Table 3. Memory Options Available

Device	Data RAM	Program ROM	ROM Augmentation Boundary
DSP16A0X	2,048 x 16	4,096 x 16	4,096
DSP16A1X	2,048 x 16	12,288 x 16	12,288
DSP16A2X	1,024 x 16	4,096 x 16	8,192
DSP16A3X	1,024 x 16	8,192 x 16	8,192
DSP16A4X	2,048 x 16	24,576 x 16	24,576

Instruction Cache

An on-chip memory cache can be selectively used to store such repetitive operations as those found in a filter section. Up to 15 words in the cache can be repeated up to 127 times with no looping overhead. In addition, operations in the cache that require a ROM access (for example, reading fixed coefficients) execute at twice the normal rate. The cache greatly reduces the need for writing repetitive code in-line and, therefore, conserves ROM storage.

Architectural Information (continued)

Serial and Parallel I/O Ports

The DSP16A device has both serial and parallel I/O ports. The serial I/O unit is an asynchronous, full-duplex, double-buffered channel that operates at up to 20 Mbits/s and easily interfaces with other DSP16A devices in a multiple DSP16A environment. Commercially available codecs and time division multiplex (TDM) channels can be interfaced to the DSP16A device with few (if any) additional components. The parallel I/O unit is capable of interfacing to a 16-bit bus containing other DSP16A devices, microprocessors, or peripheral I/O devices. Data rates of up to 40 Mbytes/s are obtainable through this port.

Interrupts

The DSP16A device has a maskable interrupt that can be generated by the user or by any of four I/O conditions: input buffer full (IBF), output buffer empty (OBE), parallel input data strobe (PIDS), and parallel output data strobe (PODS). Note that branch instructions and cache operations are protected from interrupts.

Low-Power Sleep Mode

The DSP16A has a sleep state that reduces power when the device is waiting. This is implemented by stopping the internal processor clock when a 1 is written to the SLEEP bit in the CIOC register. An interrupt awakens the device, restarting the clock to the internal processor. The external INT, SIO, and PIO remain active during this sleep state to generate the interrupts that awaken the device. Four NOPs need to be placed after the write to CIOC with the SLEEP bit set in order to ensure that the processor is inactive when going to sleep. The processor will stop on the the second NOP after the write to CIOC, and then execute the third and fourth NOPs after an interrupt awakens the processor but before the jump to address one. Remember that cache operations cannot be interrupted; hence, the SLEEP bit in the CIOC register should not be written to from a cache operation.

Programming Information

Instruction Set

The DSP16A processor has five types of instructions: multiply/ALU, special function, control, cache, and data move. The multiply/ALU instructions are the primary instructions used to implement signal processing algorithms. Statements from this group can be combined to generate multiply/accumulate, logical, and other ALU functions and to transfer data between memory and registers in the data arithmetic unit. The special function instructions can be conditionally executed based on flags from the previous ALU operation, the condition of one of the counters, or the value of a randomly set bit in the DSP16A device. The control instructions implement the goto and call commands. Control instructions can also be executed conditionally. Cache instructions are used to implement low-overhead loops, conserve program memory, and decrease the execution time of certain multiply/ALU instructions. Data move instructions are used to transfer data between memory and registers or between accumulators and registers.

The following operators are used in describing the instruction set:

*	16-bit x 16-bit → 32-bit multiplication (Denotes register-indirect addressing when used as a prefix to an address register)
+	36-bit addition
−	36-bit subtraction
>>	Arithmetic right shift
<<	Logical left shift
|	32-bit bitwise OR
&	32-bit bitwise AND
^	32-bit bitwise EXCLUSIVE OR
:	Compound address swapping

Programming Information (continued)

Multiply/ALU Instructions

Note that the function statements and transfer statements in Table 4 are chosen independently. Any function statement may be combined with any transfer statement to form a valid muliply/ALU instruction. If either statement is not required, a single statement from either column constitutes a valid instruction. The number of cycles to execute the instruction is a function of the transfer column. (An instruction with no transfer statement executes in one instruction cycle.) All multiply/ALU instructions require one word of program memory. The no operation (NOP) instruction is a special case encoding of a multiply/ALU instruction and executes in one cycle. The assembly language representation of a NOP is either NOP or a single semicolon.

Table 4. Multiply/ALU Instructions

Function Statements		Transfer		
		Statements[1]		Cycles Out/In Cache
	p=x*y	y=Y	x=X	2/1
aD=p	p=x*y	y=aT	x=X	2/1
aD=aS+p	p=x*y	y[l]=Y		1/1
aD=aS–p	p=x*y	aT[l]=Y		1/1
aD=p		x=Y		1/1
aD=aS+p		Y		1/1
aD=aS–p		Y=y[l]		2/2
aD=y		Y=aT[l]		2/2
aD=aS+y		Z: y	x=X	2/2
aD=aS–y		Z: y[l]		2/2
aD=aS&y		Z: aT[l]		2/2
aD=aS|y				
aD=aS^y				
aS–y				
aS&y				

1. Brackets, [ ], indicate an optional argument and are not part of the instruction syntax. The [l] argument designates the low 16 bits of aT or y.

Table 5. Replacement Table for Multiply/ALU Instructions

Replace	Value[1]	Description
aD, aS, aT	a0, a1	One of two DAU accumulators.
X	*pt++, *pt++i	ROM location pointed to by pt. pt is postmodified by +1 and i, respectively.
Y	*rM, *rM++, rM– –, *rM++j	RAM location pointed to by rM (M = 0, 1, 2, 3). rM is postmodified by 0,+1,–1, or j, respectively.
Z	*rMzp, *rMpz, *rMm2, *rMjk	Read/write compound addressing. rM (M = 0, 1, 2, 3) is used twice. First, postmodified by 0, +1, –1, or j, respectively and, second, postmodified by +1, 0, +2, or k, respectively.

1. When loading the upper half of a0, a1, or y, the lower half of the register is cleared if the corresponding CLR bit in the AUC register is zero (see the Register Settings section).

Programming Information (continued)

Special Function Instructions

All forms of the special function instructions execute in one instruction cycle and require one word of program memory:

$$
\left.\begin{array}{l}
\text{aD = aS >> 1} \\
\text{aD = aS >> 4} \\
\text{aD = aS >> 8} \\
\text{aD = aS >> 16}
\end{array}\right\} \quad \text{Arithmetic right shift (sign preserved) of 36-bit accumulators}
$$

aD = aS
aD = -aS
aD = rnd(aS)   — Round upper 20 bits of accumulator
aDh = aSh+1   — Increment upper half of accumulator (lower half cleared)
aD = aS+1   — Increment accumulator
aD = y
aD = p

$$
\left.\begin{array}{l}
\text{aD = aS << 1} \\
\text{aD = aS << 4} \\
\text{aD = aS << 8} \\
\text{aD = aS << 16}
\end{array}\right\} \quad \begin{array}{l} \text{Logical left shift (sign not preserved) of the lower 32 bits of accumulators} \\ \text{(upper 4 bits are sign-bit-extended from bit 31 at the completion of the shift)} \end{array}
$$

The above special functions can be conditionally executed with an

> if CON instruction

and with an event counter

> ifc CON instruction

which means:

> if CON is true then
>
> > $c1 = c1 + 1$
> >
> > instruction
> >
> > $c2 = c1$
>
> else
>
> > $c1 = c1 + 1$

Table 6. Replacement Table for Special Function Instructions

Replace	Value	Description
aD, aS	a0, a1	One of two DAU accumulators
CON	mi, pl, eq, ne, gt, le, lvs, lvc, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false	See Table 8 for definitions of mnemonics.

Programming Information (continued)

Control Instructions

All unconditional control instructions (except icall) execute in two instruction cycles and require one word of program memory; conditional control instructions execute in three instruction cycles and require two words of program memory. The icall instruction requires one word of program memory and three instruction cycles to execute. Control instructions may not be executed inside the cache.

```
goto JA
goto pt
call JA
call pt
icall
return      (goto pr)
ireturn     (goto pi)
```

The above control instructions, with the exception of ireturn and icall, can be conditionally executed. For example:

```
If CON goto JA
```

Table 7. Replacement Table for Control Instructions

Replace	Value	Description
CON	mi, pl, eq, ne, gt, le, lvs, lvc, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false	See Table 8 for definitions of mnemonics.
JA	12-bit value	Least significant 12 bits of absolute address within the same 4 Kword memory section.

Conditional Mnemonics

Table 8 lists mnemonics used in conditional execution of special function and control instructions.

Table 8. DSP16A Conditional Mnemonics

Test	Description	Test	Description
pl	Result is nonnegative (sign bit is bit 35).	mi	Result is negative.
eq	Result is equal to zero.	ne	Result is not equal to zero.
gt	Result is greater than zero.	le	Result is less than or equal to zero.
lvs	Logical overflow set.*	lvc	Logical overflow clear.
mvs	Mathematical overflow.†	mvc	Mathematical overflow clear.
c0ge	Counter 0 greater than or equal to zero.	c0lt	Counter 0 less than zero.
c1ge	Counter 1 greater than or equal to zero.	c1lt	Counter 1 less than zero.
heads	Pseudorandom sequence bit set.	tails	Pseudorandom sequence bit clear.
true	The condition is always satisfied in an if instruction.	false	The condition is never satisfied in an if instruction.

* Result is not representable in the 36-bit accumulators (36-bit overflow).
† Bits 35—31 are not the same (32-bit overflow).
Notes:
Testing the state of the counters (c0 or c1) automatically increments the counter by one.

The 10-bit pseudorandom sequence is reset by writing the pi register (writing to the pi register will not affect its contents except during interrupt service routines).

Programming Information (continued)

Cache Instructions

Cache instructions require one word of program memory. The do instruction executes in one instruction cycle; the redo instruction executes in two instruction cycles. Control instructions and immediate loads of non-YAAU registers may not be executed inside the cache. The instruction formats are as follows:

```
do K {
        inst1
        instr2
        .
        .
        .
        instrNI
        }
redo K
```

Table 9. Replacement Table for Cache Instructions

Replace	Value	Description
K	$2 \leq K \leq 127$	Number of times the instructions are to be executed.
NI	$1 \leq NI \leq 15$	1 to 15 instructions may be included.

When the cache is used to execute a block of instructions, the cycle timings of the instructions are as follows:

1. The first pass will not affect cycle timings except for the last instruction in the block of instructions. This instruction will execute in two cycles.

2. During the second through the K–1 pass, each instruction is executed in the cache. (See multiply/ALU instructions.)

3. During the last (K) pass, the block of instructions executes inside the cache, except for the last instruction which executes outside the cache.

Programming Information (continued)

Data Move Instructions

Data move instructions execute in two instruction cycles. Immediate data move instructions require two words of program memory; all other data move instructions require only one word. The only exception to these statements is a special case immediate load (short immediate) instruction. If a YAAU register is loaded with a 9-bit or smaller value, the instruction requires only one word of memory and executes in one instruction cycle. All data move instructions except immediate loads of non-YAAU registers may be executed from within the cache. The data move instructions are as follows:

R = N	aT = R
R = M	Y = R
R = Y	Z : R
R = aS	

Table 10. Replacement Table for Data Move Instructions

Replace	Value[1]	Description[2,3]
R	x, y,p	DAU registers — signed, 16 bits
	yl,pl	DAU registers — unsigned, 16 bits
	auc	DAU control register — unsigned, 7 bits
	c0, c1, c2	DAU counters — signed, 8 bits
	r0, r1, r2, r3	YAAU pointer registers — unsigned, 16 bits
	rb, re	YAAU modulo addressing registers — unsigned, 16 bits
	j, k	YAAU increment registers — signed, 16 bits
	pt	XAAU pointer register — unsigned, 16 bits
	pr, pi	XAAU program return registers— unsigned, 16 bits[4]
	i	XAAU increment register — signed, 12 bits
	psw	Processor status word.
	sioc	Serial I/O control register.
	sdx	Serial I/O data register.
	tdms	Serial I/O TDMS control register.
	srta	Serial receive/transmit address.
	pioc	Parallel I/O control register.
	pdx0	Parallel I/O data register with PSEL = 0 (pin 72).
	pdx1	Parallel I/O data register with PSEL = 1 (pin 72).
	cioc	Sleep control register.
aD, aS, aT	a0, a1	High half of accumulator.
Y	*rM, *rM++, *rM– –, *rM++j	Same as in multiply/ALU instructions.
Z	*rmZp,**rMpz, *rMm2, *rMjk,	Same as in multiply/ALU instructions.
N	16-bit value	Immediate data.
M	9-bit value	Immediate data for YAAU registers.

1. sioc, tdms, and srta registers are not readable.
2. When signed registers less than 16 bits wide are read, their contents are sign-extended to 16 bits. When unsigned registers less than 16 bits wide are read, their contents are zero-extended to 16 bits.
3. Loading an accumulator with a data move instruction does not affect the flags.
4. The pi register acts as a shadow of the pc register. Writes to pi will not alter its contents except during interrupt service routines (shadowing is disabled during ISRs).

Register Settings

Table 11 through Table 17 show how to set various operating conditions for the DSP16A device.

Serial I/O Control (SIOC) Register

Table 11. Serial I/O Control (SIOC) Register

Bit	9	8	7	6	5	4	3	2	1	0
Field	LD	CLK		MSB	OLD	ILD	OCK	ICK	OLEN	ILEN

Field	Value	Description
LD	0	Active ILD/OLD = ICK + 16, active SYNC = ICK + 128/256*.
	1	Active ILD/OLD = OCK + 16, active SYNC = OCK + 128/256*.
CLK	0 0	Active clock = CKI + 4.
	0 1	Active clock = CKI + 12.
	1 0	Active clock = CKI + 16.
	1 1	Active clock = CKI + 20.
MSB	0	LSB first.
	1	MSB first (bit order is reversed when reading/writing sdx).
OLD	0	OLD is an input (passive mode).
	1	OLD is an output (active mode).
ILD	0	ILD is an input (passive mode).
	1	ILD is an output (active mode).
OCK	0	OCK is an input (passive mode).
	1	OCK is an output (active mode).
ICK	0	ICK is an input (passive mode).
	1	ICK is an output (active mode).
OLEN	0	16-bit output.
	1	8-bit output.
ILEN	0	16-bit input.
	1	8-bit input.

* See tdms register, SYNC field.

Register Settings (continued)

Time-Division Multiplex Slot (TDMS) Register

Table 12. Time-Division Multiplex Slot (TDMS) Register

Bit	9	8	7	6	5	4	3	2	1	0
Field	SYNCSP	MODE			TRANSMIT SLOT					SYNC

Field	Value*	Description
SYNCSP	0	SYNC = ICK/OCK† + 128.‡
	1	SYNC = ICK/OCK† + 256.
MODE	0	Multiprocessor mode off; DOEN is an input (passive mode).
	1	Multiprocessor mode on; DOEN is an output (active mode).
TRANSMIT SLOT	1xxxxxx	Transmit slot 7.
	x1xxxxx	Transmit slot 6.
	xx1xxxx	Transmit slot 5.
	xxx1xxx	Transmit slot 4.
	xxxx1xx	Transmit slot 3.
	xxxxx1x	Transmit slot 2.
	xxxxxx1	Transmit slot 1.
SYNC	1	Transmit slot 0, SYNC is an output (active mode).
	0	SYNC is an input (passive mode).

* x is don't care.
† See sioc register, LD field.
‡ Select this mode when in multiprocessor mode.

Register Settings (continued)

Serial Receive/Transmit Address (SRTA) Register

Table 13. Serial Receive/Transmit Address (SRTA) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field		RECEIVE ADDRESS								TRANSMIT ADDRESS						

Field	Value*	Description
RECEIVE ADDRESS	1xxxxxxx	Receive address 7.
	x1xxxxxx	Receive address 6.
	xx1xxxxx	Receive address 5.
	xxx1xxxx	Receive address 4.
	xxxx1xxx	Receive address 3.
	xxxxx1xx	Receive address 2.
	xxxxxx1x	Receive address 1.
	xxxxxxx1	Receive address 0.
TRANSMIT ADDRESS	1xxxxxxx	Transmit address 7.
	x1xxxxxx	Transmit address 6.
	xx1xxxxx	Transmit address 5.
	xxx1xxxx	Transmit address 4.
	xxxx1xxx	Transmit address 3.
	xxxxx1xx	Transmit address 2.
	xxxxxx1x	Transmit address 1.
	xxxxxxx1	Transmit address 0.

*   x is don't care.

Sleep Control (CIOC) Register

Table 14. Sleep Control (CIOC) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RES			SLEEP	RES											

Field	Value*	Description
RES	xxx	Reserved.
SLEEP	0	Normal operation.
	1	Processor clock stopped until interrupted.
RES	xxxx xxxx xxxx	Reserved.

*   x is don't care.

Register Settings (continued)

Processor Status Word (PSW) Register

Table 15. Processor Status Word (PSW) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	DAU Flags				X	X	a1[V]	a1[35—32]				a0[V]	a0[35—32]			

Field	Value*	Description
DAU Flags	Wxxx	LMI — logical minus when set.
	xWxx	LEQ — logical equal when set.
	xxWx	LLV — logical overflow when set.
	xxxW	LMV — mathematical overflow when set.
a1[V]	W	Accumulator 1 (a1) overflow when set.
da1[35—32]	Wxxx	Accumulator 1 (a1) bit 35.
	xWxx	Accumulator 1 (a1) bit 34.
	xxWx	Accumulator 1 (a1) bit 33.
	xxxW	Accumulator 1 (a1) bit 32.
a0[V]	W	Accumulator 0 (a0) overflow when set.
da0[35—32]	Wxxx	Accumulator 0 (a0) bit 35.
	xWxx	Accumulator 0 (a0) bit 34.
	xxWx	Accumulator 0 (a0) bit 33.
	xxxW	Accumulator 0 (a0) bit 32.

* x is don't care; W is write only.

Arithmetic Unit Control (AUC) Register

Table 16. Arithmetic Unit Control (AUC) Register

Bit	6	5	4	3	2	1	0
Field	CLR			SAT		ALIGN	

Field	Value*	Description
CLR	1xx	Clearing yl is disabled (enabled when 0).
	x1x	Clearing a1l is disabled (enabled when 0).
	xx1	Clearing a0l is disabled (enabled when 0).
SAT	1x	a1 saturation on overflow is disabled (enabled when 0).
	x1	a0 saturation on overflow is disabled (enabled when 0).
ALIGN	00	Product register unshifted when used in multiply/ALU instructions $aD = p$, $aD = aS + p$, $aD = aS - p$.
	01	Product register shifted right 2 when used in multiply/ALU instructions $aD = p + 4$, $aD = aS + (p + 4)$, $aD = aS - (p + 4)$.
	10	Product register shifted left 2 when used in multiply/ALU instructions $aD = p \times 4$, $aD = aS + (p \times 4)$, $aD = aS - (p \times 4)$.
	11	Reserved.

* x is don't care.

Register Settings (continued)

Parallel I/O Control (PIOC) Register

Table 17. Parallel I/O Control (PIOC) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	IBF	STROBE		PODS	PIDS	S/C	INTERRUPTS					STATUS				

Field	Value*	Description
IBF	R	IBF interrupt status bit (same as bit 4).
STROBE	00 01 10 11	Strobe width of: PODS† PIDS† T T 2T 2T 3T 3T 4T 4T
PODS	0	PODS is an input (passive mode).
	1	PODS is an output (active mode).
PIDS	0	PIDS is an input (passive mode).
	1	PIDS is an output (active mode).
S/C	0	Not status/control mode.
	1	Status/control mode.
INTERRUPTS	1xxxx	IBF interrupt enabled (disabled when 0).
	x1xxx	OBE interrupt enabled (disabled when 0).
	xx1xx	PIDS interrupt enabled (disabled when 0).
	xxx1x	PODS interrupt enabled (disabled when 0).
	xxxx1	INT interrupt enabled (disabled when 0).
STATUS	Rxxxx	IBF status bit.
	xRxxx	OBE status bit.
	xxRxx	PIDS status bit.
	xxxRx	PODS status bit.
	xxxxR	INT status bit.

*   x is don't care; R is read only.
†   T = 2 x tCKIHCKIH (see Figure 4).

Instruction Set Formats

This section defines the hardware-level encoding of the DSP16A device instructions.

Multiply/ALU Instructions

Format 1: Multiply/ALU Read/Write Group:

Field	T					D	S	F1			X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 1a: Multiply/ALU Read/Write Group:

Field	T					$\overline{aT}$	S	F1			X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2: Multiply/ALU Read/Write Group:

Field	T					D	S	F1			X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2a: Multiply/ALU Read/Write Group:

Field	T					$\overline{aT}$	S	F1			X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Special Function Instructions

Format 3: Special Functions:

Field	T					D	S	F2			C				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Control Instructions

Format 4: Branch Direct Group:

Field	T				JA										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 5: Branch Indirect Group:

Field	T					B			Reserved						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 6: Conditional Branch Qualifier/Software Interrupt (icall):
   Note that a branch instruction immediately follows except for a software interrupt (icall).

Field	T				SI	Reserved				C					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Instruction Set Formats (continued)

Data Move Instructions

Format 7: Data Move Group:

Field	T					$\overline{aT}$	R						Y/Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 8: Data Move (immediate operand — 2 words):

Field	T				D	R						Y				
	Immediate Operand (N)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 9: Short Immediate Group:

Field	T					I	Short Immediate Operand									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Cache Instructions

Format 10: Do — Redo:

Field	T					NI				K						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Instruction Set Formats (continued)

Field Descriptions

T Field. Specifies the type of instruction.

T	Operation*		Format
0000x	goto JA		4
00010	Short imm j, k, rb, re		9
00011	Short imm r0, r1, r2, r3		9
00100	Y=a1[l] F1		1
00101	Z : aT[l] F1		2a
00110	Y F1		1
00111	aT[l]=Y F1		1a
01000	aT=R		7
01001	R=a0		7
01010	R=N		8
01011	R=a1		7
01100	Y=R		7
01101	Z : R		7
01110	Do, redo		10
01111	R=Y		7
1000x	call JA		4
10010	ifc C F2		3
10011	if C F2		3
10100	Y=y[l] F1		1
10101	Z : y[l] F1		2
10110	x=Y F1		1
10111	y[l]=Y F1		1
11000	Branch indirect		5
11001	y=a0 x=X F1		1
11010	Cond. branch qualifier		6
11011	y=a1 x=X F1		1
11100	Y=a0[l] F1		1
11101	Z : y x=X F1		2
11110	Reserved		—
11111	y=Y x=X F1		1

* imm = immediate.

D Field. Specifies a destination accumulator.

D	Register
0	Accumulator 0
1	Accumulator 1

aT Field. Specifies transfer accumulator.

aT	Register
0	Accumulator 1
1	Accumulator 0

S Field. Specifies a source accumulator.

S	Register
0	Accumulator 0
1	Accumulator 1

F1 Field. Specifies the multiply/ALU function.

F1	Operation	
0000	aD = p	p = x * y
0001	aD = aS + p	p = x * y
0010		p = x * y
0011	aD = aS – p	p = x * y
0100	aD = p	
0101	aD = aS + p	
0110	NOP	
0111	aD = aS – p	
1000	aD = aS | y	
1001	aD = aS ^ y	
1010	aS & y	
1011	aS – y	
1100	aD = y	
1101	aD = aS + y	
1110	aD = aS & y	
1111	aD = aS – y	

X Field. Specifies the addressing of ROM data in two-operand multiply/ALU instructions. Specifies the high or low half of an accumulator or the y register in one-operand multiply/ALU instructions.

X	Operation
Two-Operand Multiply/ALU	
0	*pt++
1	*pt++i
One-Operand Multiply/ALU	
0	aTl, yl
1	aTh, yh

Instruction Set Formats (continued)

Field Descriptions (continued)

Y Field. Specifies the form of register indirect addressing with postmodification.

Y	Operation
0000	*r0
0001	*r0++
0010	*r0--
0011	*r0++j
0100	*r1
0101	*r1++
0110	*r1--
0111	*r1++j
1000	*r2
1001	*r2++
1010	*r2--
1011	*r2++j
1100	*r3
1101	*r3++
1110	*r3--
1111	*r3++j

Z Field. Specifies the form of register indirect compound addressing with postmodification.

Z	Operation
0000	*r0zp
0001	*r0pz
0010	*r0m2
0011	*r0jk
0100	*r1zp
0101	*r1pz
0110	*r1m2
0111	*r1jk
1000	*r2zp
1001	*r2pz
1010	*r2m2
1011	*r2jk
1100	*r3zp
1101	*r3pz
1110	*r3m2
1111	*r3jk

F2 Field. Specifies the special function to be performed.

F2	Operation
0000	aD = aS >> 1
0001	aD = aS << 1
0010	aD = aS >> 4
0011	aD = aS << 4
0100	aD = aS >> 8
0101	aD = aS << 8
0110	aD = aS >> 16
0111	aD = aS << 16
1000	aD = p
1001	aDh = aSh + 1
1010	Reserved
1011	aD = rnd(aS)
1100	aD = y
1101	aD = aS + 1
1110	aD = aS
1111	aD = -aS

C Field. Specifies the condition for special functions and conditional control instructions.

C	Condition
00000	mi
00001	pl
00010	eq
00011	ne
00100	lvs
00101	lvc
00110	mvs
00111	mvc
01000	heads
01001	tails
01010	c0ge
01011	c0lt
01100	c1ge
01101	c1lt
01110	true
01111	false
10000	gt
10001	le
10010	Reserved
.	.
.	.
.	.
11111	Reserved

Instruction Set Formats (continued)

Field Descriptions (continued)

R Field. Specifies the register for data move instructions.

R	Register
000000	r0
000001	r1
000010	r2
000011	r3
000100	j
000101	k
000110	rb
000111	re
001000	pt
001001	pr
001010	pi
001011	i
001100	p
001101	pl
001110	Reserved
001111	Reserved
010000	x
010001	y
010010	yl
010011	auc
010100	psw
010101	c0
010110	c1
010111	c2
011000	sioc
011001	srta
011010	sdx
011011	tdms
011100	pioc
011101	pdx0
011110	pdx1
011111	Reserved
.	.
.	.
.	.
111110	Reserved
111111	cioc

B Field. Specifies the type of branch instruction (except software interrupt).

B	Operation
000	return
001	ireturn
010	goto pt
011	call pt
1xx	Reserved

I Field. Specifies a register for short, immediate data move instructions.

I	Register
00	r0/j
01	r1/k
10	r2/rb
11	r3/re

SI Field. Specifies when the conditional branch qualifier instruction should be interpreted as a software interrupt instruction.

SI	Operation
0	Not a software interrupt
1	Software interrupt

NI Field. Number of instructions to be loaded into the cache. Zero implies redo operation.

K Field. Number of times the NI instructions in cache are to be executed.

JA Field. 12-bit jump address.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Min	Max	Unit
Voltage Range on any Pin with Respect to Ground	−0.5	6	V
Power Dissipation	—	1	W
Storage Temperature Range	−65	150	°C
External Lead Bonding and Soldering Temperature	—	300	°C

Handling Precautions

All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static build-up, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting. AT&T employs a human-body model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current, voltage and, hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human-body model test circuit. The breakdown voltage for the DSP16A is greater than 3000 V.

Recommended Operating Conditions

Device Speed	Package Option	Temperature Class	Supply Voltage V_{DD} (V)		Ambient Temperature T_A (°C)	
			Min	Max	Min	Max
25 ns	84 PLCC	Commercial	4.75	5.25	0	70
		Industrial	4.75	5.25	−40	85
33 ns	84 PLCC	Commercial	4.5	5.5	0	70
		Industrial	4.5	5.5	−40	85
	84 PQFP	Commercial	4.5	5.5	0	70
		Industrial	4.75	5.25	−40	85
55 ns	84 PLCC	Commercial	4.5	5.5	0	70
		Industrial	4.5	5.5	−40	85
	84 PQFP	Commercial	4.5	5.5	0	70
		Industrial	4.5	5.5	−40	85

Recommended Operating Conditions (continued)

Package Thermal Considerations

The recommended operating temperature specified above is based on the maximum power, package type, and maximum junction temperature. The following equation describes the relationship between these parameters. Certain applications' maximum power may be less than the worst-case value and can use this relationship to determine maximum ambient temperature allowed.

$$T_A = T_J - P \times \theta_{JA}$$

Maximum Junction Temperature, T_J .... +125 °C
84-pin PLCC Maximum Thermal Resistance in still-air-ambient, θ_{JA} .... +43 °C /W
84-pin PQFP Maximum Thermal Resistance in still-air-ambient, θ_{JA} .... +68 °C /W

Electrical Characteristics

The following electrical characteristics are preliminary information, and are subject to change. The parameters below are valid for the following conditions: V_{DD} = 5 V $\pm$ 10%, V_{SS} = 0 V, T = 2 x tCKIHCKIH (see Figure 4.)

Table 18. Electrical Characteristics

Parameter	Symbol	T_A = 0 °C to 70 °C		T_A = –40 °C to 85 °C		Unit
		Min	Max	Min	Max	
Input Voltage: All Pins except CKI, ICK, OCK, PIDS						
Low	V_{IL}	—	0.8	—	0.8	V
High	V_{IH}	2.0	—	2.0	—	V
Clock Input Voltage: Pins CKI, ICK, OCK, PIDS						
Low	V_{IL}	—	0.8	—	0.8	V
High	V_{IH}	2.4	—	2.7	—	V
Output Low Voltage:						
Low (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	—	0.4	V
Low (I_{OL} = 5.0 μA)	V_{OL}	—	0.2	—	0.2	V
Output High Voltage:						
High (I_{OH} = –2.0 mA)	V_{OH}	V_{DD} – 0.7	—	V_{DD} – 0.7	—	V
High (I_{OH} = –5.0 μA)	V_{OH}	V_{DD} – 0.2	—	V_{DD} – 0.2	—	V
Output 3-state Current:						
High (V_{OH} = 5.5 V)	I_{OZH}	—	10	—	10	μA
Low (V_{OL} = 0.0 V)	I_{OZL}	–10	—	–10	—	μA
Input Current: All Pins except EXM						
High (V_{IH} = 5.5 V)	I_{IH}	—	5	—	5	μA
Low (V_{IL} = 0.0 V)	I_{IL}	–5	—	–5	—	μA
Input Current: EXM Pin						
High (V_{IH} = 5.5 V)	I_{IH}	—	100	—	100	μA
Low (V_{IL} = 0.0 V)	I_{IL}	–100	—	–100	—	μA
Input, Output, and I/O Pin Capacitance	C_I	—	10	—	10	pF

Latch-up Warning: All CMOS devices are prone to latch-up if excessive current is injected to/from the substrate. To prevent latch-up at powerup, no input pin should be subjected to input voltages greater than V_{IL}, or less than V_{SS} – 0.5 V before V_{DD} is applied. After powerup, inputs should not be greater than V_{DD} + 0.5 V or less than V_{SS} – 0.5 V.

Electrical Characteristics (continued)

Power Dissipation

Power dissipation is highly dependent on program activity. The typical power dissipation listed is for a selected application, while the maximum power dissipation listed is for a worst-case continuous loop of multiply/accumulates with memory accesses. One can see that the variation due to program activity can produce power dissipations for a specific application that are lower than the worst-case maximum specification. The following electrical characteristics are preliminary information, and are subject to change.

Table 19. Power Dissipation

Parameter	Symbol	25 ns		33 ns		55 ns		Unit
		Typ	Max	Typ	Max	Typ	Max	
Power Supply Voltage	V_{DD}	5	5.25	5	5.5	5	5.5	V
Power Supply Current	I_{DD}	119	188	90	150	54	90	mA
Power Dissipation	PD	594	990	450	825	270	495	mW
Power Supply Current In Sleep State	I_{DD}	7.9	8.8	6	8	3.6	4.8	mA
Power Dissipation In Sleep State	PD	39	46	30	44	18	26	mW

The power dissipation listed is for outputs loaded at 70 pF. Total power dissipation can be calculated on the basis of the application by adding $C \times V_{DD}^2 \times f$ for each output, where C is the additional load capacitance and f is the output frequency.

Power dissipation due to the input and I/O buffers is highly dependent on input voltage level. At full CMOS levels, essentially no dc current is drawn; but, for levels near the threshold of 1.4 V, high and unstable levels can flow. Therefore, all unused input pins should be tied inactive to V_{DD} or Vss, and all unused I/O pins should be tied inactive through a 10 kΩ resistor to V_{DD} or Vss . Table 20 shows the input buffer power dissipation for 43 inputs biased at dc level, V_{IN}, with V_{DD} at 5.0 V.

Table 20. Input Buffer Power Dissipation

V_{IN} (V)	5.0	3.6	2.8	2.4	2.0	1.4	0.8	0.4	0
PD (mW)	<1.0	13.5	140	180	180	High and unstable	80	7.5	<1.0

Timing Characteristics and Requirements

The following timing characteristics requirements are preliminary information, and are subject to change. Timing characteristics refer to the behavior of the device under specified conditions. Timing requirements refer to conditions imposed on the user for proper operation of the device. All timing data is valid for the following conditions unless otherwise specified:

■ $T_A = -40\ °C$ to $+85\ °C$ or 0 °C to 70 °C (see Recommended Operating Conditions)

■ $V_{DD} = 5\ V \pm 10\%$ or $5\ V \pm 5\%$, Vss = 0 V (see Recommended Operating Conditions)

■ T = 2 x tCKIHCKIH

■ Capacitance load on outputs = 50 pF

■ Timing requirements and characteristics are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V.

Timing Characteristics and Requirements (continued)
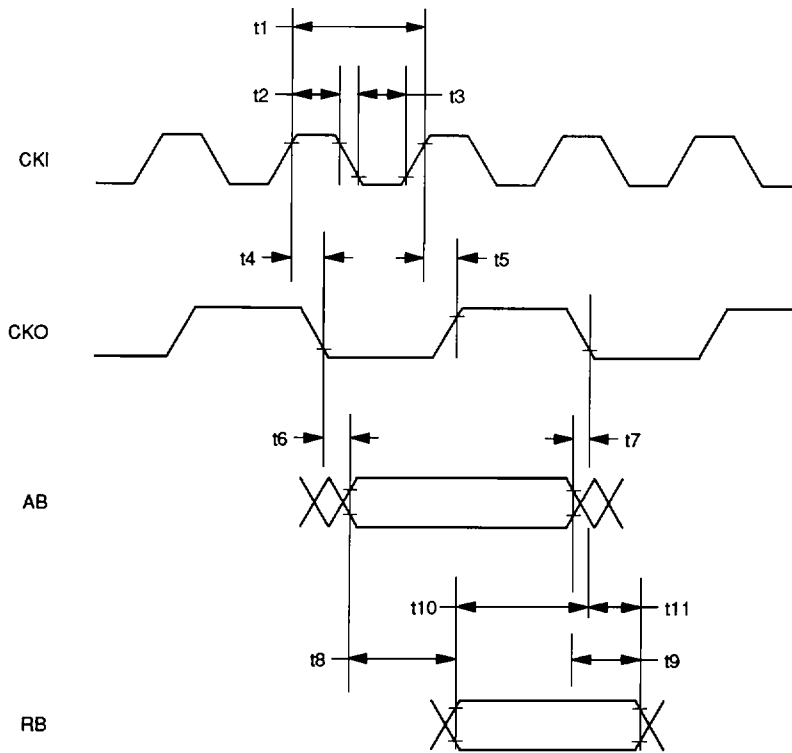
External Memory and Clocks

Figure 4. External Memory Interface

Table 21. Timing Requirements for External ROM and Clocks (See Figure 4.)

Abbreviated Reference	IEEE Symbol	Parameter	25 ns Min	25 ns Max	33 ns Min	33 ns Max	55 ns Min	55 ns Max	Unit
t1	tCKIHCKIH	Clock in Period.	12.5	—*	16.5	—*	27.5	—*	ns
t2	tCKIHCKIX	Clock in High Time.	4	—	5	—	8	—	ns
t3	tCKILCKIX	Clock in Low Time.	4	—	5	—	8	—	ns
t8	tABVRBV	Ext. Memory Access.	T – 10	—	T – 13	—	T – 15	—	ns
t9	tABXRBX	Ext. Memory Hold.	0	—	0	—	0	—	ns
t10	tRBVCKOL	Ext. Memory Setup.	7.5	—	10.5	—	12.5	—	ns
t11	tCKOLRBX	Ext. Memory Hold.	0	—	0	—	0	—	ns

* Device is fully static; tCKIHCKIH is tested at 500 ns; memory hold time is tested at 0.1 s.

Table 22. Timing Characteristics for External ROM and Clocks (See Figure 4.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t4	tCKIHCKOL	Clock Out Delay.	—	14	ns
t5	tCKIHCKOH		—	11	
t6	tCKOLABV	Address Delay Time.	—	2.5	ns
t7	tCKOLABX	Address Hold Time.	–8	—	ns

30

Timing Characteristics and Requirements (continued)

Reset and Interrupts
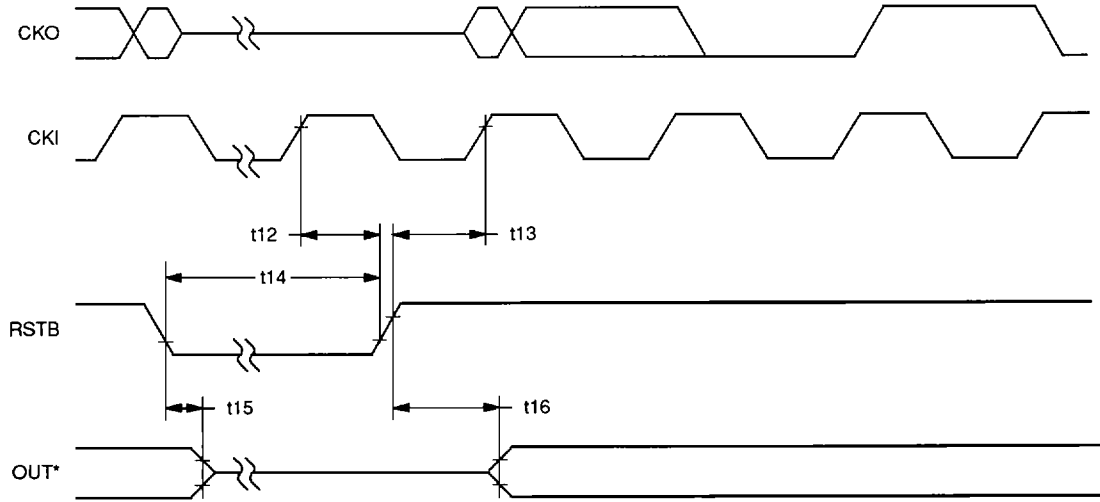
Figure 5. Reset Timing
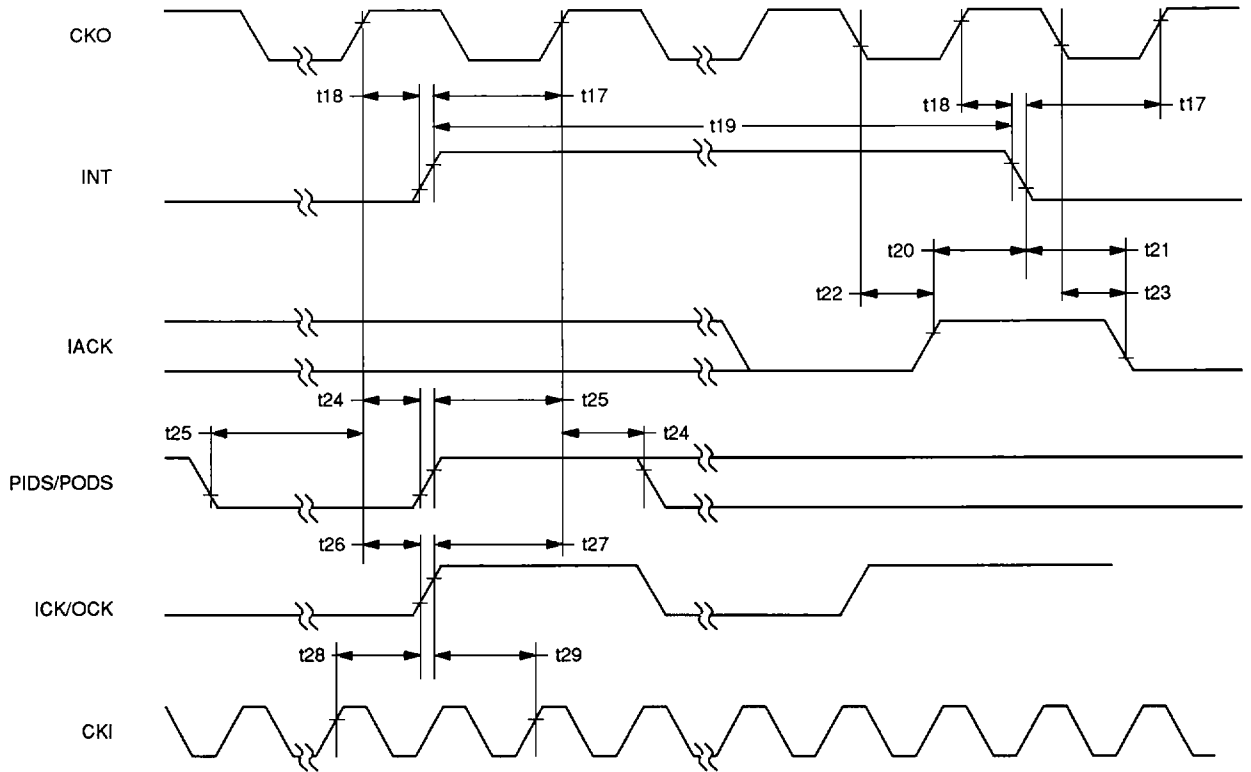
Figure 6. Interrupt Timing

Timing Characteristics and Requirements (continued)

Reset and Interrupts (continued)

Table 23. Timing Requirements for Reset and Interrupts
(See Figure 5 and Figure 6.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t14	tRSTBLRSTBX	RSTB Low Time.	6T	—	ns
t19	tINTHINTX	INT Assertion Time.	T + 10	—	ns
t20	tIACKHINTL or	INT Hold Time.	—	3T − 30	ns
t21	tINTLIACKL		T + 30	—	

Table 24. Timing Characteristics for Reset and Interrupts
(See Figure 5 and Figure 6.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t15	tRSTBHOUTZ	RSTB Disable Time.	—	100	ns
t16	tRSTBHOUTE	RSTB Enable Time.	—	100	ns
t22	tCKOLIACKH	IACK Delay Time.	—	10	ns
t23	tCKOLIACKL				

Table 25. Timing Requirements for Synchronous Reset and Interrupts
(See Figure 5 and Figure 6.)

Setup and hold time requirements are used to guarantee synchronous operation and do not have to be satisified for asynchronous operation.

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t12	tCKIHRSTBX	RSTB Hold Time.	0	—	ns
t13	tRSTBVCKIH	RSTB Setup Time.	3	—	ns
t17	tINTHCKOH	INT Setup Time.	20	—	ns
t17	tINTLCKOH				
t18	tCKOHINTX	INT Hold Time.	0	—	ns
t24	tCKOHPIODSX	PIDS/PODS Hold Time.	0	—	ns
t25	tPIODSVCKOH	PIDS/PODS Setup Time.	16	—	ns
t26	tCKOHIOCKX	ICK/OCK CKO Hold Time.	0	—	ns
t27	tIOCKVCKOH	ICK/OCK CKO Setup Time.	21	—	ns
t28	tCKIHIOCKX	ICK/OCK CKI Hold Time.	2	—	ns
t29	tIOCKVCKIH	ICK/OCK CKI Setup Time.	7	—	ns

Timing Characteristics and Requirements (continued)
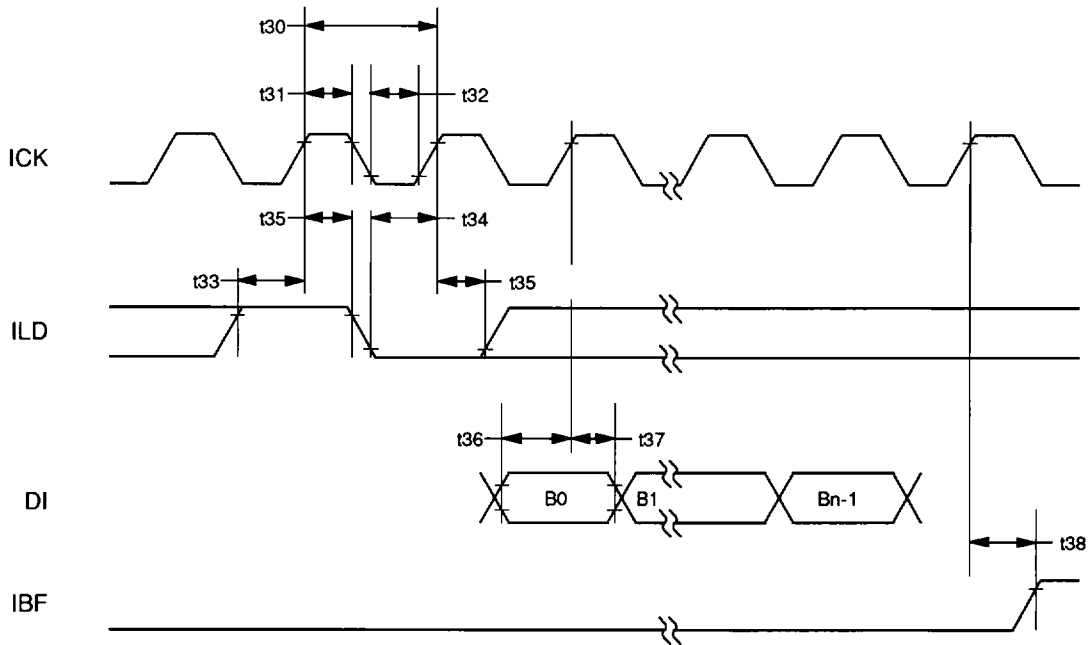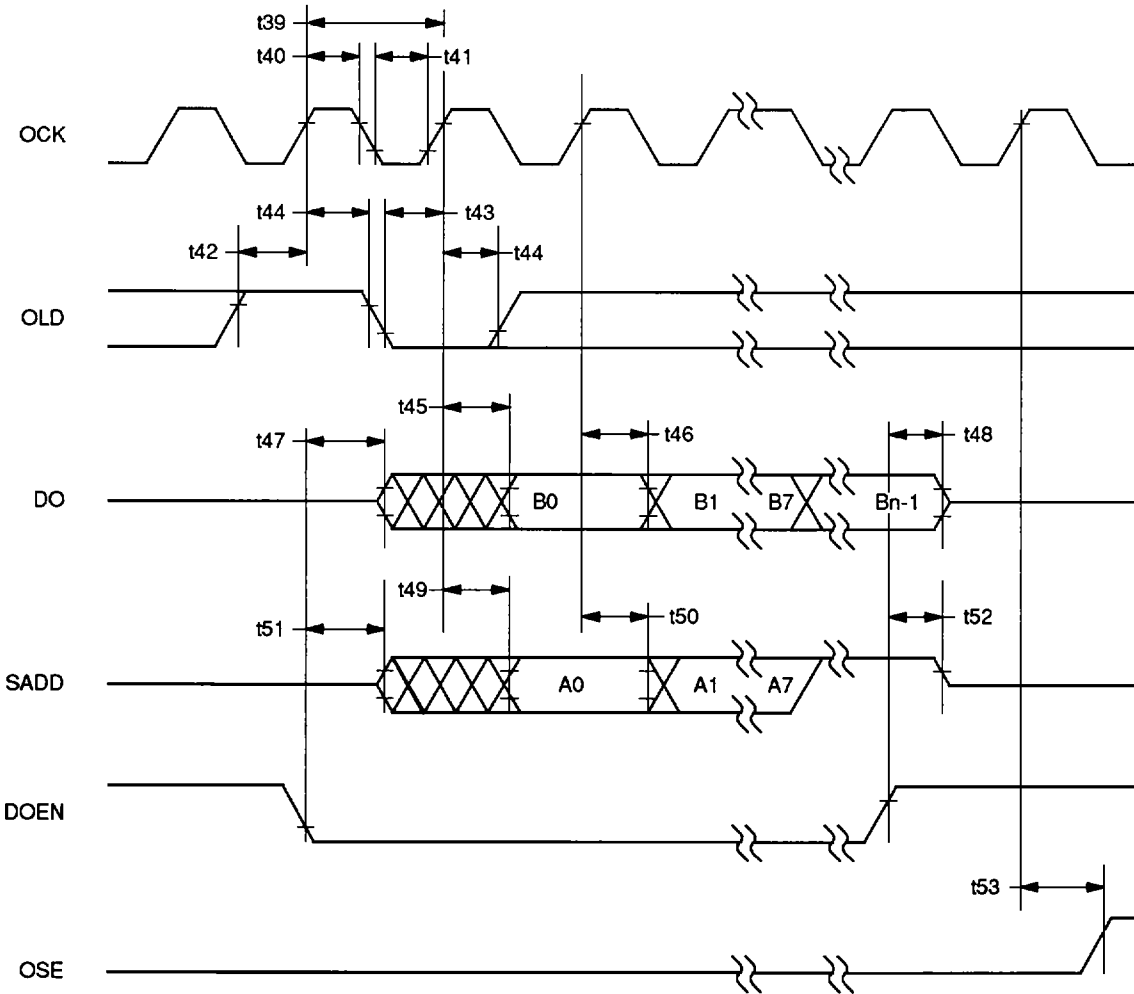
Serial I/O (SIO)

Figure 7. Serial Input Timing

Table 26. Timing Requirements for Serial Inputs (See Figure 7.)

Abbreviated Reference	IEEE Symbol	Parameter	25 ns		33 ns		55 ns		Unit
			Min	Max	Min	Max	Min	Max	
t30	tICKHICKH	Clock Period.	50	—*	66	—*	110	—*	ns
t31	tICKHICKX	Clock High Time.	23	—	30	—	45	—	ns
t32	tICKLICKX	Clock Low Time.	23	—	30	—	45	—	ns
t33 t34	tILDHICKH tILDLICKH	Load Setup.	8	—	8	—	8	—	ns
t35	tICKHILDX	Load Hold.	0	—	0	—	0	—	ns
t36	tDIVICKH	Data Setup.	7		7		7		
t37	tICKHDIX	Data Hold.	0	—	0	—	0	—	ns

* Device is fully static; tICKHICKH is tested at 2000 ns.

Table 27. Timing Characteristics for Serial Input (See Figure 7.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t38	tICKHIBFH	IBF Delay.	—	20	ns

Timing Characteristics and Requirements (continued)

Serial I/O (SIO) (continued)

Figure 8. Serial Output Timing

Timing Characteristics and Requirements (continued)

Serial I/O (SIO) (continued)

Table 28. Timing Requirements for Serial Output (See Figure 8.)

Abbreviated Reference	IEEE Symbol	Parameter	25 ns		33 ns		55 ns		Unit
			Min	Max	Min	Max	Min	Max	
t39	tOCKHOCKH	Clock Period.	50	—*	66	—*	110	—*	ns
t40	tOCKHOCKX	Clock High Time.	23	—	30	—	45	—	ns
t41	tOCKLOCKX	Clock Low Time.	23	—	30	—	45	—	ns
t42	tOLDHOCKH	Load Setup.	7	—	7	—	7	—	ns
t43	tOLDLOCKH								
t44	tOCKHOLDX	Load Hold.	0	—	0	—	0	—	ns

* Device is fully static; tOCKHOCKH is tested at 2000 ns.

Table 29. Timing Characteristics for Serial Output* (See Figure 8.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t45	tOCKHDOV	Data Delay.	—	16	ns
t46	tOCKHDOX	Data Hold.	3	—	ns
t47	tDOENLDOE	Data Enable Delay.	—	21	ns
t48	tDOENHDOZ	Data Disable Delay.	—	35	ns
t49	tOCKHSADDV	Address Delay.	—	20	ns
t50	tOCKHSADDOX	Address Hold.	3	—	ns
t51	tDOENLSADDE	Address Enable Delay.	—	35	ns
t52	tDOENHSADDZ	Address Disable Delay.	—	35	ns
t53	tOCKHOSEH	OSE Delay.	—	16	ns

* Capacitance load on OCK and DO equals 100 pF.

Timing Characteristics and Requirements (continued)

Signal Generation (Active Mode)
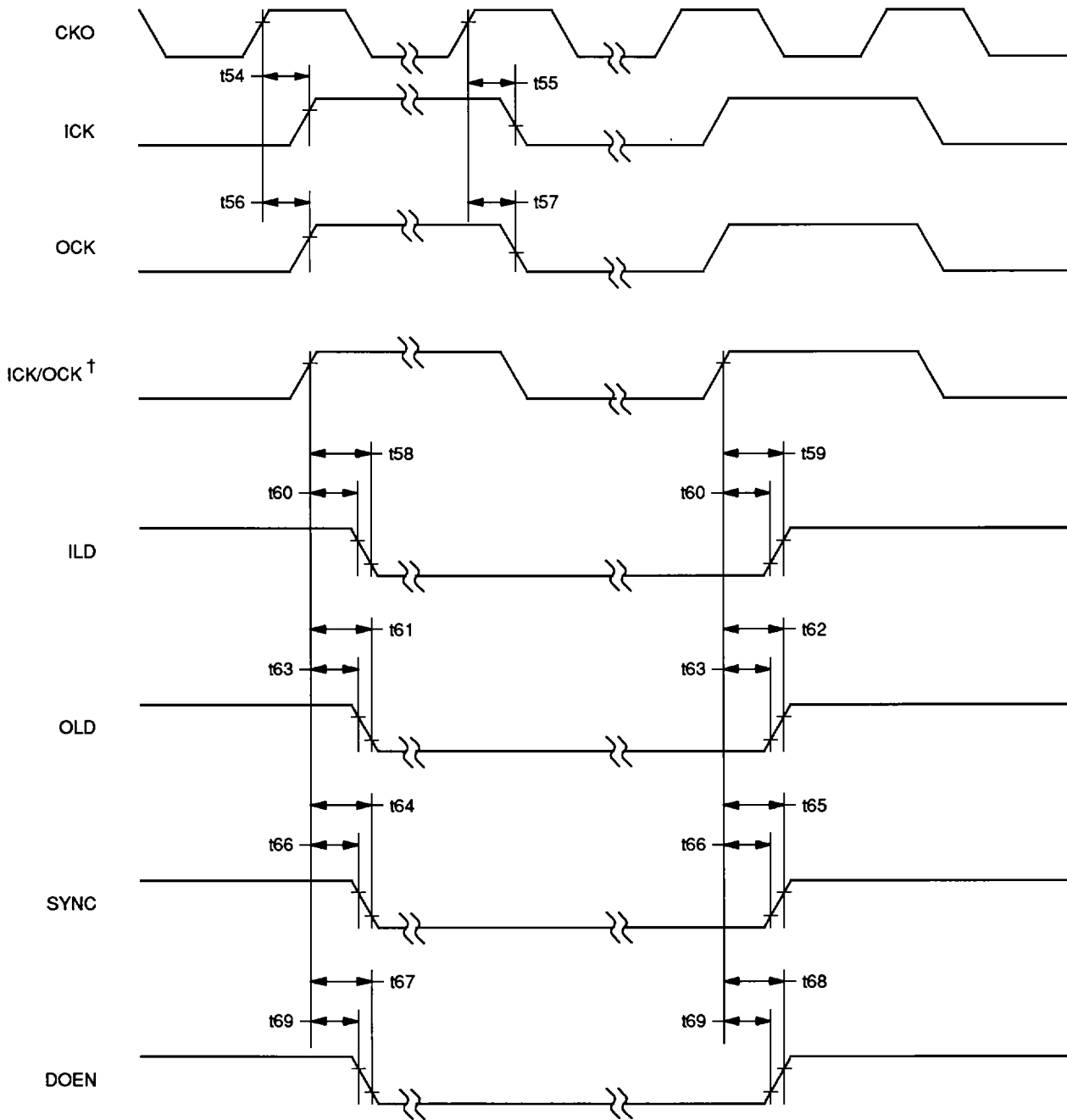
† See sioc register, LD field.

Figure 9. Serial I/O Active Timing

Timing Characteristics and Requirements (continued)

Signal Generation (Active Mode) (continued)

Table 30. Timing Characteristics for Signal Generation (See Figure 9.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t54	tCKOHICKH	ICK Delay.	—	8	ns
t55	tCKOHICKL				
t56	tCKOHOCKH	OCK Delay.	—	8	ns
t57	tCKOHOCKL				
t58	tIOCKHILDL	ILD Delay.	—	25	ns
t59	tIOCKHILDH				
t60	tIOCKHILDX	ILD Hold.	3	—	ns
t61	tIOCKHOLDL	OLD Delay.	—	25	ns
t62	tIOCKHOLDH				
t63	tIOCKHOLDX	OLD Hold.	3	—	ns
t64	tIOCKHSYNCL	SYNC Delay.	—	15	ns
t65	tIOCKHSYNCH				
t66	tIOCKHSYNCX	SYNC Hold.	3	—	ns
t67	tIOCKHDOENL	DOEN Delay.	—	18	ns
t68	tIOCKHDOENH				
t69	tIOCKHDOENX	DOEN Hold.	3	—	ns

Timing Characteristics and Requirements (continued)

Multiprocessor Communication

All serial I/O timing requirements and characteristics (except DO and SADD output enable and bit 0 characteristics) still apply.
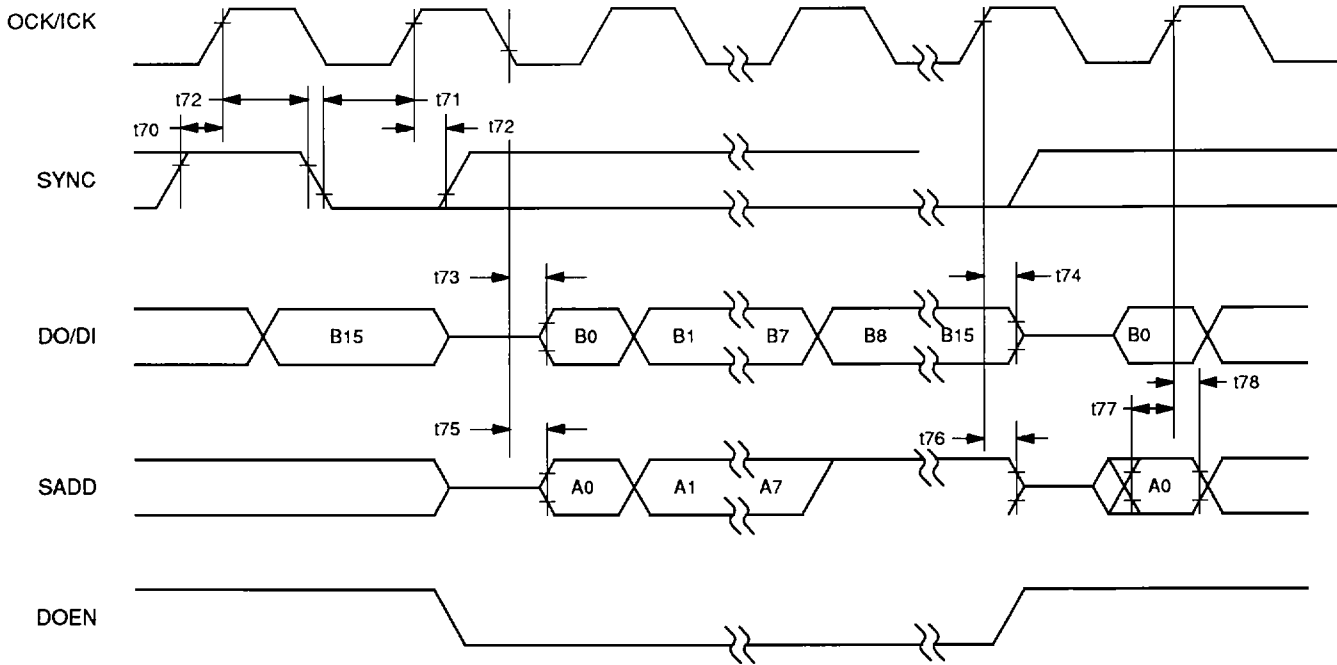
Figure 10. Serial Multiprocessor Timing

Table 31. Timing Requirements for Multiprocessor Communication (See Figure 10.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t70	tSYNCHIOCKH	SYNC Setup.	12	—	ns
t71	tSYNCLIOCKH				
t72	tIOCKHSYNCX	SYNC Hold.	2	—	ns
t77	tSADDVIOCKH	Address Setup.	12	—	ns
t78	tIOCKHSADDX	Address Hold.	0	—	ns

Table 32. Timing Characteristics for Multiprocessor Communication (See Figure 10.)

Abbreviated Reference	IEEE Symbol*	Parameter	Min	Max	Unit
t73	tOCKLDOV	Data Delay (bit 0 only).	—	19	ns
t74	tOCKHDOZ	Data Disable Delay.	—	40	ns
t75	tOCKLSADDV	Address Delay (bit 0 only).	—	19	ns
t76	tOCKHSADDZ	Address Disable Delay.	—	40	ns

* Capacitance load on ICK, OCK, DO, SYNC, and SADD = 100 pF. tICKHICKH and tOCKHOCKH are tCKIHCKIH x 4, x 12, x 16, or x 20 (see sioc register). tILDHILDH and tOLDHOLDH are (tICKHICKH or tOCKHOCKH) x 16 (see sioc register). tSYNCHSYNCH is (tICKHICKH or tOCKHOCKH) x 128 or x 256 (see tdms register).

Timing Characteristics and Requirements (continued)
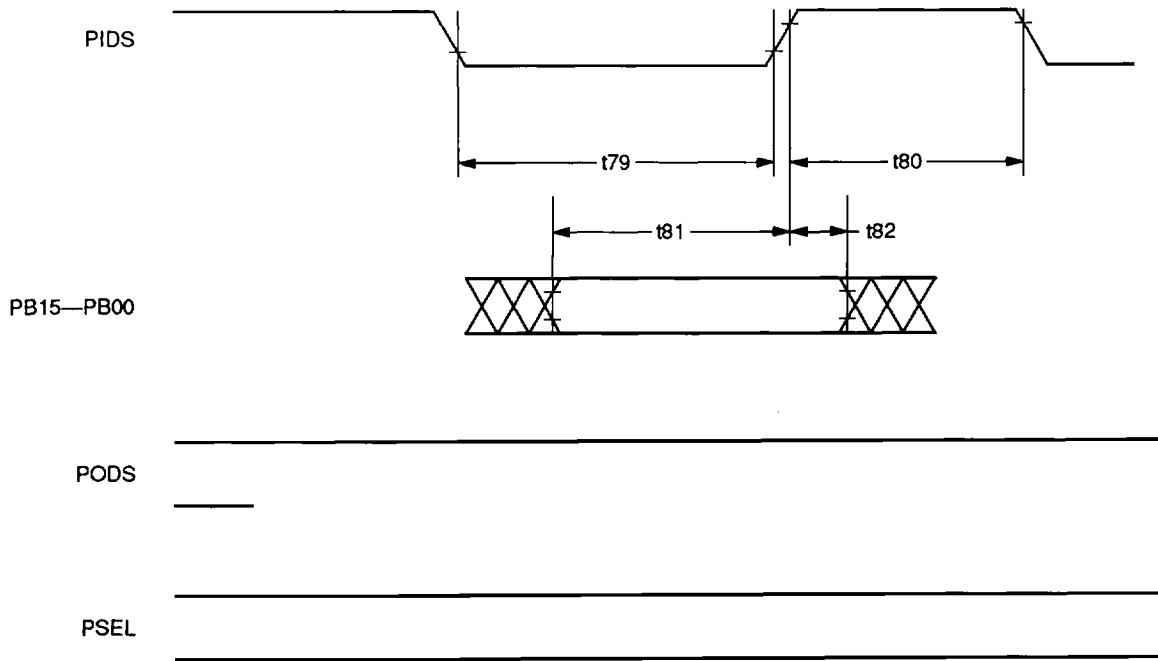
Parallel I/O (PIO)

Figure 11. Parallel Input Timing
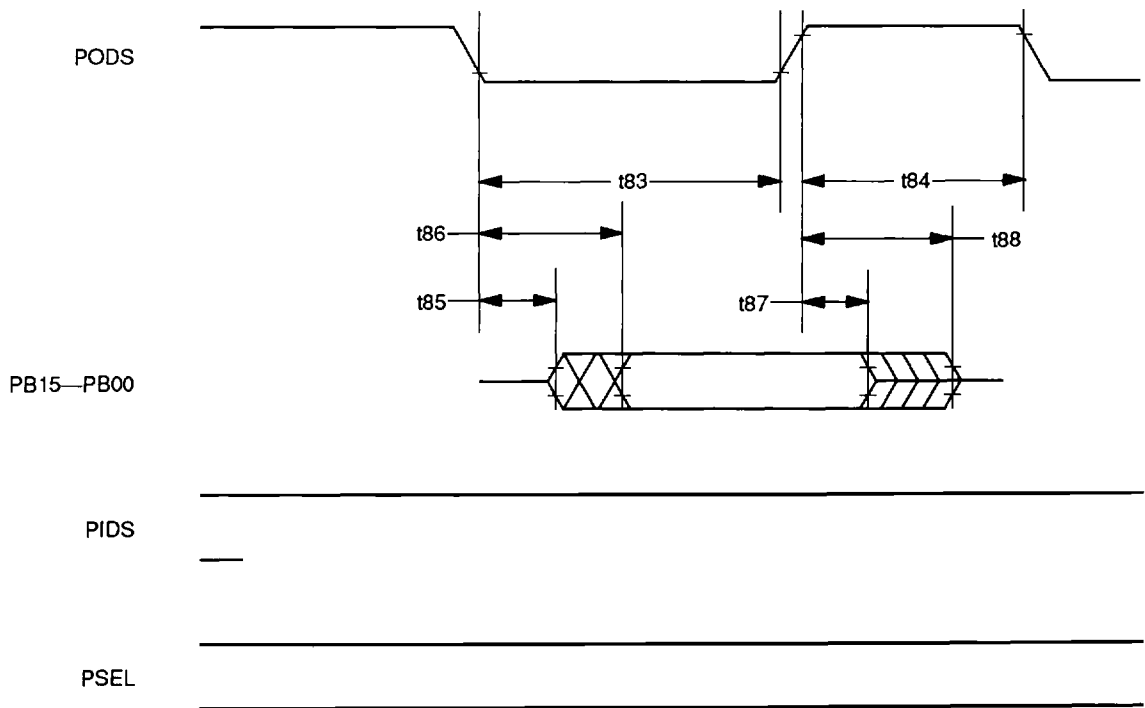
Figure 12. Parallel Output Timing

Timing Characteristics and Requirements (continued)

Parallel I/O (PIO) (continued)

Table 33. Timing Requirements for PIO (See Figure 11 and Figure 12.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t79	tPIDSLPIDSX	Passive Strobe Width (read).	T	—	ns
t80	tPIDSHPIDSX	PIDS High Between Reads.	T	—	ns
t81	tPDBVPIDSH	PB Setup Time.	10	—	ns
t82	tPIDSHPDBX	PB Hold Time.	0	—	ns
t83	tPODSLPODSX	Passive Strobe Width (write).	T	—	ns
t84	tPODSHPODSX	PODS High Between Writes.	T	—	ns

Table 34. Timing Characteristics for PIO (See Figure 12.)

Abbreviated Reference	IEEE Symbol	Parameter	Min	Max	Unit
t85	tPODSHPDBE	Data Enable Delay.	2	—	ns
t86	tPODSLPDBV	Data Valid After PODS.	—	15	ns
t87	tPODSHPDBX	Data Hold Time.	6	—	ns
t88	tPODSHPDBZ	Data Disable Delay.	—	12	ns

Timing Characteristics and Requirements (continued)

Parallel I/O (PIO) (continued)
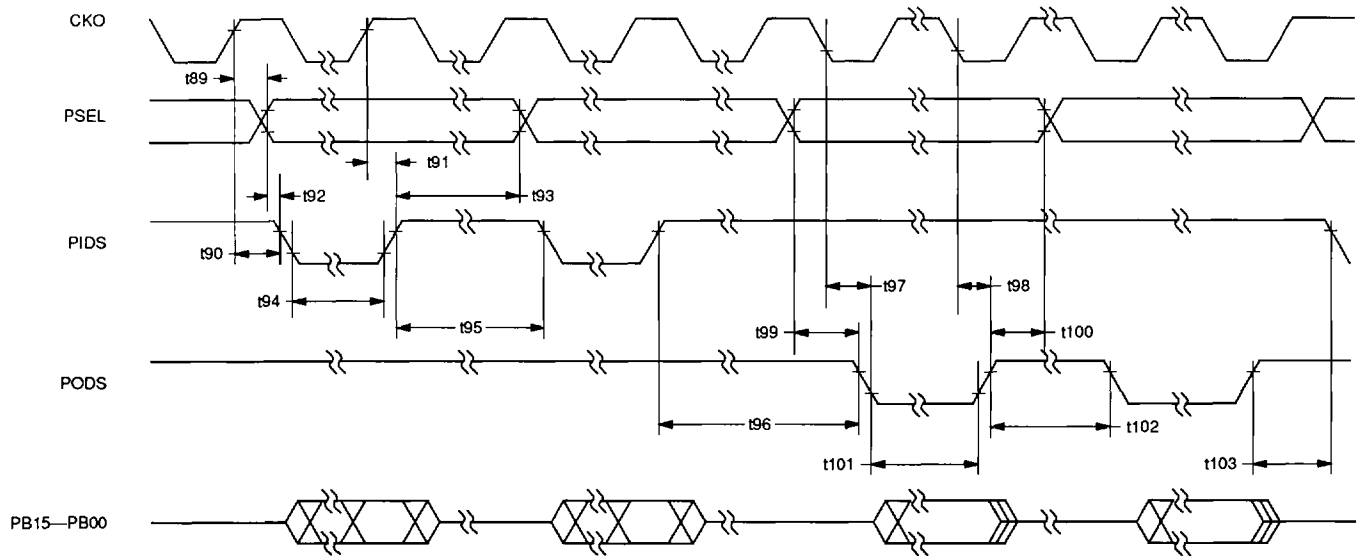
Figure 13. Parallel I/O Active Timing

Table 35. Timing Characteristics for PIO Signal Generation (See Figure 13.)

Abbreviated Reference	IEEE Symbol	Parameter	Min*	Max	Unit
t89	tCKOHPSELV	PSEL Delay.	—	6	ns
t90	tCKOHPIDSL	PIDS Delay.	—	6	ns
t91	tCKOHPIDSH		—	11	ns
t92	tPSELVPIDSX	PSEL Setup PIDS Low.	–5	—	ns
t93	tPIDSHPSELX	PSEL Hold Time PIDS High.	T – 1	—	ns
t94	tPIDSLPODSX	PIDS Low Time.	N x T – 5	—	ns
t95	tPIDSHPIDSX	PIDS High (interaccess).	T – 1	—	ns
t96	tPIDSHPODSX	PIDS High to PODS Low.	T + T/2	—	ns
t97	tCKOLPODSL	PODS Delay.	—	6	ns
t98	tCKOLPODSH		—	8	ns
t99	tPSELVPODSX	PSEL Setup PODS Low.	T/2 – 1	—	ns
t100	tPODSHPSELX	PSEL Hold Time PODS High.	T/2 – 1	—	ns
t101	tPODSLPODSH	PODS Low Time.	N x T – 5	—	ns
t102	tPODSHPODSX	PODS High (interaccess).	T – 1	—	ns
t103	tPODSHPIDSX	PODS High to PIDS Low.	T/2 – 1	—	ns

* N = 1, 2, 3, 4 depending on the STROBE field of the pioc register.

Outline Diagrams

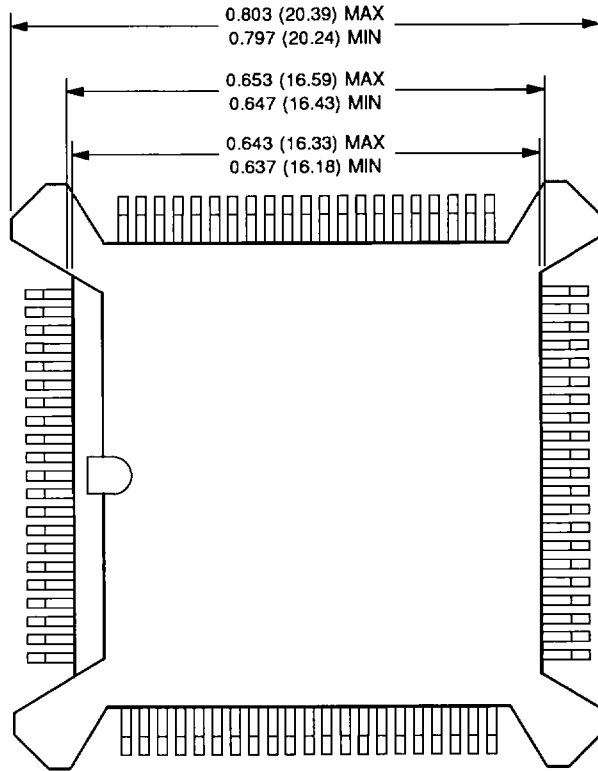## 84-Pin, Plastic Leaded Chip Carrier (PLCC)

All dimensions are in inches and (millimeters).
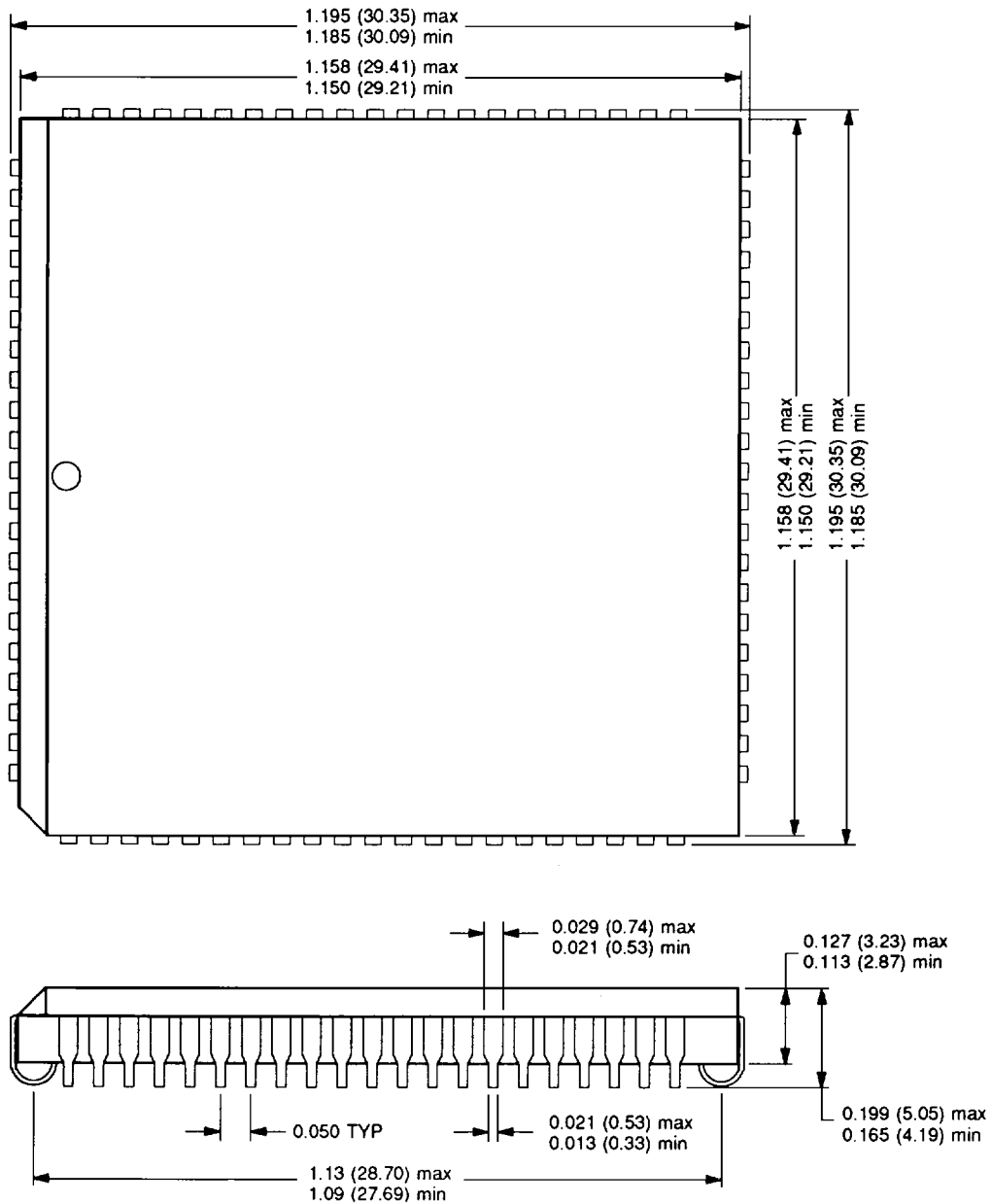
Outline Diagrams (continued)

84-Pin, Plastic Quad Flat Pack (PQFP)

All dimensions are in inches and (millimeters).

0.803 (20.39) MAX
0.797 (20.24) MIN

0.653 (16.59) MAX
0.647 (16.43) MIN

0.643 (16.33) MAX
0.637 (16.18) MIN

0.067 (1.70)
0.073 (1.85)
0.020 (0.51) MIN

0.180 (4.57) MAX

0.025 (0.635) TYP

0.012 (0.30) MAX
0.008 (0.20) MIN

0.030 (0.76) MAX
0.020 (0.51) MIN

0.785 (19.94) MAX
0.775 (19.69) MIN

May 1991
DS91-052DMOS (Replaces DS88-58DMOS and DA89-006DMOS)

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