N-Channel 100-V (D-S) 175°C MOSFET

CHARACTERISTICS

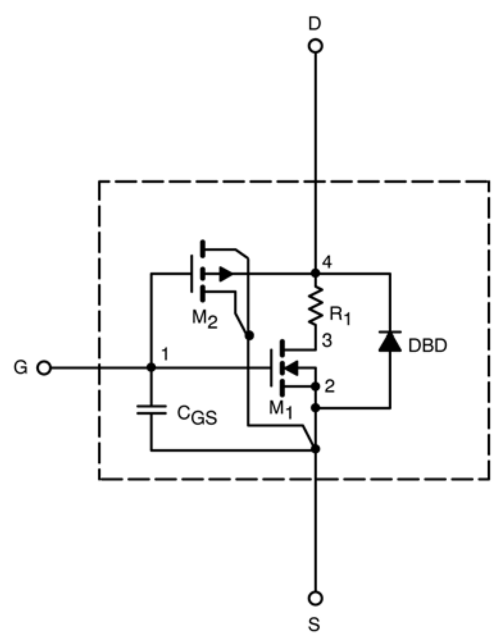
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

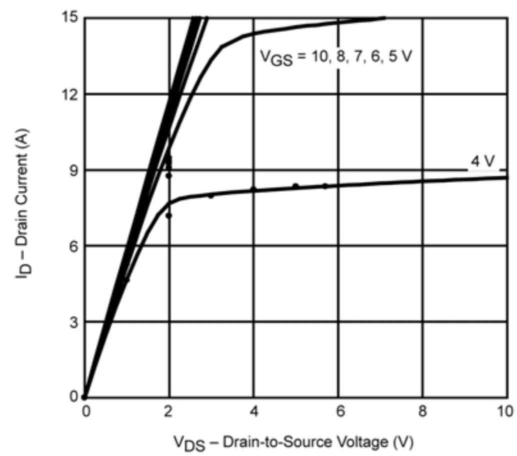


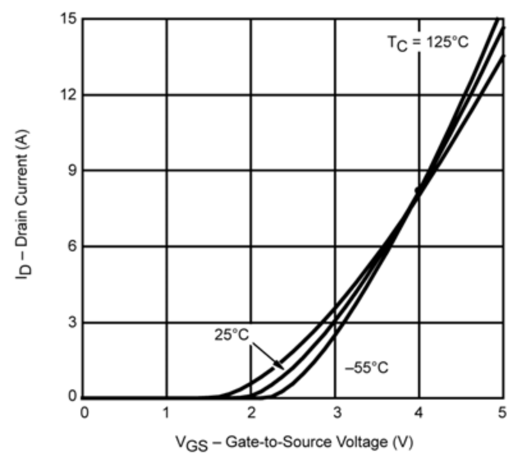
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

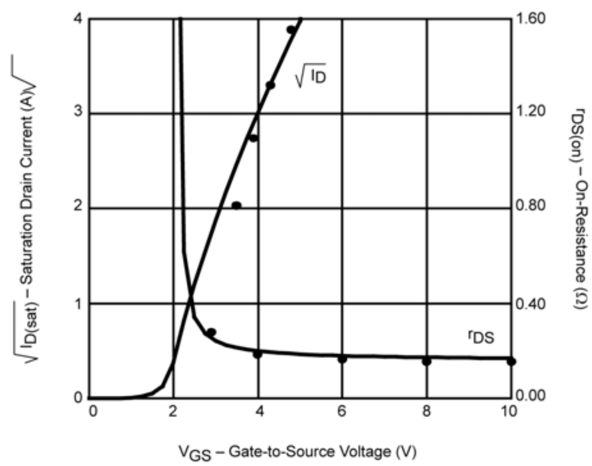
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1.5		V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	29		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3 A	0.169	0.160	Ω
		V_{GS} = 10 V, I_D = 3 A, T_J = 125°C	0.275		
		V_{GS} = 10 V, I_D = 3 A, T_J = 175°C	0.331		
		V_{GS} = 4.5 V, I_D = 1 A	0.191	0.180	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 3 A	4.5	8.5	S
Forward Voltage[a]	V_{SD}	I_S = 6.5 A, V_{GS} = 0 V	0.85	0.90	V
Dynamic[b]					
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	236	240	pF
Output Capacitance	C_{oss}		43	42	
Reverse Transfer Capacitance	C_{rss}		16	17	
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 6.5 A	2.8	2.7	nC
Gate-Source Charge[c]	Q_{gs}		0.60	0.60	
Gate-Drain Charge[c]	Q_{gd}		0.70	0.70	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 7.5 Ω $I_D \cong$ 6.5 A, V_{GEN} = 10 V, R_G = 2.5 Ω	6	7	ns
Rise Time[c]	t_r		6	8	
Turn-Off Delay Time[c]	$t_{d(off)}$		8	8	
Fall Time[c]	t_f		10	9	
Reverse Recovery Time	t_{rr}	I_F = 6.5 A, di/dt = 100 A/µs	51	35	

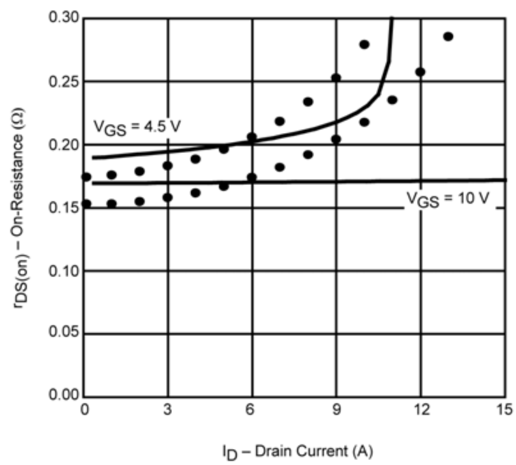
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

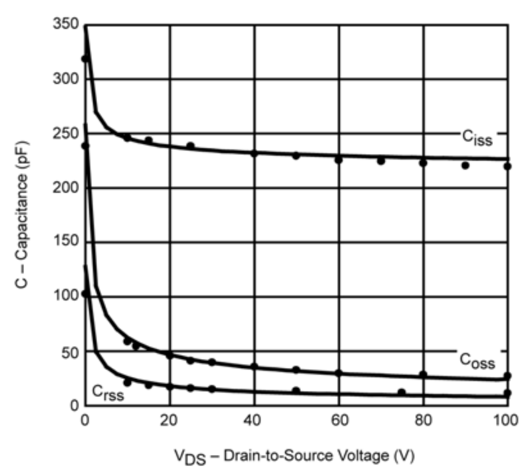
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

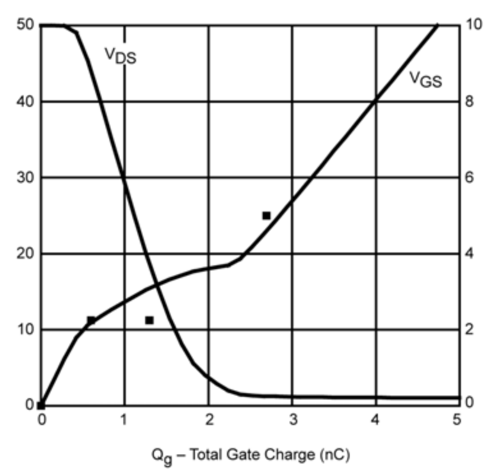












Note: Dots and squares represent measured data.

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