V370PDC PCI SDRAM Controller

QUICKLOGIC®

• • • • • • High Performance PCI Target Interface with Integrated SDRAM Controller

Device Highlights

- Fully compliant with PCI 2.2 specification target interface

- Multiplexed or non-multiplexed 8-, 16-, or 32-bit generic peripheral bus interface

- Supports up to 1 GB of SDRAM

- Supports up to two single banks or one dual bank industrial standard 168-pin PC SDRAM DIMM

- Supports up to 1 KB of burst access from PCI

- Up to five programmable chip selects for peripheral strobe generation

- Large on-chip FIFOs using Dynamic Bandwidth Allocation™ architecture

- Buffered PCI clock output

- Hot swap ready (*PICMG™ Hot Swap Specification*)

- Implementation of *PCI Bus Power Management Interface Specification*, Version 1.0

- Initialization through PCI or serial EEPROM

- Programmable PCI and local interrupt management

- Two 32-bit general purpose timers

- Up to 66 MHz local bus clock with asynchronous PCI clock up to 33 MHz

- 3.3 V operation with 5 V tolerant inputs

- Industrial temperature range (-40°C to +85°C)

- Low cost 160-pin PQFP package

Overview

The V370PDC PCI SDRAM Controller simplifies the design of PCI based memory sub-systems. System designers can replace many lower integration support components with this single, high-integration device saving design time, board area, and manufacturing cost.

The V370PDC is a high performance PCI SDRAM Controller with integrated peripheral control unit operating at up to 66 MHz local bus speed. It features multiple address translation units from PCI which allow designers the freedom to customize their local address space. Access latency of slower peripherals are absorbed through the large on-chip FIFOs.

The peripheral bus provides low latency access to SDRAM. The peripheral control unit on the V370PDC also performs address decoding and chip-select strobes generation for SRAM, PROM and other slow peripherals. The peripheral bus can also be tri-stated through a simple hand-shaking protocol to allow other local bus masters control of the bus.

The SDRAM Controller connects the PCI bus through on-chip FIFOs to SDRAM arrays of up to 1 GB in size. The fully programmable SDRAM controller also supports the use of Enhanced SDRAM to achieve even greater performance. Burst accesses of up to 1 KB from PCI is supported.

The two general purpose 32-bit timers can be individually configured as a pulse width modulator, or used in other modes such as retriggerable or one-shot. Interrupts for a real-time operating system can be easily generated by the system heartbeat timer. A watchdog timer is also provided for graceful recovery from catastrophic program failures. Interrupt requests for all on-chip peripherals are managed by the Interrupt Control Unit. Additionally, off-chip interrupts can be routed to the Interrupt Control Unit.

The V370PDC is packaged in a low-cost 160-pin EIJA Plastic Quad Flat Pack (PQFP), and is available in 66 MHz speed grade.

This document contains the product codes, electrical specifications, pinout, and package mechanical information for the V370PDC. Detailed functional information is contained in the *V370PDC User's Manual*.

Product Code

Table 1 describes the product code codes available.

Table 1: Product Code

Product Code	Package	Frequency
V370PDC-66LP REV A0	160-pin EIAJ PQFP	66 MHz
V370PDC-66LPN REV A0[a]	PB-Free 160-pin EIAJ PQFP	66 MHz

a. Lead-free.

Electrical Specifications

DC Specifications

The DC specifications for the PCI bus signals match exactly those given in the *PCI Specification*, Rev. 2.2 Section 4.2.1.1. For more information on the PCI DC specifications, see the *PCI Specification*.

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to +3.6	V
V_{IN}	DC input voltage	-0.3 to 6.0	V
T_{STG}	Storage temperature range	-55 to +125	°C

Table 3: Guaranteed Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3.0 to 3.6	V
J_{max}	Maximum junction temperature	125	°C
Theta J_a	Thermal resistance (Package)	41 to 46	°C/w
Theta J_c	Thermal resistance (Junction-Case)	21	°C/w
T_A	Ambient temperature range	-40 to +85	°C

PCI Bus DC Specifications

Table 4: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IH}	Input high voltage		0.5 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5	0.3 V_{CC}	V
I_{IH}	Input high leakage current[a]		0.7 V_{CC}		μA
I_{IL}	Input low leakage current[a]	0 < V_{IN} < V_{CC}		+10	μA
V_{OH}	Output high voltage	I_{OUT} = -500 μA	0.9 V_{CC}		V
V_{OL}	Output low voltage[b]	I_{OUT} = 1500 μA		0.1 V_{CC}	V
C_{IN}	Input pin capacitance[c]			10	pF
C_{CLK}	PCLK pin capacitance		5	12	pF
C_{IDSEL}	IDSEL pin capacitance[d]			8	pF
L_{PIN}	Pin inductance			20	nH

a. Input leakage currents include high impedance output leakage for all bi-directional buffers with tri-state outputs.
b. Signals without pull-up resistors have greater than 3mA low output current. Signals requiring pull resistors have greater than 6mA output current. The latter include FRAME, TRDY, IRDY, STOP, SERR, PERR.
c. Absolute maximum pin capacitance for a PCI unit is 10pF (except for CLK).
d. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Local Bus DC Specifications

Table 5: Local Bus/M Bus Signals DC Operating Specifications (V_{CC} = 3.3 V ± 0.3 V)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IH}	Input high leakage current	V_{IN} = V_{CC}	-10	10	μA
I_{IL}	Input low leakage current	V_{IN}=GND	-10	10	μA
V_{OH}	Output high voltage	I_{OUT} = -2, -8, -12 mA	2.4		V
V_{OL}	Output low voltage	I_{OUT} = 2, 8, 12 mA		0.4	V
I_{OZL}	Low level float input leakage	V_{OL} = GND	-10	10	μA
I_{OZH}	High level float input leakage	V_{OH} = V_{CC}	-10	10	μA
I_{CC} (max.)	Maximum supply current	PCLK = 33 MHz, CLKIN = 66 MHz, V_{CC} = 3.6 V all buses operating		70	mA
I_{CC} (typ.)	Typical supply current			40	mA
C_{IO}	Input and output capacitance			10	pF

AC Specifications

The AC specifications for the PCI bus signals match exactly those given in the *PCI Specification*, Rev. 2.1, Section 4.2.1.2. For more information on the PCI AC specifications, including the V/I curves for 5 V signalling, see section 4.2.1.2 of the *PCI Specification*, Rev 2.1.

PCI Bus Timings

Table 6: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min.	Max.	Unit
$I_{OH(AC)}$	Switching current high	$0\ V < V_{OUT} \leq 0.3\ V_{CC}$	$-12\ V_{CC}$		mA
		$0.3\ V_{CC} < V_{OUT} < 0.9\ V$	$-17.1(V_{CC}-V_{OUT})$		mA
		$0.7\ V_{CC} < V_{OUT} < V_{CC}$		Equation C	
	(Test point)	$V_{OUT} = 0.7\ V_{CC}$		$-32\ V_{CC}$	
$I_{OL(AC)}$	Switching current low	$V_{CC} > V_{OUT} > 0.6\ V_{CC}$	$16 V_{CC}$		mA
		$0.6\ V_{CC} > V_{OUT} > 0.1\ V_{CC}$	$26.7 V_{CC}$		mA
	(Test point)	$V_{OUT} = 0.18\ V_{CC}$		$38\ V_{CC}$	mA
I_{CL}	Low clamp current	$-3\ V < V_{IN} < -1\ V$	$-25+(V_{IN}+1)/0.015$		mA
t_R	Unloaded output rise time	$0.2\ V_{CC}$ to $0.6\ V_{CC}$	1	4	V/ns
t_F	Unloaded output fall time	$0.6\ V$ to $0.2\ V$	1	4	V/ns

Local Bus Timings

Table 7: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Unit
V_{CC}	Supply voltage 3.3 V operation	3.0 to 3.60	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 8: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply Voltage	Derating
8 mA	3.3 V	0.019 ns/pF for loads >50 pF
12 mA	3.3 V	0.017 ns/pF for loads >50 pF

Timing Parameters

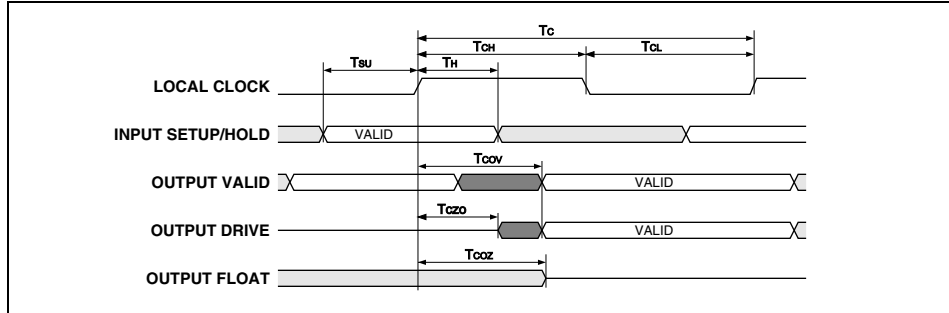Figure 1: Clock and Synchronous Signals

:

Table 9: Local Bus Timing Parameters for Vcc = 3.3 V ± 5%

Number	Symbol	Description	66 MHz		Unit
			Min.	Max.	
1	T_C	CLKIN period	15		ns
2	T_{CH}	CLKIN high time	5.5		ns
3	T_{CL}	CLKIN low time	5.5		ns
4	T_{SU}	Synchronous input setup	3		ns
4a	T_{SU}	Asynchronous input ($\overline{READY}$)[a]	7		ns
5	T_H	Synchronous input hold	1		ns
6	T_{COV}	CLKIN to output valid delay	3	11	ns
7	T_{CZO}	CLKIN to output driving delay	3	11	ns
8	T_{COZ}	CLKIN to high impedance delay	4	12	ns
9	T_{ALE}	ALE pulse width	T_{CH}+0.5	T_{CH}+1	ns
10	T_{CLH}	CLKIN rising to ALE rising	2	10	ns
11	T_{AH}	CLKIN falling to ALE falling	2	10	ns

a. Applies only to $\overline{READY}$ pin when i960_RDY bit in the LB_BUS_CFG register is set to '1'.

Table 10: PCI Bus Timing Parameters for Vcc = 3.3 V ± 10%

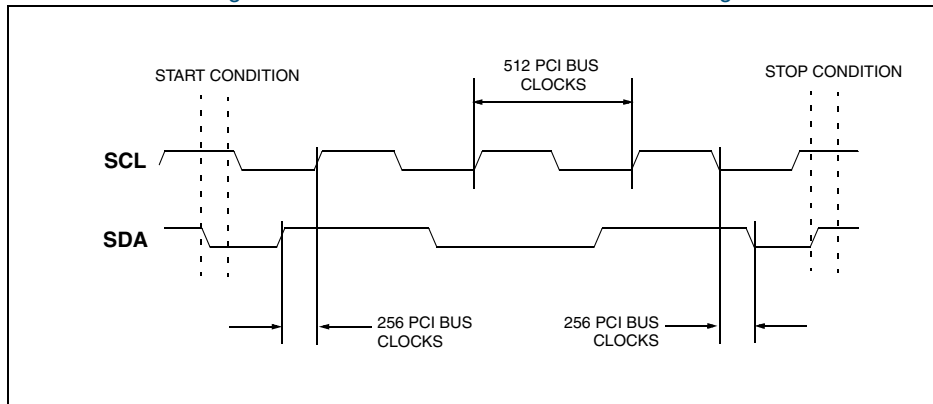| Number	Symbol	Description	Min.	Max.	Unit
1	T_C	PCLK period	30		ns
2	T_{SU}	Synchronous input setup to PCLK[a]	7		ns
3	T_H	Synchronous input hold from PCLK	0		ns
4	T_{COV}	PCLK to output valid delay[b]	3	11	ns
5	T_{CZO}	PCLK to output driving delay	4	11	ns
6	T_{COZ}	PCLK to high impedance delay	5	18	ns
7	T_{RST}	Reset period when PRST used as input	$16 \cdot T_C$		

a. All PCI signals except $\overline{GNT}$.
b. All PCI signals except $\overline{REQ}$.

Serial EEPROM Port Timings

The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in **Figure 2**.

Figure 2: Serial EEPROM Waveforms and Timings

Pin Description

Table 11 lists the pin types found on the V370PDC.

Table 11: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/OD	PCI input with open drain output.
I/O$_8$	TTL I/O pins with 8 mA drive.
I/OD	TTL input with open drain output.
I	TTL input only pin.
O$_2$, O$_8$, O$_{12}$	TTL output pins with 2/8/12 mA drive.

Signal Description

Table 12 through **Table 15** describe the function of each pin on the V370PDC.

Table 12: Signal Description—PCI Bus Interface

Signal	Type	R[a]	Description
AD[31:0]	PCI I/O	Z	Address and data, multiplexed on the same pins.
C/$\overline{BE}$[3:0]	PCI I		Bus Command and Byte Enables, multiplexed on the same pins.
PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and C/$\overline{BE}$[3:0].
$\overline{FRAME}$	PCI I		Cycle Frame indicates the beginning and burst length of an access.
$\overline{IRDY}$	PCI I		Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{TRDY}$	PCI O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{STOP}$	PCI O	Z	Stop indicates the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{DEVSEL}$	PCI O	Z	Device Select, when actively driven by a target, indicates the driving device has decoded its address as the target of the current access.
IDSEL	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
$\overline{PERR}$	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{SERR}$	PCI I/OD	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
PCLK	PCI I		PCLK provides timing for all transactions on the PCI bus.

a. **R** indicates state during reset.

Table 13: Signal Description—SDRAM and Peripheral Bus Interface

Signal	Type	R	Description
CLKIN	I		Local clock input
CLKOUT	O_{12}	X	Buffered PCI clock output
$\overline{DCS}$[3:0]	O_8	Z	SDRAM Chip Select
MA[14:0]	O_{12}	Z	SDRAM Memory Address (also, A[16:2] for peripheral access). MA[14:13] are typically used for BA[1:0]
$\overline{RAS}$	O_{12}	Z	SDRAM Row Address Strobe
$\overline{CAS}$	O_{12}	Z	SDRAM Column Address Strobe
$\overline{MWE}$	O_{12}	Z	SDRAM Memory Write Enable
MAD[31:0]	I/O_8	Z	SDRAM and peripheral bus data
$\overline{DQM}$[3:0]	O_8	Z	SDRAM Data Mask (these act as $\overline{MBE}$[3:0], A[1:0] for peripheral access)

Table 13: Signal Description—SDRAM and Peripheral Bus Interface *(Continued)*

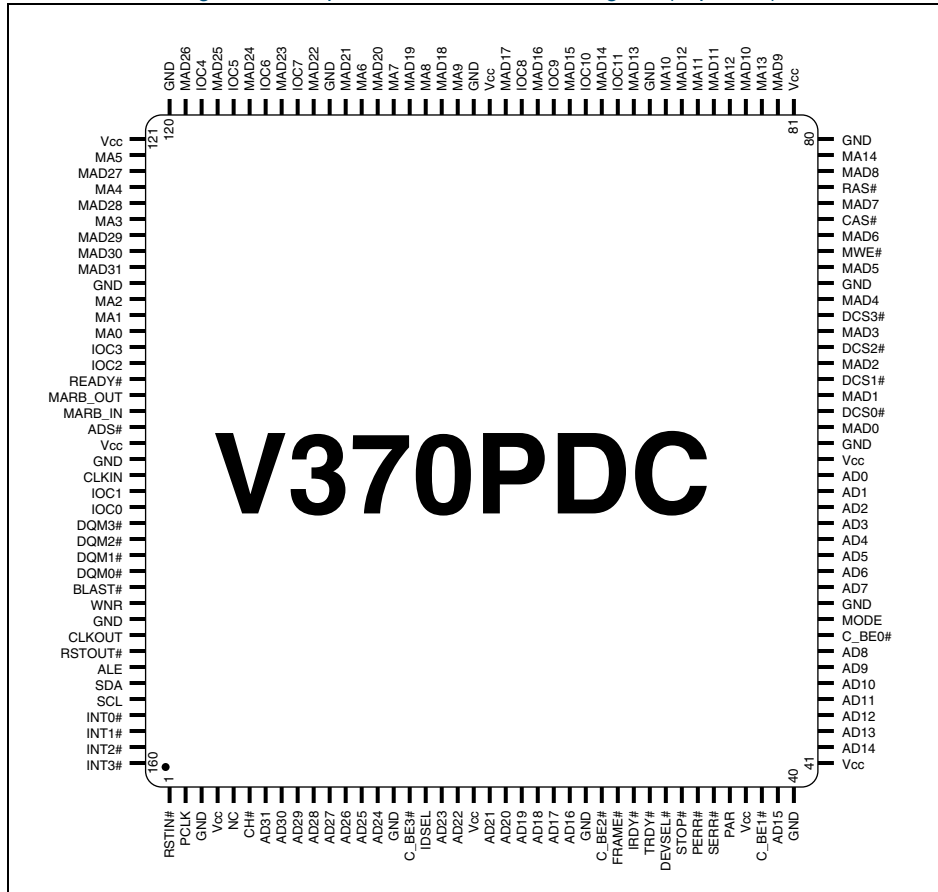| Signal	Type	R	Description
MARB_IN	I		Peripheral bus arbitration input: Treated as bus request input when V370PDC is the primary bus master. When V370PDC is the secondary bus master, this input acts as bus grant.
MARB_OUT	O_8	O	Peripheral bus arbitration output: Treated as bus grant output when V370PDC is the primary bus master. When V370PDC is the secondary bus master, this output acts bus request.
ALE	O_8	Z	Address Latch Enable: used to latch the address on MAD[31:0] during the address phase of a peripheral bus access.
$\overline{ADS}$	O_8	Z	Asserted low to indicate the beginning of a bus cycle.
$\overline{BLAST}$	O_8	Z	Burst last.
$\overline{READY}$	I		Data ready.
WNR	O_8	Z	Write/$\overline{Read}$.
SDA	I/OD	Z	Serial EEPROM Data
SCL	O_2	Z	Serial EEPROM Clock
IOC[11:0]	I/O_8	Z	Multi-purpose I/O that can be configured for many functions
$\overline{INT}$[3:0]	I/O_8	Z	General purpose interrupt inputs/outputs: may be used for either PCI or local processor interrupts

Table 14: Signal Description—Mode and Reset

Signal	Type	R	Description
$\overline{RSTIN}$	I		Reset Input: Active low reset input used to initialize all internal functions of the chip.
$\overline{RSTOUT}$	O_8	O	Reset Output: Driven active when the input reset is driven active. Driven inactive when the RSTOUT bit in the system register is set. The $\overline{RSTOUT}$ signal is synchronous to the rising edge of CLKIN.
$\overline{CH}$	I		PCI Precharge Bias: This signal is driven low to activate the on-chip precharge bias for use in PICMG Hot Swap applications. Non-Hot Swap applications should pull this signal high.

MODE	I		MODE Input: selects mastership of V370PDC:
			    0 = Secondary master
			    1 = Primary master

Table 15: Signal Description—Power and Ground Signals

Signal	Type	R	Description
V_{CC}	-		POWER leads for external connection to a 3.3V V_{CC} board plane.
GND	-		GROUND leads for external connection to a GND board plane.
NC	-		No connect.

160-pin EIAJ PQFP Pinout Diagram
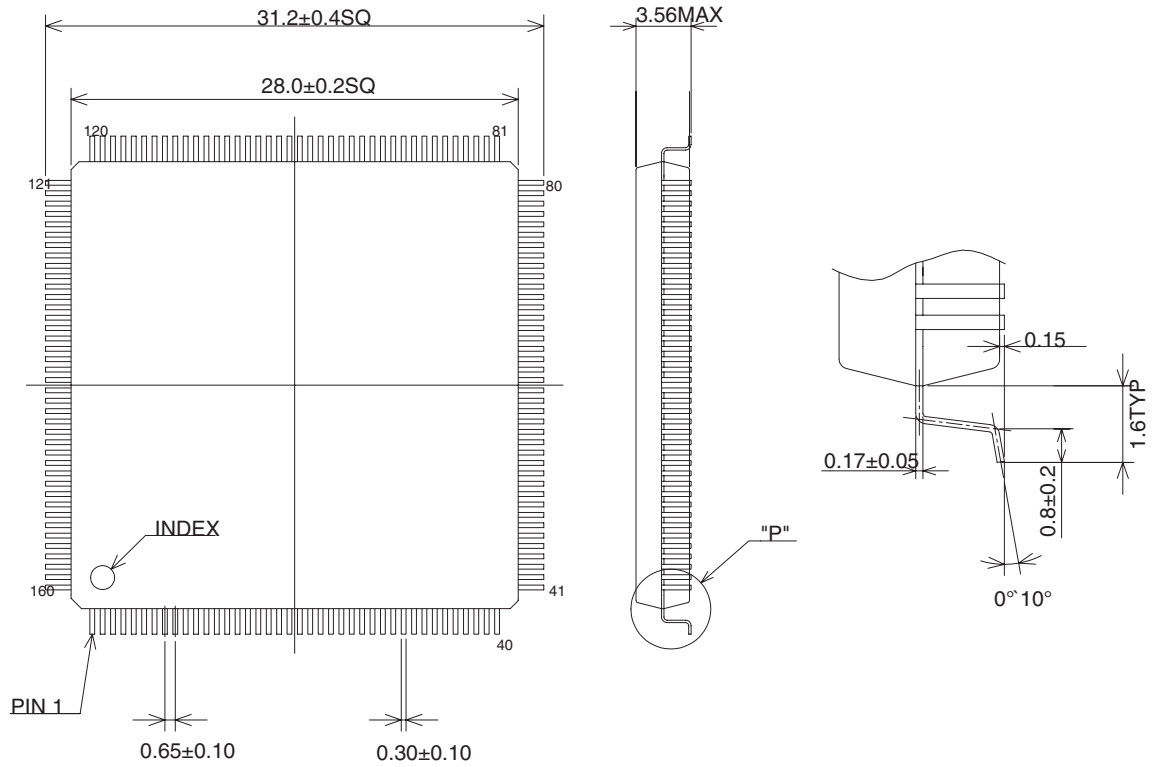
Figure 3: 160-pin EIAJ PQFP Pinout Diagram (Top View)

160-pin EIAJ PQFP Pinout Table

Table 16: 160-pin EIAJ PQFP Pinout Table

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	$\overline{\text{RSTIN}}$	41	Vcc	81	Vcc	121	Vcc
2	PCLK	42	AD14	82	MAD9	122	MA5
3	GND	43	AD13	83	MA13	123	MAD27
4	Vcc	44	AD12	84	MAD10	124	MA4
5	NC	45	AD11	85	MA12	125	MAD28
6	$\overline{\text{CH}}$	46	AD10	86	MAD11	126	MA3
7	AD31	47	AD9	87	MA11	127	MAD29
8	AD30	48	AD8	88	MAD12	128	MAD30
9	AD29	49	$\overline{\text{C\_BE0}}$	89	MA10	129	MAD31
10	AD28	50	MODE	90	GND	130	GND
11	AD27	51	GND	91	MAD13	131	MA2
12	AD26	52	AD7	92	IOC11	132	MA1
13	AD25	53	AD6	93	MAD14	133	MA0
14	AD24	54	AD5	94	IOC10	134	IOC3
15	GND	55	AD4	95	MAD15	135	IOC2
16	$\overline{\text{C\_BE3}}$	56	AD3	96	IOC9	136	$\overline{\text{READY}}$
17	IDSEL	57	AD2	97	MAD16	137	MARB_OUT
18	AD23	58	AD1	98	IOC8	138	MARB_IN
19	AD22	59	AD0	99	MAD17	139	$\overline{\text{ADS}}$
20	Vcc	60	Vcc	100	Vcc	140	Vcc
21	AD21	61	GND	101	GND	141	GND
22	AD20	62	MAD0	102	MA9	142	CLKIN
23	AD19	63	$\overline{\text{DCS0}}$	103	MAD18	143	IOC1
24	AD18	64	MAD1	104	MA8	144	IOC0
25	AD17	65	$\overline{\text{DCS1}}$	105	MAD19	145	$\overline{\text{DQM3}}$
26	AD16	66	MAD2	106	MA7	146	$\overline{\text{DQM2}}$
27	GND	67	$\overline{\text{DCS2}}$	107	MAD20	147	$\overline{\text{DQM1}}$
28	$\overline{\text{C\_BE2}}$	68	MAD3	108	MA6	148	$\overline{\text{DQM0}}$
29	$\overline{\text{FRAME}}$	69	$\overline{\text{DCS3}}$	109	MAD21	149	$\overline{\text{BLAST}}$
30	$\overline{\text{IRDY}}$	70	MAD4	110	GND	150	WNR
31	$\overline{\text{TRDY}}$	71	GND	111	MAD22	151	GND
32	$\overline{\text{DEVSEL}}$	72	MAD5	112	IOC7	152	CLKOUT
33	$\overline{\text{STOP}}$	73	$\overline{\text{MWE}}$	113	MAD23	153	$\overline{\text{RSTOUT}}$
34	$\overline{\text{PERR}}$	74	MAD6	114	IOC6	154	ALE
35	$\overline{\text{SERR}}$	75	$\overline{\text{CAS}}$	115	MAD24	155	SDA
36	PAR	76	MAD7	116	IOC5	156	SCL
37	Vcc	77	$\overline{\text{RAS}}$	117	MAD25	157	$\overline{\text{INT0}}$
38	$\overline{\text{C\_BE1}}$	78	MAD8	118	IOC4	158	$\overline{\text{INT1}}$
39	AD15	79	MA14	119	MAD26	159	$\overline{\text{INT2}}$
40	GND	80	GND	120	GND	160	$\overline{\text{INT3}}$

160-pin EIAJ PQFP Mechanical Drawing

Figure 4: 160-pin EIAJ PQFP Mechanical Drawing

Contact Information

Phone: (408) 990-4000 (US)

(905) 940-4149 (Canada)

+(44) 1932 57 9011 (Europe – except Germany/Benelux)

+(49) 89 930 86 170 (Germany/Benelux)

+(86) 21 6867 0273 (Asia – except Japan)

+(81) 45 470 5525 (Japan)

E-mail: info@quicklogic.com

Sales: www.quicklogic.com/sales

Support: www.quicklogic.com/support

Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
0.8	January 1999	First pre-silicon revision of preliminary data sheet.
0.9	March 2999	Updated Figure 2: Mechanical Drawing, Table 8: Local Bus Signals DC Operating Specifications, Table 10: Local Bus AC Test Conditions, and Table 12: Local Bus Signals AC Operating Specifications.
1.0	March 1999	First Release
1.1	June 2000	Updated TBA parameters.
E	August 2005	Mehul Kochar and Kathleen Murchek Updated to QuickLogic format standards. Updated Product Code table to include item V370PDC-66LPN REV A0.
F	November 2005	Mehul Kochar and Kathleen Murchek Added footnote that product code item V370PDC-66LPN REV A0 is lead-free.

Copyright and Trademark Information