OKI Semiconductor

MSM51257CLP

32,768-Word × 8-Bit CMOS STATIC RAM

DESCRIPTION

The MSM51257CLP is a 32,768-word by 8-bit CMOS static RAM featuring a 5 V power supply operation in the range of –40°C to 85°C and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257CLP, which uses NMOS cells and CMOS peripherals, can be used in high-speed operation at 70 ns access time and in the low current consumption of a standby current max. 100 µA when there is no chip selection. The MSM51257CLP's ability to hold the memory contents at 2 V provides a battery back-up. Since the MSM51257CLP is provided with the $\overline{CS}$ and $\overline{OE}$ signals, it can connect with outputs of other chips in a wired OR technique, which provides easy memory expansion and bus line control.

FEATURES

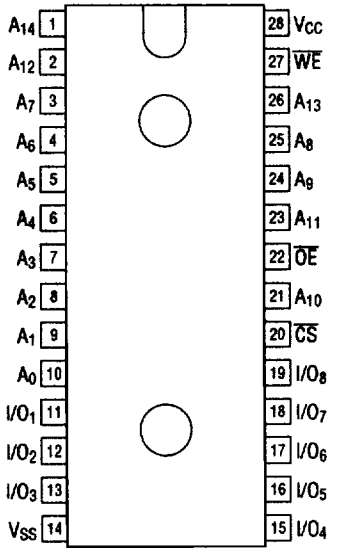
- 32,768-word × 8-bit configuration
- Single 5 V power supply
- Operating temperature range: Ta = –40°C to 85°C
- (Input/Output) TTL compatible
- 3-state output
- Data retention available at power supply voltage 2 V
- Package options:

28-Pin 600 mil plastic DIP	(DIP28-P-600)	(Product : MSM51257CLP-xxRS)
28-Pin 430 mil plastic SOP	(SOP28-P-430-K)	(Product : MSM51257CLP-xxGS-K)
32-Pin plastic TSOP (Type I)	(TSOP32-P-814-1K)	(Product : MSM51257CLP-xxTS-1K)
	(TSOP32-P-814-1L)	(Product : MSM51257CLP-xxTS-1L)
		xx indicates speed rank.

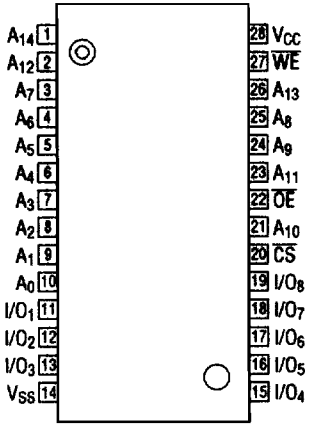
PRODUCT FAMILY

Family	Access Time (Max.)	Power Dissipation	
		Operating (Max.)	Standby (Max.)
MSM51257CLP-70	70 ns	385 mW	0.55 mW
MSM51257CLP-85	85 ns		
MSM51257CLP-10	100 ns		

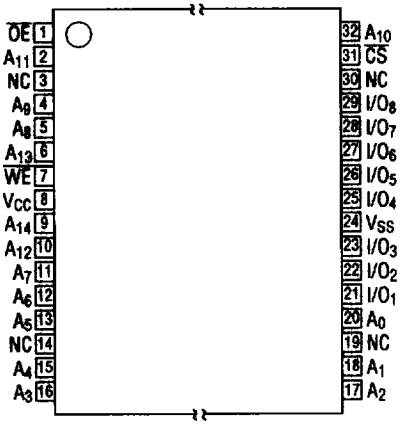
PIN CONFIGURATION (TOP VIEW)



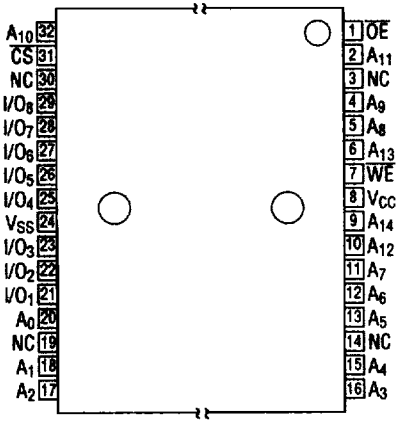
28-Pin Plastic DIP



28-Pin Plastic SOP



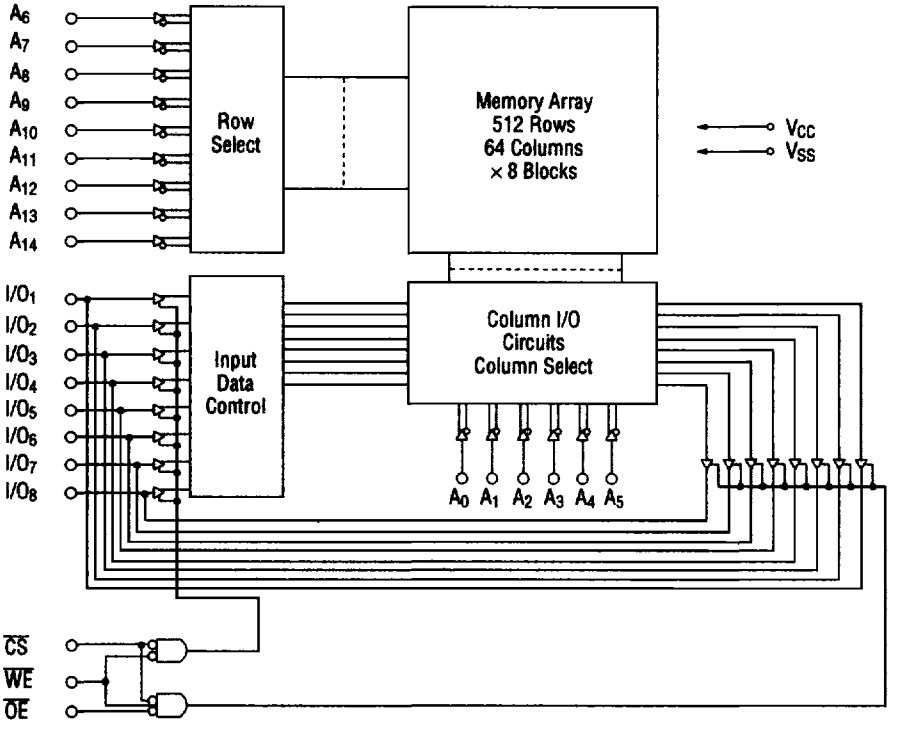
32-Pin Plastic TSOP (I)
(K Type)



32-Pin Plastic TSOP (I)
(L Type)

Pin Name	Function
A_0 - A_{14}	Address Input
I/O_1 - I/O_8	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}, V_{SS}	Power Supply
NC	No Connection

BLOCK DIAGRAM



FUNCTION TABLE

Operating Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Operating Contents
Standby	H	*	*	Output Floating
Read Cycle	L	H	H	Output Floating
	L	H	L	Data Read
Write Cycle	L	L	*	Data Write

*Don't Care ("H" or "L")

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}	Ta = 25°C, for V_{SS}	−0.3 to 7.0	V
Pin Voltage	V_T		−0.3* to V_{CC} + 0.3	V
Power Dissipation	P_D	Ta = 25°C	1.0	W
Operating Temperature	T_{opr}	—	−40 to 85	°C
Storage Temperature	T_{stg}	—	−55 to 150	°C

* −3.0 V Min. for pulse width less than 30 ns.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}		0	0	0	V
Data Retention Voltage	V_{CCH}	—	2	—	5.5	V
Input High Voltage	V_{IH}	V_{CC} = 5 V ±10%	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3*	—	0.8	V
Load Capacitance	C_L	—	—	—	100	pF
Fan Out	N	TTL	—	—	1	—

* −3.0 V Min. for pulse width less than 30 ns.

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	V_I = 0 V	—	10	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	10	pF

Note: This parameter is periodically sampled and not 100% tested.

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = −40°C to 85°C)

Parameter	Symbol	Condition	MSM51257CLP			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_I = 0 to V_{CC}	−1	—	1	µA
Input/Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}	−1	—	1	µA
Output High Voltage	V_{OH}	I_{OH} = −1 mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Standby Power Supply Current	I_{CCS}	$\overline{CS}$ ≥ V_{CC} − 0.2 V, V_I = 0 to V_{CC}	—	—	100	µA
	I_{CCS1}	$\overline{CS}$ = V_{IH}	—	—	3	mA
Operating Power Supply Current	I_{CCA}	Min. cycle, I_{OUT} = 0 mA	—	—	70	mA
		f = 1 MHz, V_{IH} ≥ V_{CC} − 0.2 V, V_{IL} ≤ 0.2 V, I_{OUT} = 0 mA	—	—	15	mA

AC Characteristics

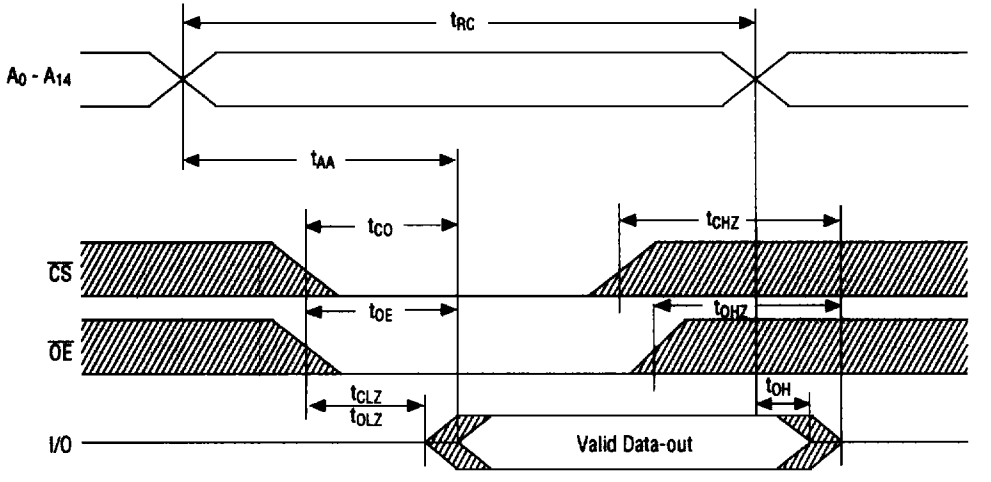
Test Conditions

Parameter	Condition
Input Pulse Level	V_{IH} = 2.4 V, V_{IL} = 0.6 V
Input Rise and Fall Times	5 ns
Input/Output Timing Level	1.5 V
Output Load	C_L = 100 pF, 1 TTL Gate

Read Cycle

(V_{CC} = 5 V ±10%, Ta = −40°C to 85°C)

Parameter	Symbol	MSM51257CLP-70		MSM51257CLP-85		MSM51257CLP-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	ns
$\overline{CS}$ Access Time	t_{CO}	—	70	—	85	—	100	ns
$\overline{OE}$ Access Time	t_{OE}	—	40	—	45	—	50	ns
$\overline{CS}$ to Output in Low-Z	t_{CLZ}	10	—	10	—	10	—	ns
$\overline{OE}$ to Output in Low-Z	t_{OLZ}	5	—	5	—	5	—	ns
Output Hold Time from Address Change	t_{OH}	10	—	10	—	10	—	ns
$\overline{CS}$ to Output in High-Z	t_{CHZ}	—	30	—	30	—	35	ns
$\overline{OE}$ to Output in High-Z	t_{OHZ}	—	30	—	30	—	35	ns

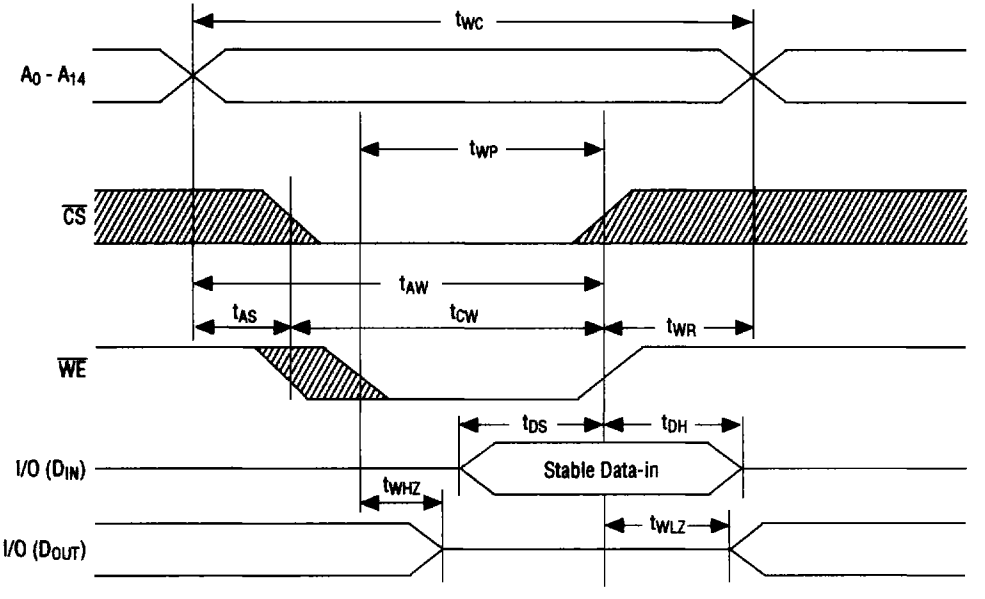


Notes: 1. A read cycle occurs during the overlap of $\overline{CS}$ = "L", $\overline{OE}$ = "L" and $\overline{WE}$ = "H".
2. t_{CHZ} and t_{OHZ} are specified by the time when DATA is floating, not defined by the output level.

Write Cycle

(V_{CC} = 5 V ±10%, Ta = −40°C to 85°C)

Parameter	Symbol	MSM51257CLP-70		MSM51257CLP-85		MSM51257CLP-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	55	—	70	—	75	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	5	—	ns
Data Setup Time	t_{DS}	35	—	40	—	40	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
$\overline{WE}$ to Output in High-Z	t_{WHZ}	—	30	—	30	—	35	ns
$\overline{CS}$ to End of Write	t_{CW}	65	—	75	—	90	—	ns
Address Valid to End of Write	t_{AW}	65	—	75	—	90	—	ns
Output Active from End of Write	t_{WLZ}	5	—	5	—	5	—	ns



Notes:
1. A write cycle occurs during the overlap of $\overline{CS}$ = "L" and $\overline{WE}$ = "L".
2. $\overline{OE}$ may be either of "H" or "L" in the write cycle.
3. t_{AS} is specified from $\overline{CS}$ = "L" or $\overline{WE}$ = "L", whichever occurs last.
4. t_{WP} is an overlap time of $\overline{CS}$ = "L" and $\overline{WE}$ = "L".
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ = "H" or $\overline{WE}$ = "H", whichever occurs first.
6. t_{WHZ} is specified by the time when DATA output is floating, not defined by the output level.
7. When I/O pins are in the output mode, don't apply the inverted input signal to the output pins.

Data Retention Characteristics

(Ta = −40°C to 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V_{CCH}	$\overline{CS} \geq V_{CC} - 0.2$ V	2.0	—	5.5	V
Data Retention Power Supply Current	I_{CCH}	$V_{CC} = 3$ V, $\overline{CS} \geq V_{CC} - 0.2$ V	—	—	50*	µA
Chip Deselect to Data Retention Time	t_{CDR}	—	0	—	—	ns
Operation Recovery Time	t_R	—	50	—	—	ms

* 7 µA Max. when Ta = 0°C to 40°C.