FAIRCHILD SEMICONDUCTOR™

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NC7SZ3157
TinyLogic™ Low Voltage UHS Analog Switch 2-Channel Multiplexer/Demultiplexer (Preliminary)

General Description

The NC7SZ3157 is a high performance, Analog Switch 2-channel CMOS multiplexer/demultiplexer from Fairchild's Ultra High Speed Series of TinyLogic™. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low on resistance. The break before make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The control input tolerates voltages up to 5.5V independent of the V_{CC} operating range.

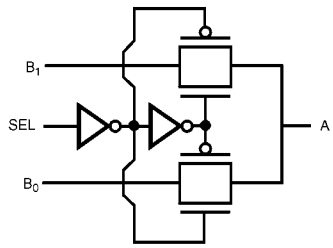
Features

- Useful in both analog and digital applications
- Space saving SC70 6-lead surface mount package
- Low on resistance; < 10Ω on typ @ 3.3V V_{CC}
- Broad V_{CC} operating range; 1.65V to 5.5V
- Power down high impedance control input
- Overvoltage tolerance of control input to 5.5V's
- Break before make disable-enable timing.

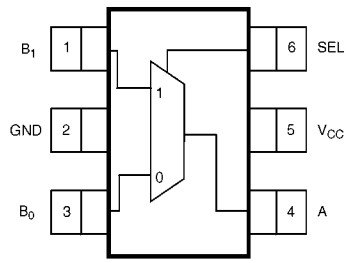
Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7SZ3157P6X	MAA06A	ZA7	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel

Logic Symbol



Connection Diagram



(Top View)

Pin Descriptions

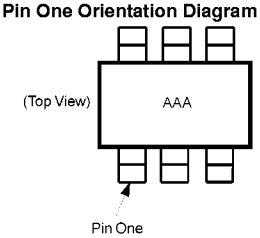
Pin Names	Description
A, B_0, B_1	Data Ports
SEL	Control Input

Function Table

Input (SEL)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level
L = LOW Logic Level

Pin One Orientation Diagram



AAA = Package Top Mark - see ordering code.

Note: Orientation of Top Mark determines Pin One location. Read the top package mark left to right, Pin One is the lower left pin (see diagram).

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Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
@ (I_{IK}) V_{IN} < 0V	−50 mA
DC Output Current (I_{OUT})	128 mA
DC V_{CC} or Ground Current (I_{CC}/I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	180 mW

Recommended Operating Conditions (Note 3)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Control Input Voltage (V_{IN})	0V to V_{CC}
Switch Input Voltage (V_{IN})	0V to V_{CC}
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
Control Input V_{CC} = 2.3V - 3.6V	0 ns/V to 10 ns/V
Control Input V_{CC} = 4.5V - 5.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	350°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Control input must be held HIGH or LOW, it must not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	1.65 – 1.95	0.75 V_{CC}			0.75 V_{CC}		V	
		2.3 – 5.5	0.7 V_{CC}			0.7 V_{CC}			
V_{IL}	LOW Level Input Voltage	1.65 – 1.95			0.25 V_{CC}		0.25 V_{CC}	V	
		2.3 – 5.5			0.3 V_{CC}		0.3 V_{CC}		
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1	µA	0 ≤ V_{IN} ≤ 5.5V
I_{OFF}	OFF State Leakage Current	1.65 – 5.5			±0.1		±1	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch ON Resistance (Note 4)	4.5		3	7		7	Ω	V_{IN} = 0V, I_{IN} = 30 mA
				5	12		12	Ω	V_{IN} = 2.4V, I_{IN} = 30 mA
				7	15		15	Ω	V_{IN} = 4.5V, I_{IN} = 30 mA
		3.0		4	9		9	Ω	V_{IN} = 0V, I_{IN} = 24 mA
				10	20		20	Ω	V_{IN} = 3V, I_{IN} = 24 mA
		2.3		5	12		12	Ω	V_{IN} = 0V, I_{IN} = 8 mA
				13	30		30	Ω	V_{IN} = 2.3V, I_{IN} = 8 mA
		1.65		TBD	TBD		TBD	Ω	V_{IN} = 0V, I_{IN} = 4 mA
				TBD	TBD		TBD	Ω	V_{IN} = 1.65V, I_{IN} = 4 mA
I_{CC}	Quiescent Supply Current All Channels ON or OFF	5.5			1		10	µA	V_{IN} = V_{CC} or GND I_{OUT} = 0
	Analog Signal Range	V_{CC}	0		V_{CC}	0	V_{CC}	V	
R_{RANGE}	ON Resistance Over Signal Range (Note 4)(Note 5)	1.65						Ω	I_A = −4 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		2.3							I_A = −8 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		3.0							I_A = −24 mA, 0 ≤ V_{Bn} ≤ V_{CC}
		4.5							I_A = −30 mA, 0 ≤ V_{Bn} ≤ V_{CC}
ΔR_{ON}	ON Resistance Match Between Channels (Note 4)(Note 5)(Note 6)	1.65						Ω	I_A = −4 mA, V_{Bn} = 1.15
		2.3							I_A = −8 mA, V_{Bn} = 1.6
		3.0							I_A = −24 mA, V_{Bn} 2.1
		4.5							I_A = −30 mA, V_{Bn} = 3.15

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
R_{flat}	On Resistance Flatness (Note 4)(Note 5)(Note 7)	1.8						Ω	$I_A = -4$ mA $0 \le V_{Bn} \le V_{CC}$
		2.5							$I_A = -8$ mA $0 \le V_{Bn} \le V_{CC}$
		3.3							$I_A = -24$ mA $0 \le V_{Bn} \le V_{CC}$
		5.0							$I_A = -30$ mA $0 \le V_{Bn} \le V_{CC}$
I_{B-OFF}	OFF Leakage Current	5.5			±0.1		±1	μA	$V_A = 1.0V$ or $4.5V$ $V_{Bn} = 4.5V$ or $1V$
I_{A-OFF}	OFF Leakage Current	5.5			±0.1		±1	μA	$V_A = 4.5V$ or $1.0V$ $V_{Bn} = 1.0V$ or $4.5V$

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).

Note 5: Parameter is characterized but not tested in production.

Note 6: $\Delta R_{ON} = R_{ON}$ max – R_{ON} min measured at identical V_{CC}, temperature and voltage levels.

Note 7: Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus (Note 9)	1.65 – 1.95			TBD		TBD	ns	V_I = OPEN	Figure 1 Figure 2
		2.3 – 2.7			1.2		1.2			
		3.0 – 3.6			0.8		0.8			
		4.5 – 5.5			0.3		0.3			
t_{PZL} t_{PZH}	Output Enable Time Turn on Time (A to B– or B– to A)	1.65 – 1.95			TBD		TBD	ns	$V_I = 2 \times V_{CC}$ for t_{PZL} $V_I = 0V$ for t_{PZH}	Figure 1 Figure 2
		2.3 – 2.7			15		15			
		3.0 – 3.6			10		10			
		4.5 – 5.5			7		7			
t_{PLZ} t_{PHZ}	Output Enable Time Turn Off Time (A Port to B Port)	1.65 – 1.95			TBD		TBD	ns	$V_I = 2 \times V_{CC}$ for t_{PLZ} $V_I = 0V$ for t_{PHZ}	Figure 1 Figure 2
		2.3 – 2.7			8		8			
		3.0 – 3.6			6		6			
		4.5 – 5.5			4		4			
t_{B-M}	Break Before Make Time (Note 8)	1.65 – 1.95	0.5		TBD	0.5	TBD	ns		Figure 3
		2.3 – 2.7	0.5		TBD	0.5	TBD			
		3.0 – 3.6	0.5		TBD	0.5	TBD			
		4.5 – 5.5	0.5		TBD	0.5	TBD			
Q	Charge Injection (Note 8)			TBD				pC	$C_L = 1$ nF, $V_{GEN} = 0V$ $R_{GEN} = 0Ω$	Figure 4
OIRR	Off Isolation (Note 10)			TBD				dB	$R_L = 50Ω$, $C_L = 5$ pF f = 10MHz	Figure 5
Xtalk	Crosstalk			TBD				dB	$R_L = 50Ω$, $C_L = 5$ pF f = 10MHz	Figure 6
BW	–3dB Bandwidth			TBD				MHz	RL = 50Ω	Figure 9

Note 8: Guaranteed by Design.

Note 9: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

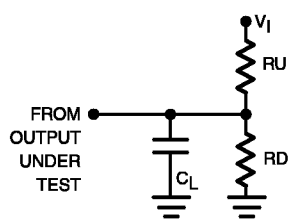
Note 10: Off Isolation = 20 $\log_{10}$ [V_A / V_{Bn}]

Capacitance (Note 11)

Symbol	Parameter	Typ	Max	Units	Conditions	Figures
C_{IN}	Control Pin Input Capacitance	2	TBD	pF	V_{CC} = 0V	
C_{IO-B}	B Port Off Capacitance	6	TBD	pF	V_{CC} = 5.0V	Figure 7
C_{IOA-ON}	A Port Capacitance when switch is enabled		TBD	pF	V_{CC} = 5.0V	Figure 8

Note 11: TA = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz; t_W = 500 ns

FIGURE 1. AC Test Circuit

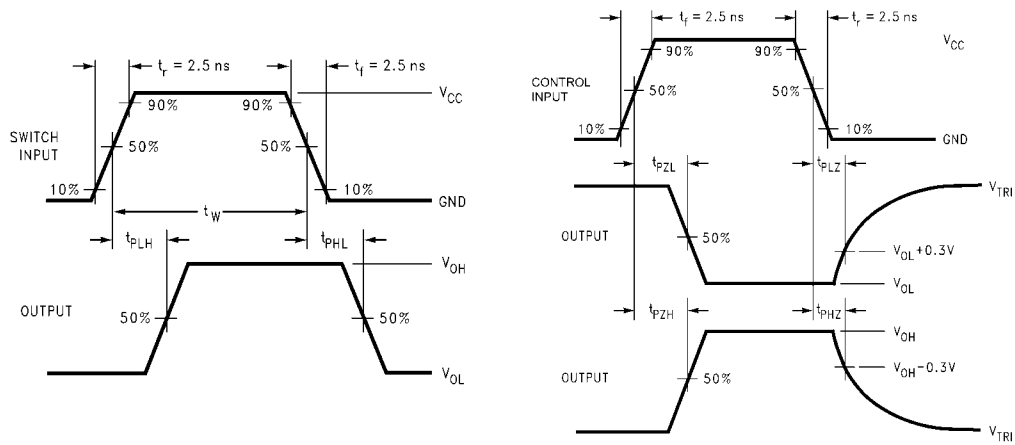


FIGURE 2. AC Waveforms

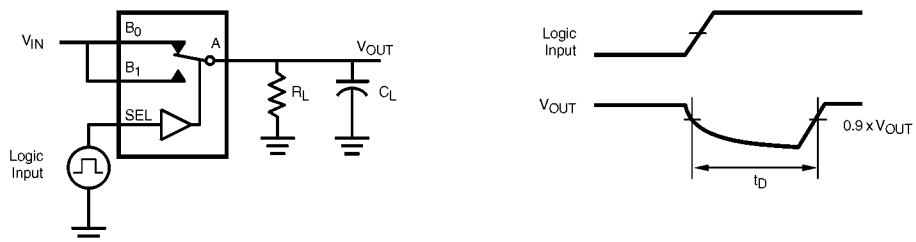


FIGURE 3. Break Before Make Interval Timing

AC Loading and Waveforms (Continued)

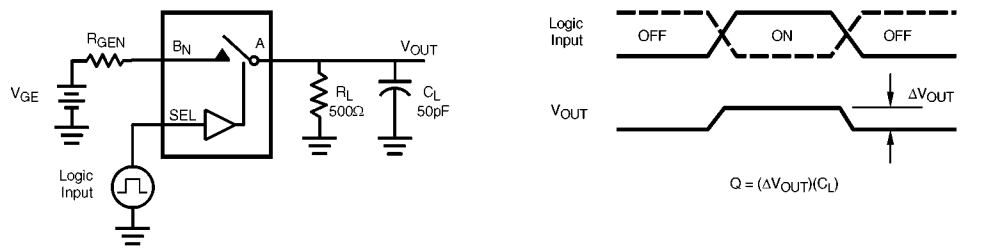


FIGURE 4. Charge Injection Test

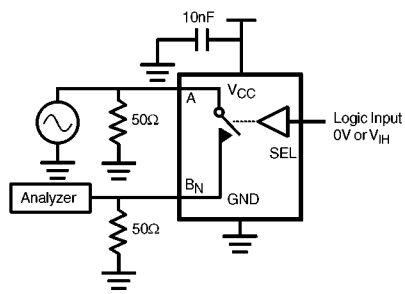


FIGURE 5. Off Isolation

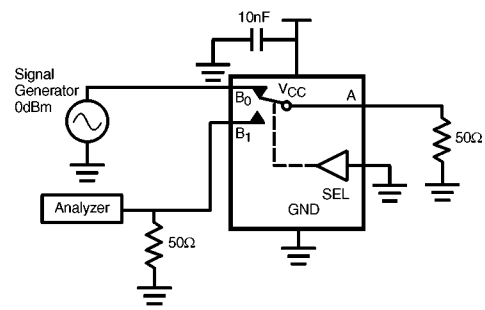


FIGURE 6. Crosstalk

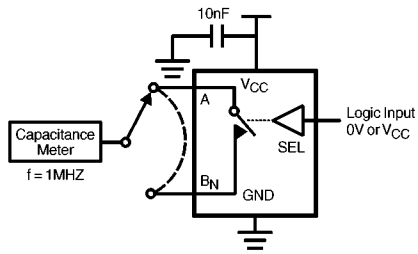


FIGURE 7. Channel Off Capacitance

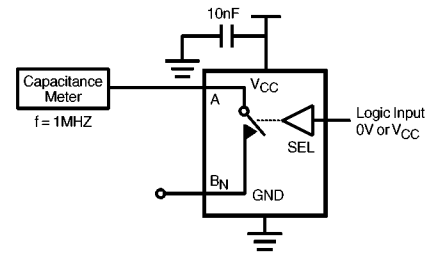


FIGURE 8. Channel On Capacitance

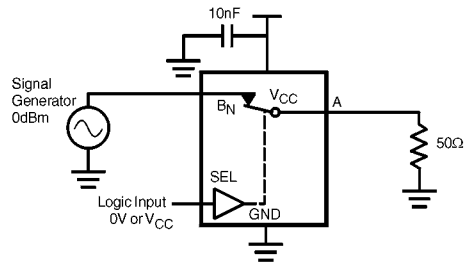


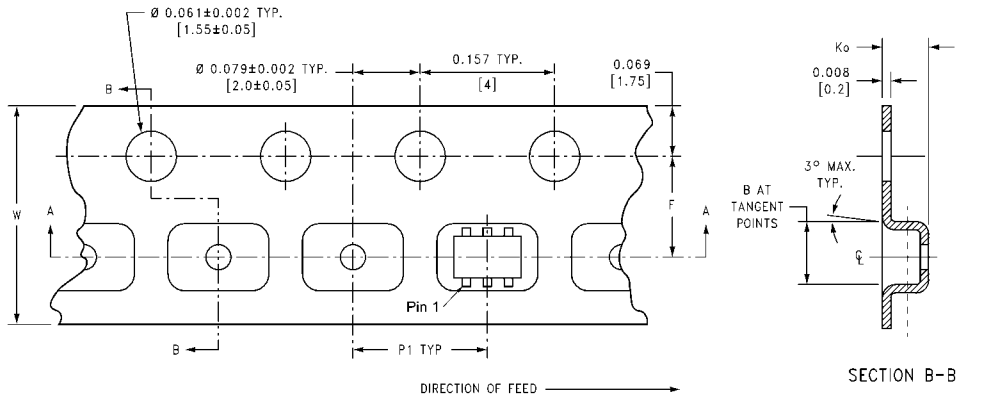
FIGURE 9. Bandwidth

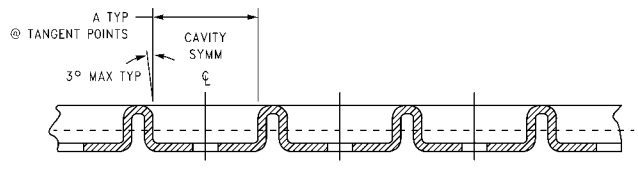
Tape and Reel Specification

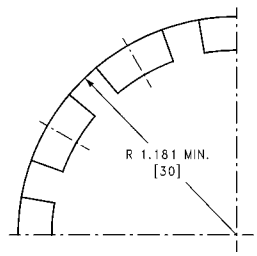
TAPE FORMAT

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

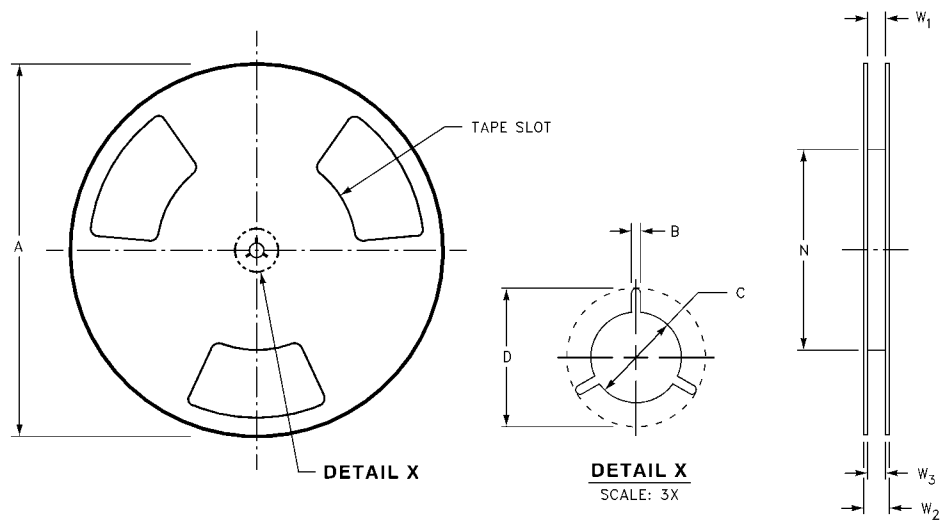






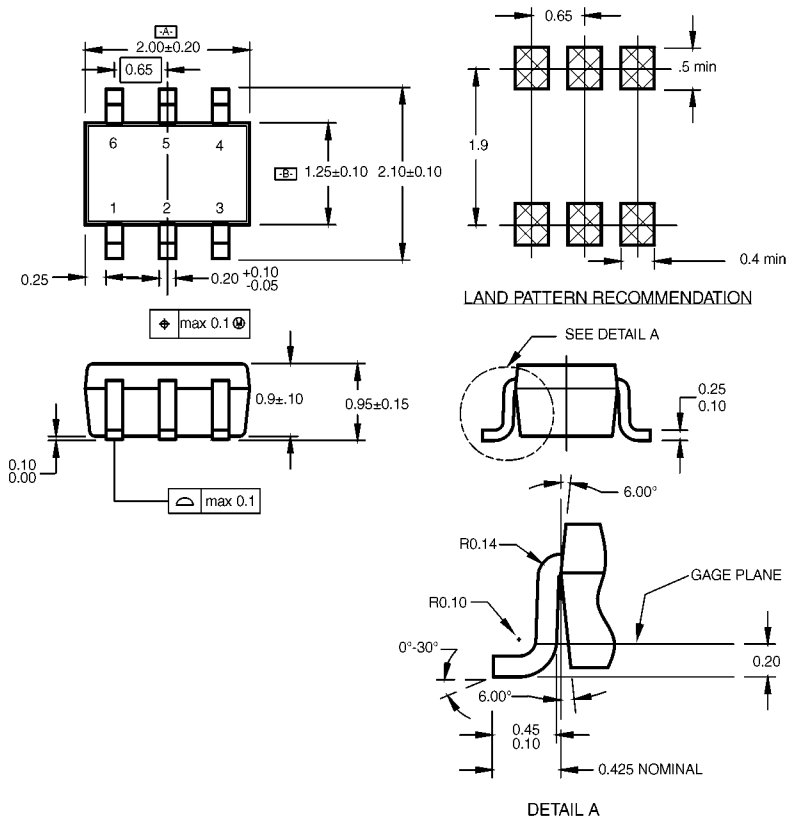
Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A

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