STATIC RAM 1M × 9 9M BIT

Type name	Max. Access time (ns)	Load memory	Outward dimensions W × H × D (mm)	Data sheet page
MH1M09AN-85L	85	M5M51008AFP × 8 + M5M51001J × 1	107.95 × 29.88 × 8.4	3/9
MH1M09AN-10L	100			
MH1M09AN-12L	120			
MH1M09AN-15L	150			
MH1M09AN-85H	85			
MH1M09AN-10H	100			
MH1M09AN-12H	120			
MH1M09AN-15H	150			
MH1M09ANZ-85L	85		100.33 × 29.9 × 8.4	
MH1M09ANZ-10L	100			
MH1M09ANZ-12L	120			
MH1M09ANZ-15L	150			
MH1M09ANZ-85H	85			
MH1M09ANZ-10H	100			
MH1M09ANZ-12H	120			
MH1M09ANZ-15H	150			
COMMON DATA				4/9

MH1M09AN-85L,-10L,-12L,-15L,-85H,-10H,-12H,-15H/ MH1M09ANZ-85L,-10L,-12L,-15L,-85H,-10H,-12H,-15H

9437184-BIT (1048576-WORD BY 9-BIT) CMOS STATIC RAM

DESCRIPTION

The MH1M09AN/ANZ is 9437184-bit CMOS static RAM organized as 1048576-word by 9-bit. It consists of eight industry standard 128K × 8 static RAMs and a industry standard 1M × 1 static RAM and a decoder.

It is mounted a SOP package and a SOJ package on a 72-pin single in-line package and 70-pin zig-zag in-line package.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH1M09AN-85L MH1M09ANZ-85L	85ns	254mA	500μA (Vcc=3.0V)
MH1M09AN-10L MH1M09ANZ-10L	100ns		
MH1M09AN-12L MH1M09ANZ-12L	120ns		
MH1M09AN-15L MH1M09ANZ-15L	150ns		
MH1M09AN-85H MH1M09ANZ-85H	85ns		180μA (Vcc=3.0V)
MH1M09AN-10H MH1M09ANZ-10H	100ns		
MH1M09AN-12H MH1M09ANZ-12H	120ns		
MH1M09AN-15H MH1M09ANZ-15H	150ns		

- Single 5V power supply
- No clicks, no refresh
- Simple memory expansion by $\overline{S}$
- MH1M09AN ····· Gold plating contact
  MH1M09ANZ ····· Solder dipping lead

APPLICATION

Small capacity memory units

MH1M09AN
MH1M09ANZ

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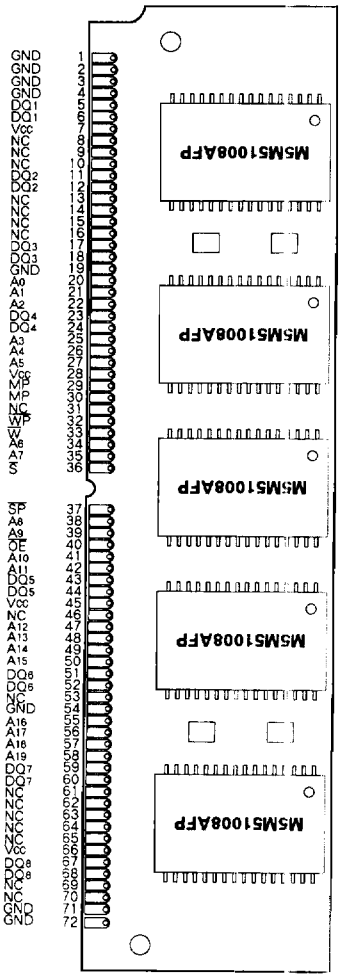
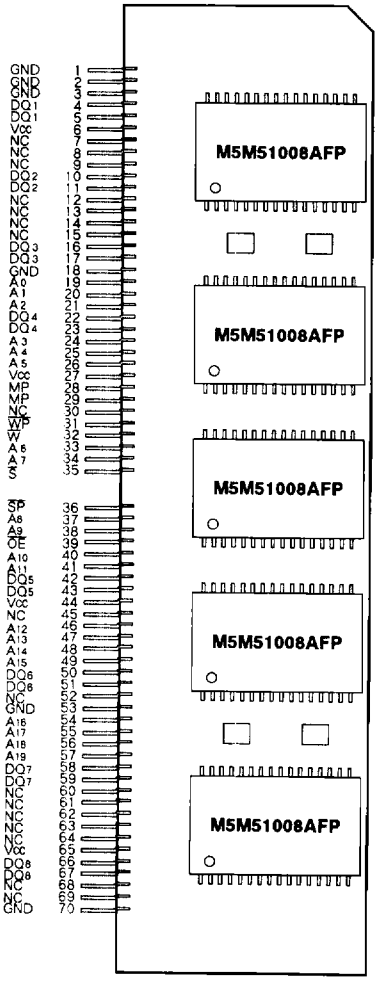
PIN CONFIGURATION (TOP VIEW) (Both side)



Outline 72N9K-B (MH1M09AN)



Outline 70N5 (MH1M09ANZ)

NC : NO CONNECTION

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FUNCTION

The operation mode of the MH1M09AN / ANZ are determined by a combination of the device control inputs $\overline{Sn}$, $\overline{SPn}$ $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$, $\overline{SP}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$ or $\overline{SP}$ whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

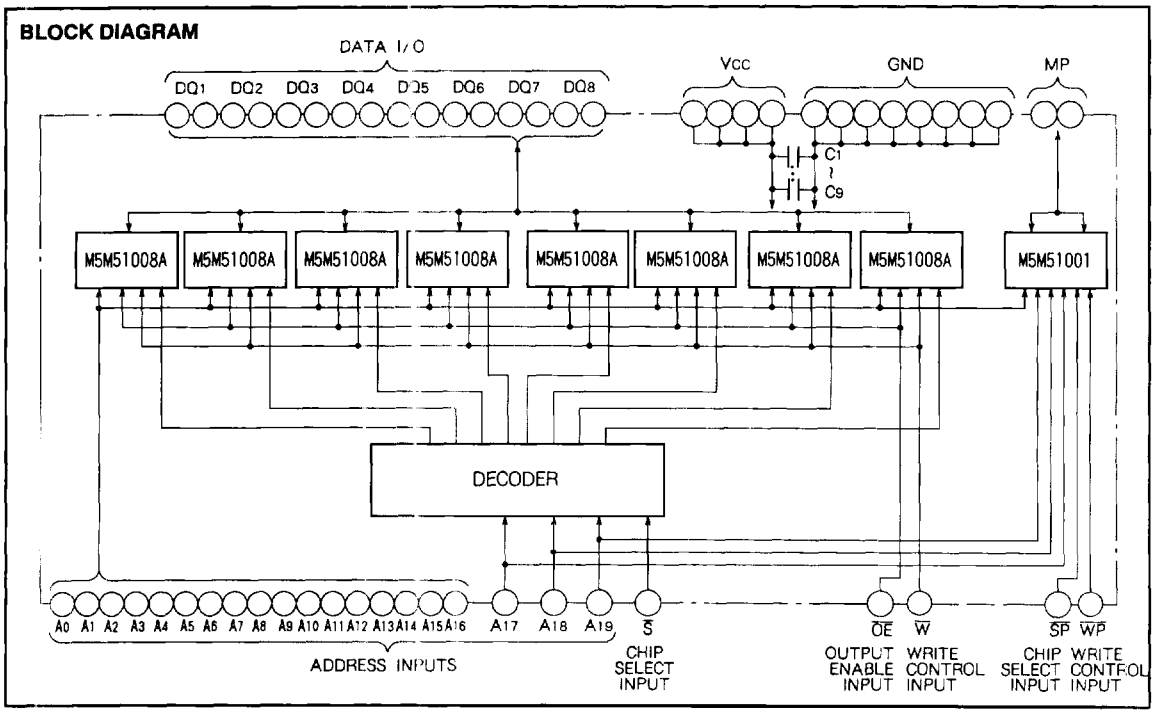
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ and $\overline{SP}$ are in an active state.

When setting $\overline{S}$ at a high level or $\overline{SP}$ at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output state is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$ and $\overline{SP}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$, $\overline{SP}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non-selection	High-impedance	Stand-by
L	L	X	Write	DIN	Active
L	H	L	Read	DOUT	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3~7	V
V_I	Input voltage	With respect to GND	− 0.3*~V_{CC}	V
V_O	Output voltage	With respect to GND	0~V_{CC}	V
P_d	Power dissipation	T_a = 25℃	1.7	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 40~125	℃

* − 3.0V incase of AC (Pulse width ≦ 50ns)

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			− 0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = − 1mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				±9	μA
I_O	Output current in off-state	$\overline{S}$, $\overline{SP}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				±10	μA
I_{CC1}	Active supply current (AC. MOS level)	$\overline{S}$, $\overline{SP}$ ≦ 0.2V, other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V, output open (duty 100%)	Min cycle			249	mA
I_{CC2}	Active supply current (AC. TTL level)	$\overline{S}$, $\overline{SP}$ = V_{IL} other inputs = V_{IH} or V_{IL} output open (duty 100%)	Min cycle			254	mA
I_{CC3}	Stand by current	$\overline{S}$, $\overline{SP}$ ≧ V_{CC} − 0.2V other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V	N/NZ-L			900	μA
			N/NZ-H		18	260	
I_{CC4}	Stand by current	$\overline{S}$, $\overline{SP}$=V_{IH}, other inputs≧V_{IH} or ≦ V_{IL}				54	mA

* − 3.0V incase of AC (Pulse width ≦ 50ns)

CAPACITANCE (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_i = 25mVrms, f = 1MHz			85	pF
C_O	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz			85	pF

Note 1. Direction for current flowing into an IC is positive (no mark).
2. Typical value is V_{CC} = 5V, T_a = 25℃.

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AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall time ····· 5ns
Reference levels ····· V_{OH} = V_{OL} = 1.5V
Transition is measured ±500mV from steady state voltage.(for t_{en}, t_{dis})
Output loads ····· Fig.1 C_L = 100pF (-10L,-12L,-15L,-10H,-12H,-15H)
C_L = 30pF (-85L,-85H)
C_L = 5pF (for t_{en}, t_{dis})

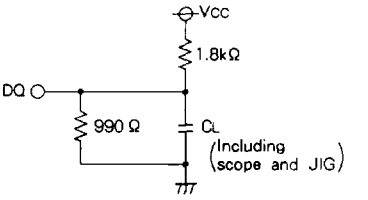

Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits								Unit
		MH1M09AN/NZ -85L, -85H		MH1M09AN/NZ -10L, -10H		MH1M09AN/NZ -12L, -12H		MH1M09AN/NZ -15L, -15H		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	85		100		120		150		ns
$t_{a(A)}$	Address access time		85		100		120		150	ns
$t_{a(S)}$	Chip select access time		85		100		120		150	ns
$t_{a(SP)}$	Chip select access time		85		100		120		150	ns
$t_{a(OE)}$	Output enable access time		50		60		65		75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		40		45		50		55	ns
$t_{dis(SP)}$	Output disable time after $\overline{SP}$ high		40		45		50		55	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		40		45		50		55	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	10		10		10		10		ns
$t_{en(SP)}$	Output enable time after $\overline{SP}$ low	10		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits								Unit
		MH1M09AN/NZ -85L, -85H		MH1M09AN/NZ -10L, -10H		MH1M09AN/NZ -12L, -12H		MH1M09AN/NZ -15L, -15H		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	85		100		120		150		ns
$t_{w(W)}$	Write pulse width	55		65		75		85		ns
$t_{su(A)}$	Address set up time	0		0		0		0		ns
$t_{su(A-\overline{WH})}$	Address set up time with respect to $\overline{W}$ high	65		75		85		100		ns
$t_{su(S)}$	Chip select set up time	80		90		100		115		ns
$t_{su(SP)}$	Chip select set up time	80		90		100		115		ns
$t_{su(D)}$	Data set up time	30		35		40		45		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		30		35		40	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		30		35		40	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		5		ns

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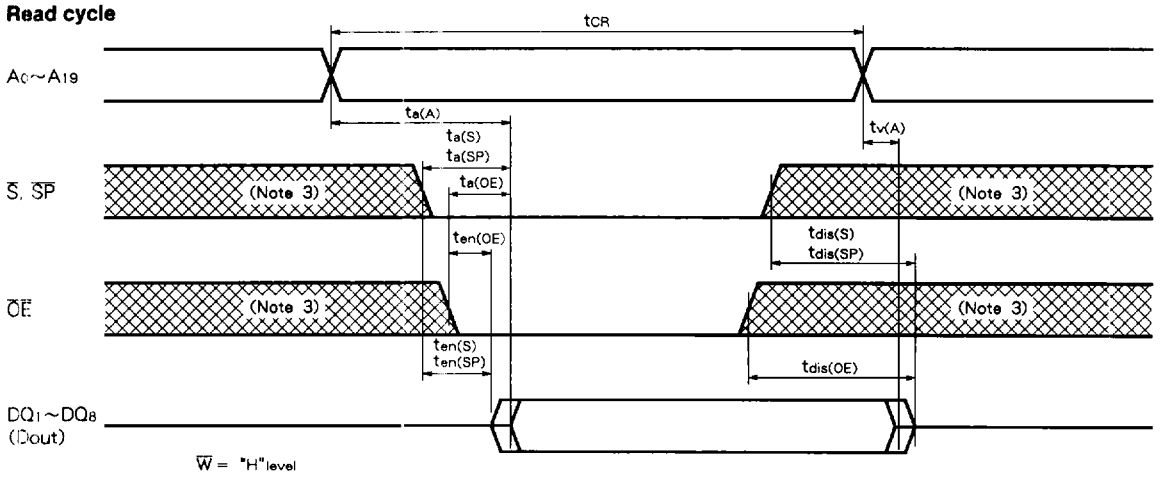
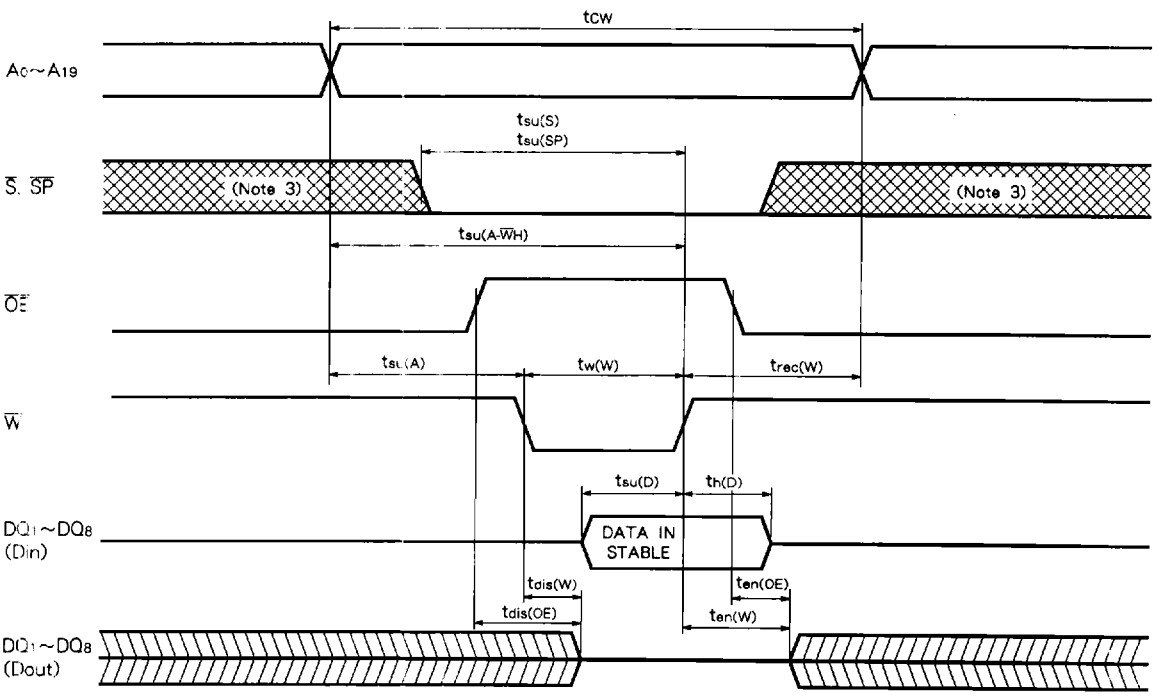
(4) TIMING DIAGRMS

Read cycle



Write cycle ($\overline{W}$ control mode)



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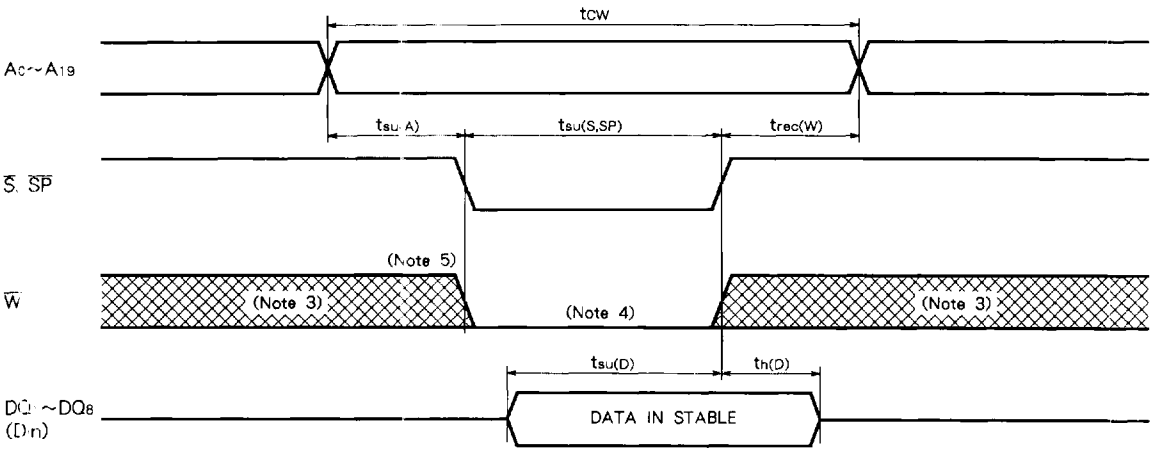
Write cycle ($\overline{S}$, $\overline{SP}$ control mode)



Note 3. Hatching indicates the state is don't care.
4. Writing is executed in overlap $\overline{S}$ and $\overline{W}$ low.
5. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
6. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S}, \overline{SP})}$	Chip select input $\overline{S}$, $\overline{SP}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC}=3V, A_{17}~A_{19}=V_{CC} or 0V $\overline{S}$, $\overline{SP}$ ≧ V_{CC}-0.2V, Other inputs ≦0.2V or ≧V_{CC}-0.2V	N/NZ-L			500	μA
			N/NZ-H			180 (Note 7)	

Note 7. $I_{CC(PD)}$ = 18(μA) in case of Ta = 25℃
* When $\overline{S}$ is at 2.2V(V_{IH} min) and supply voltage is at any level between 4.5V and 2.4V, supply current is defined as I_{CC4}.

TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

POWER DOWN CHARACTERISTICS