LCD Panel Timing Controller (15")

GENERAL DESCRIPTION

CS5842 is a TFT-LCD timing controller, which is applicable to 8-bit data XGA (1024*768), SXGA (1280*1024).

CS5842 can update the response timing for display mode of XGA and SXGA automatically.

CS5842 provides a selectable polarity check function to inverse output data for EMI reducing, when the toggle number of ODD/EVEN RGB outputs is larger than 13.

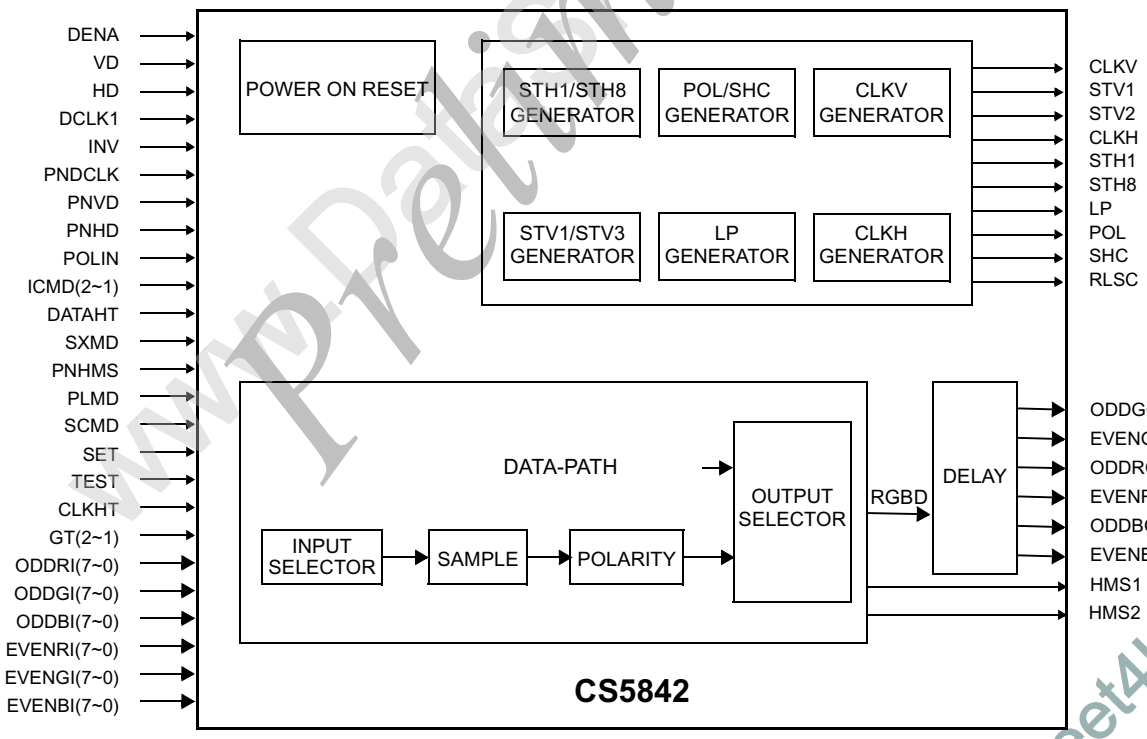
FEATURES

- Interface (5V/3.3V[CMOS] input, 3.3V[CMOS] output)
- Single (XGA2: 65MHz)/dual (XGA: 32.5MHz) 8-bit Data input; dual port 8-bit output; SXGA auto detective
- Timing adjustable for horizontal clock output

FEATURES (continued)

- Correspondent to control timing & specific resolution for different Driver IC by changing a Mask:
  1. can vary the pulse width & starting position of LP signal and POL signal polarity position changed along with LP signal
  2. can vary the pulse width & starting position of CLKV signal and tgs time
- Control ASIC output timing design is based on Data Enable signals
- Embedded Power On Reset circuits, Vth=2.1V, tolerance ± 0.3V
- ESD spec. 4KV
- Power On Latch Up 200mA/6.6V
- Single 3.3V supply
- 144-pin LQFP package

BLOCK DIAGRAM



Century Semiconductor, Inc.
Taiwan:
No. 2, Industry East Rd. 3rd,
Science-Based Industrial Park, Hsin-Chu, Taiwan
Tel: 886-3-5784866 Fax: 886-3-5784349

USA:
1485 Saratoga Ave. #200
San Jose, CA, 95129
Tel: 408-973-8388 Fax: 408-973-9388

Sales@century-semi.com
Sales@century-semi.com.tw
www.century-semi.com

PIN CONNECTION DIAGRAM

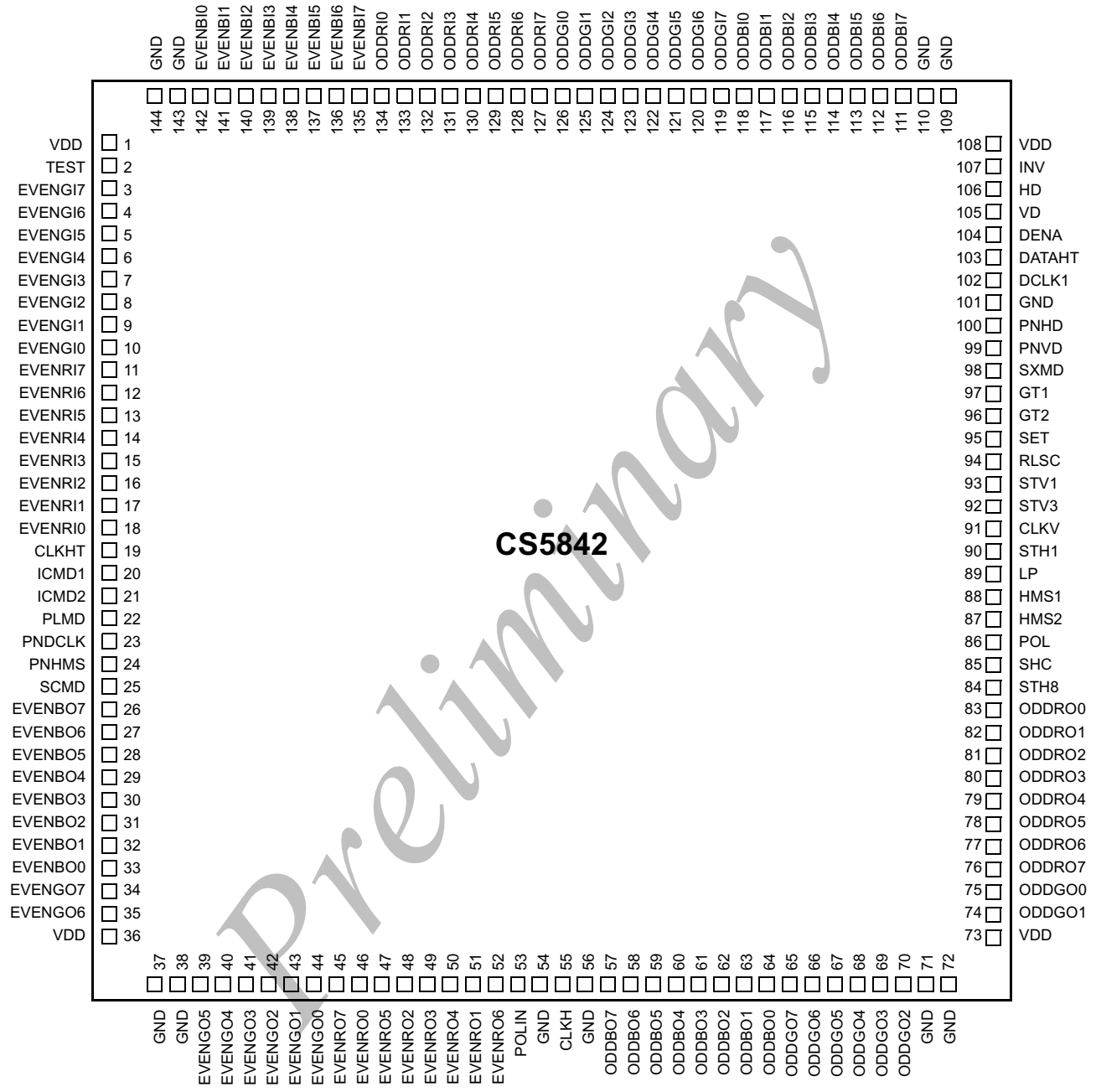


Figure-1 144-pin LQFP

PIN DESCRIPTION

Name	I/O	Pin	Block Type	Description	Note
VDD		1		Supply 3.3V ± 10%	
TEST	I	2	P5INPHU	TEST pin, usually open	Open
EVENGI(7-0)	I	3-10	P5INPMN	EVEN green pixel data input. (EVENGI0: LSB, EVENGI7:MSB) (DCLK1 synchronized; low as XGA2 mode.)	XGA:16.25MHz 5V tolerant
EVENRI(7-0)	I	11-18	P5INPMN	EVEN red pixel data input. (EVENRI0: LSB, EVENRI7: MSB) (DCLK1 synchronized; low as XGA2 mode.)	XGA:16.25MHz 5V tolerant
CLKHT	I	19	P5INPHU	Adjust CLKH TIMING output. 1. CLKHT=LOW, 0.0ns delay 2. CLKHT=OPEN, 3.3ns delay	20kΩ pull up (CLKHT:0Ω)
ICMD(1-2)	I	20-21	P5INPHU	Source Driver IC selection (ICMD:LSB, ICMD2:MSB) 1. ICMD2 = OPEN, ICMD1 = LOW, (10): IC1 (NECμPD16750, Hitachi HD66350T) 2. ICMD2 = OPEN, ICMD1 = OPEN, (11): IC2 (Toshiba T6L64C, Sharp LH168R) 3. ICMD2 = LOW, ICMD1 = LOW, (00): IC3 (Winbond WFP6815) 4. ICMD2 = LOW, ICMD1 = OPEN, (01): IC4 (T.I.TMS57571)	20kΩ pull up (ICMD1:0Ω ICMD2:OPEN)
PLMD	I	22	P5INPHU	Polarity invert signal. 1. PLMD = OPEN: TWO LINE inverted 2. PLMD = LOW: ONE LINE inverted	20kΩ pull up (0Ω)
PNDCLK	I	23	P5INPHU	Input CLOCK signal polarity switch input. LOW = inverted OPEN = non-inverted	20kΩ pull up (OPEN)
PNHMS	I	24	P5INPHU	HMS input invert switch output. OPEN = non-inverted LOW = invert output signal of HMS1 and HMS2.	20kΩ pull up (0Ω)
SCMD	I	25	P5INPHD	Controlling PIN of DRIVER IC R/L PIN OPEN: RLSC = HIGH⇒ output STV1, STH1; STV3, STH8: no output (low) HIGH: RLSC = LOW⇒ output STV3, STH8; STV1, STH1: no output (low)	
EVENBO(7-0)	O	26-33	P3OUTRB	EVEN blue pixel output (EVENBO0:LSB, EVENBO7:MSB)	XGA:16.25MHz
EVENGO(7-6)	O	34-35	P3OUTRB	EVEN green pixel output (EVENGO0:LSB, EVENGO7:MSB)	XGA:16.25MHz
VDD		36		Power 3.3V ± 10%	
GND		37		Ground.	
GND		38		Ground.	

Name	I/O	Pin	Block Type	Description	Note
EVENGO(5-0)	O	39-44	P3OUTRB	EVEN green pixel output (EVENGO0:LSB, EVENGO7:MSB)	XGA:16.25MHz
EVENRO7	O	45	P3OUTRB	EVEN red pixel output (EVENRO7:MSB)	XGA:16.25MHz
EVENRO0	O	46	P3OUTRB	EVEN red pixel output (EVENRO0:LSB)	XGA:16.25MHz
EVENRO5	O	47	P3OUTRB	EVEN red pixel output	XGA:16.25MHz
EVENRO2	O	48	P3OUTRB	EVEN red pixel output	XGA:16.25MHz
EVENRO3	O	49	P3OUTRB	EVEN red pixel output	XGA:16.25MHz
EVENRO4	O	50	P3OUTRB	EVEN red pixel output	XGA:16.25MHz
EVENRO1	O	51	P3OUTRB	EVEN red pixel output	XGA:16.25MHz
EVENRO6	O	52	P3OUTRB	EVEN red pixel output	XGA:16.25MHz
POLIN	I	53	P5INPHU	HMS polarity function calculation switch set. 1. POLIN = OPEN: calculated; HMS1, HMS2 calculated separately. 2. POLIN = LOW: un-calculated; HMS1 = HMS2 = INV	20kΩ pull up (OPEN)
GND		54		Ground	
CLKH	O	55	P3OUTRD	SHIFT clock output used by Source driver IC.	XGA:32.25MHz
GND		56		Ground	
ODDBO(7-0)	O	57-64	P3OUTRB	ODD blue pixel output. (ODDBO0: LSB, ODDBO7: MSB)	XGA:16.25MHz
ODDGO(7-2)	O	65-70	P3OUTRB	ODD green pixel output. (ODDGO0: LSB, ODDGO7: MSB)	XGA:16.25MHz
GND		71		Ground	
GND		72		Ground	
VDD		73		Supply 3.3V± 10%	
ODDGO(1-0)	O	74-75	P3OUTRB	ODD green pixel output. (ODDGO0: LSB; ODDGO7: MSB)	XGA:16.25MHz
ODDRO(7-0)	O	76-83	P3OUTRB	ODD red pixel output. (ODDRO0: LSB; ODDRO7: MSB)	XGA:16.25MHz
STH8	O	84	P3OUTRB	START PULSE (S8→ S1) of Source Driver IC	
SHC	O	85	P3OUTRB	Signal for T.I.	
POL	O	86	P3OUTRB	Polarity invert signal of Source Driver IC	
HMS(2-1)	O	87-88	P3OUTRB	Data polarity invert control signal output. Output is based on POLIN set.	
LP	O	89	P3OUTRB	Latch Pulse of Source Driver IC.	

Name	I/O	Pin	Block Type	Description	Note
STH1	O	90	P3OUTRB	START PULSE (S1→ S8) of Source Driver IC.	
CLKV	O	91	P3OUTRB	SHIFT CLOCK output for Gate Driver IC.	
STV3	O	92	P3OUTRB	START PULSE (G3→ G1) of Gate Driver IC.	
STV1	O	93	P3OUTRB	START PULSE (G1→ G3) of Gate Driver IC.	
RLSC	O	94	P3OUTRB	R/L Output for Source Driver IC.	
SET	I	95	P5INPHU	ASIC internal reset setting. LOW = initialization, is usually OPEN.	20kΩ pull up (OPEN)
GT(2-1)	I	96-97	P5INPHU	Adjust CLKV Clock Timing (GT1: LSB; GT2: MSB). 1. ICMD2 = OPEN, ICMD1 = LOW: IC1 CLKV rising edge generated before LP falling edge. 4 steps: 0.5 μs (i.e. 17CLKH) each step, 2.5~4.0μs 2. ICMD2 = OPEN, ICMD1 = OPEN: IC2 CLKV rising edge generated before LP rising edge. 4 steps: 0.5 μs (i.e. 17CLKH) each step, 2.5~4.0μs 3. ICMD2 = LOW, ICMD1 = LOW: IC3 CLKV rising edge generated before LP falling edge. 4 steps: 0.5 μs (i.e. 17CLKH) each step, 2.5~4.0μs 4. ICMD2 = LOW, ICMD1 = OPEN: IC4 CLKV rising edge generated before LP falling edge. 4 steps: 0.5 μs (i.e. 17CLKH) each step, 2.5~4.0μs	20kΩ pull up (GT1:OPEN GT2:0Ω default: 01 ⇒ 3μs)
SXMD	I	98	P5INPHU	XGA/XGA2 switch selection SXMD = OPEN; XGA(32.5MHz) SXMD = LOW; XGA2(65MHz)	20kΩ pull up (OPEN)
PNVD	I	99	P5INPHU	Vertical sync signal polarity setting. Low = inverted; Open = non-inverted.	20kΩ pull up (OPEN)
PNHD	I	100	P5INPHU	Horizontal sync signal polarity setting. Low = inverted; Open = non-inverted.	20kΩ pull up (OPEN)
GND		101		Ground	
DCLK1	I	102	P5INPMN	Dot Clock input.	XGA: 32.5MHz 5V tolerant
DATAHT	I	103	P5INPHU	Adjust Data output Timing 1. DATAHT = OPEN 0.0ns/2.2ns/3.2ns delay 2. DATAHT = LOW 0.0ns/2.2ns/4.4ns delay	20kΩ pull up (OPEN)
DENA	I	104	P5INPMN	Data Enable signal input. DCLK1 synchronized.	5V tolerant
VD	I	105	P5INPMN	Vertical sync signal input. DCLK1 synchronized.	5V tolerant
HD	I	106	P5INPMN	Horizontal sync signal input. DCLK1 synchronized.	5V tolerant
INV	I	107	P5INPMN	Data input of polarity control. High = polarity of input data been inverted. Low = polarity of input data not been inverted.	5V tolerant

Name	I/O	Pin	Block Type	Description	Note
VDD		108		Supply 3.3V ± 10%.	
GND		109		Ground	
GND		110		Ground	
ODDBI(7-0)	I	111-118	P5INPMN	ODD blue pixel data input. (ODDBI0: LSB; ODDBI7: MSB) DCLK1 synchronized	XGA:16.25MHz 5V tolerant
ODDGI(7-0)	I	119-126	P5INPMN	ODD green pixel data input. (ODDGI0: LSB; ODDGI7: MSB) DCLK1 synchronized	XGA:16.25MHz 5V tolerant
ODDRI(7-0)	I	127-134	P5INPMN	ODD red pixel data input. (ODDRI0: LSB; ODDRI7: MSB) DCLK1 synchronized	XGA:16.25MHz 5V tolerant
EVENBI(7-0)	I	135-142	P5INPMN	EVEN blue pixel data input. (EVENBI0: LSB; EVENBI7: MSB) (DCLK1 synchronized; low as XGA2 mode.)	XGA:16.25MHz 5V tolerant
GND		143		Ground	
GND		144		Ground	

Operating Environment

Maximum operating frequency: 80MHz
Clock duty: 50 ±10%
Voltage range: 3.3 ± 0.3V
Operating temperature range: -40~85°C (storage temperature range: -65~150°C).

ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings:

Symbol	Parameter	Condition	Range	Unit
V_{DD}	Power		-0.5 ~ +4.6	V
V_I	Signal input voltage	5V tolerant buffer	-0.5 ~ +4.6 & V_1< V_{DD}+0.5	V
V_I	Signal input voltage	5V tolerant buffer	-0.5 ~ +6.6 & V_1< V_{DD}+3.0	V
V_O	Signal output voltage	Output buffer	-0.5 ~ +4.6 & V_1< V_{DD}+0.5	V
I_O	Signal output current	I_{OL} = 6mA type	20	mA
I_O	Signal output current	I_{OL} = 8mA type	30	mA
I_O	Signal output current	I_{OL} = 12mA type	40	mA
T_A	Operating ambient		-40 ~ +85	°C
T_{STG}	Storage temperature		-65 ~ +150	°C

Note: The component will be damaged if exceed the absolute maximum condition. Normal function operating condition is as below:

2. Normal operating condition:

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Power		3.0	3.3	3.6	V
T_A	Operating ambient		-40		85	°C
V_{IH}	High level input voltage	5V tolerant buffer	2.0		V_{DD}	V
V_{IL}	Low level input voltage	5V tolerant buffer	0		0.8	V
V_P	Positive trigger voltage	5V tolerant SCHMITTER buffer	1.40		2.40	V
V_N	Negative trigger voltage	5V tolerant SCHMITTER buffer	0.8		1.6	V
V_H	Hysteresis voltage	5V tolerant SCHMITTER buffer	0.3		1.5	V
V_{IH}	High level input voltage	5V tolerant buffer	2.0		5.5	V
V_{IL}	Low level input voltage	5V tolerant buffer	0		0.8	V
Tri	Input Rising Time	Normal input	0		200	ns
Tfi	Input Falling Time	Normal input	0		200	ns
Tri	Input Rising Time	Schmitter input	0		10	ms
Tfi	Input Falling Time	Schmitter input	0		10	ms

Note: Under normal operation, the function of ASIC IC must be normal; Schmitter buffer is the buffer of hysteresis characteristic.

3. DC Characteristic

(T_A = -40°C ~ +85°C, V_{DD} = 3.3V ± 0.3V; (T_j = -40°C ~ +125°C))

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DOS}		$V_I = V_{DD}$ or GND			3340	µA
I_{OZ}	Off state output current	$V_O = V_{DD}$ or GND		-	± 10	µA
I_{OS}	Output short current	V_O = 0V		-	-250	mA
I_L	Input leakage current	$V_O = V_{DD}$ or GND		-	± 1.0	µA
I_L	Input leakage current	V_I = GND (Pull-up 20kΩ)	-67	-165	-360	µA
I_L	Input leakage current	$V_I = V_{DD}$ (Pull-down 20kΩ)	67	165	360	µA
R_{PU}	Pull up resistance (20kΩ) (Note1)	V_I = GND	10	20	45	kΩ
R_{PD}	Pull down resistance (20kΩ) (Note1)	$V_I = V_{DD}$	10	20	45	kΩ
I_{OL}	Output Low current	V_{OL} = 0.4V (I_{OL} = 6.0 mA Type)	6.0	-	-	mA
I_{OL}	Output Low current	V_{OL} = 0.4V (I_{OL} = 8.0 mA Type)	8.0			mA
I_{OL}	Output Low current	V_{OL} = 0.4V (I_{OL} = 12.0 mA Type)	12.0			mA
I_{OH}	Output High current	V_{OH} = 2.4V (I_{OL} = 6.0 mA Type)	-6.0			mA
I_{OH}	Output High current	V_{OH} = 2.4V (I_{OL} = 8.0 mA Type)	-8.0			mA
I_{OH}	Output High current	V_{OH} = 2.4V (I_{OL} = 12.0 mA Type)	-12.0			mA
V_{OL}	Low level input voltage	I_{OL} = 0 mA			0.1	V
V_{OH}	High level input voltage	I_{OL} = 0 mA	V_{DD} -0.1			V

Note: 1. Impedance of pull-up and pull-down depend on input voltage and output voltage.

4. I/O buffer

Block Type	I/O	Description
P5INPHU	I(Input)	5V tolerant input buffer (Schmitt in) with Pull-up resistance 20kΩ
P5INPMN	I(Input)	5V tolerant input buffer
P5INPHD	I(Input)	5V tolerant input buffer (Schmitt in) with Pull-down resistance 20kΩ
P3OUTRB	O(Output)	Output buffer (low noise: I_{OL} = 8mA)
P3OUTRD	O(Output)	Output buffer (I_{OL} = 12mA)

Input Timing Specification

Symbol	Item	Specification			Unit
		Min	Typ	Max	
f(DCLK1)	Input Clock frequency	30	32.5	54/80	MHz
tw(DCLK1)	Input Clock period	12.5	30.8	33.3	ns
twH(DCLK1)	Input Clock High time	0.3	-	-	CLK
twL(DCLK1)	Input Clock Low time	0.3	-	-	CLK
tst(DI)	Input Data Setup time	2.3	-	-	ns
thd(DI)	Input Data Hold time	7.3	-	-	ns
tst(DENA)	Input Data Enable signal Setup time	2.3	-	-	ns
thd(DENA)	Input Data Enable signal Hold time	7.3	-	-	ns
tst(HD)	Horizontal Sync signal Setup time	2.3	-	-	ns
thd(HD)	Horizontal Sync signal Hold time	7.3	-	-	ns
tst(VD)	Vertical Sync signal Setup time	2.3	-	-	ns
thd(VD)	Vertical Sync signal Hold time	7.3	-	-	ns
tw(DENA)	Input Data Enable signal High time	512	512	640	CLK
tbh(DENAH)	Input Data Enable Horizontal Sync signal Blanking time	6	-	-	CLK
f(HD)	Horizontal Sync signal	-	48.25	62.5	KHz
tw(HD)	HD horizontal sync signal Low time	1	-	-	CLK
tf(HD)	Horizontal front porch	0	-	-	CLK
tb(HD)	Horizontal back porch	6	-	-	CLK
tbh(DENAV)	Input Data Enable Horizontal Sync signal Blanking time	4	-	-	H
f(VD)	Vertical sync signal	55	60	75	Hz
tw(VD)	VD Vertical Sync signal Low time	1	-	-	H
tf(VD)	Vertical front porch	0	-	-	H
tb(VD)	Vertical back porch	4	-	-	H

Note: HIGH, LOW level of input signal: V_{IL} = 0.8V, V_{IH} = 2.2V.

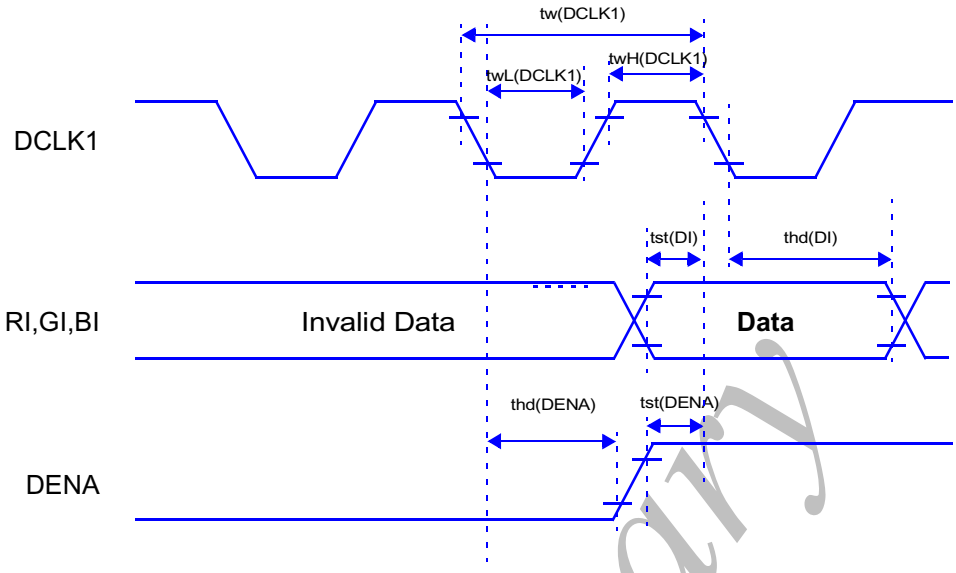


Figure-2

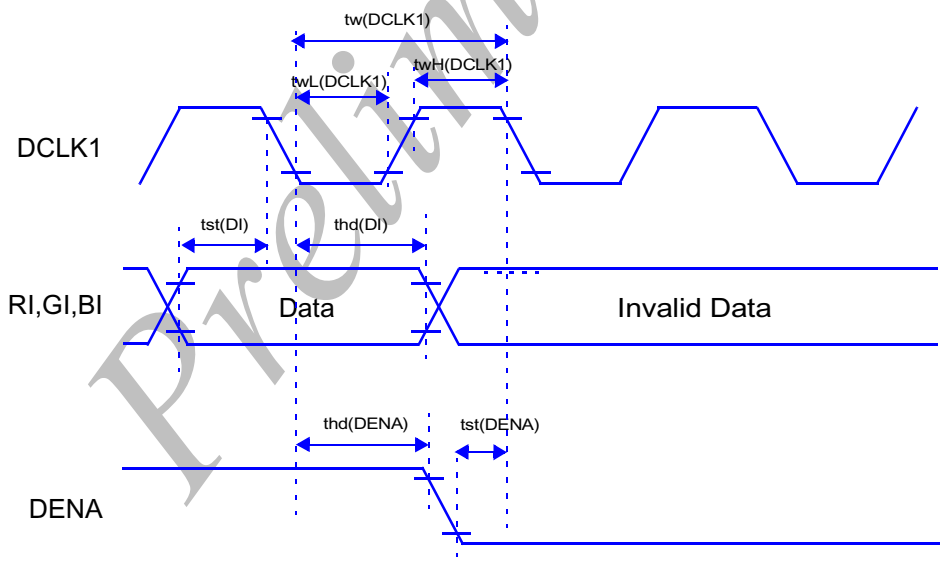


Figure-3

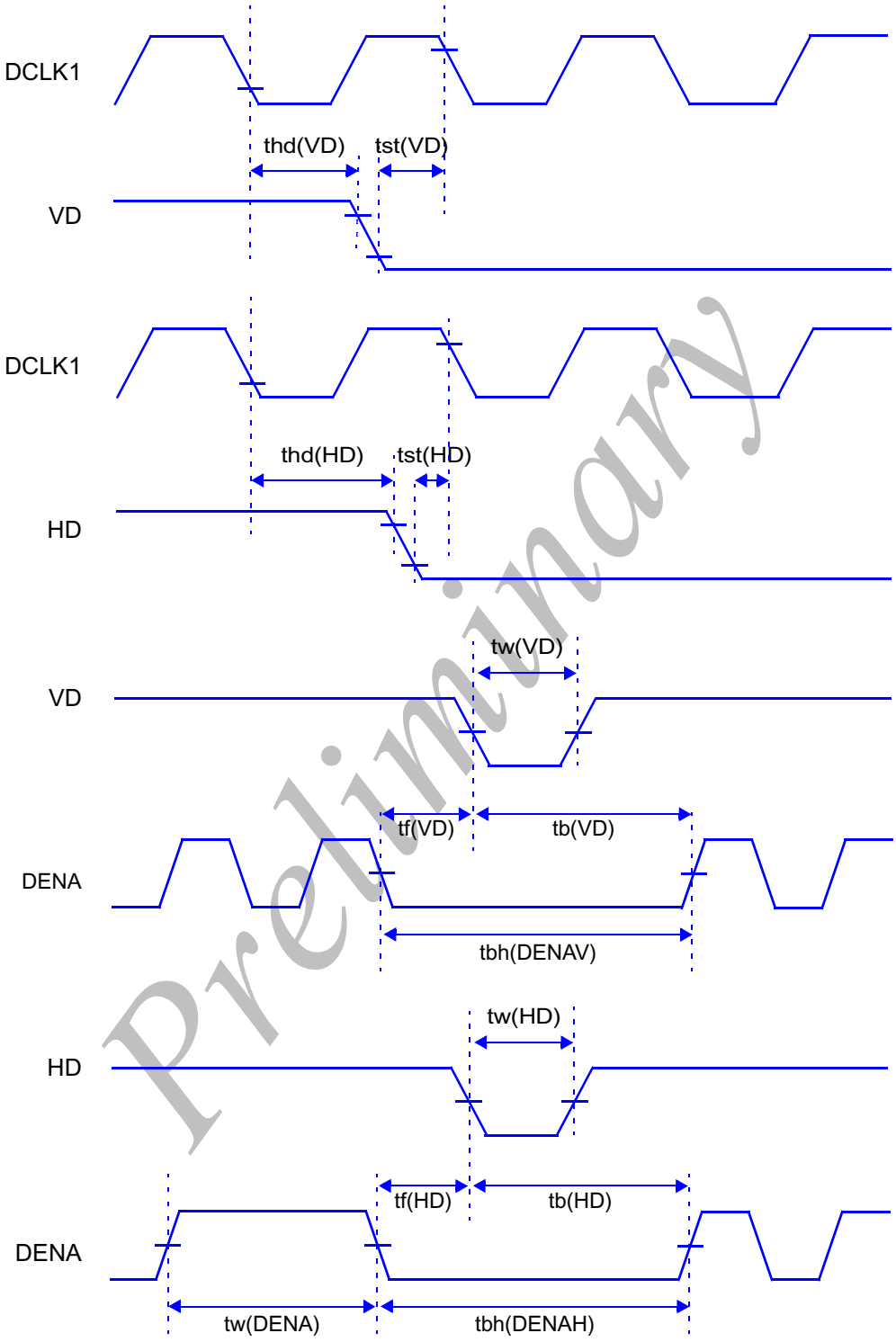


Figure-4

Horizontal Output Specification 1-1

ICMD1 = LOW --(NEC μPD16750, Hitachi HD66350T) PNDCLK, PNHVD = OPEN, ICMD2 = OPEN

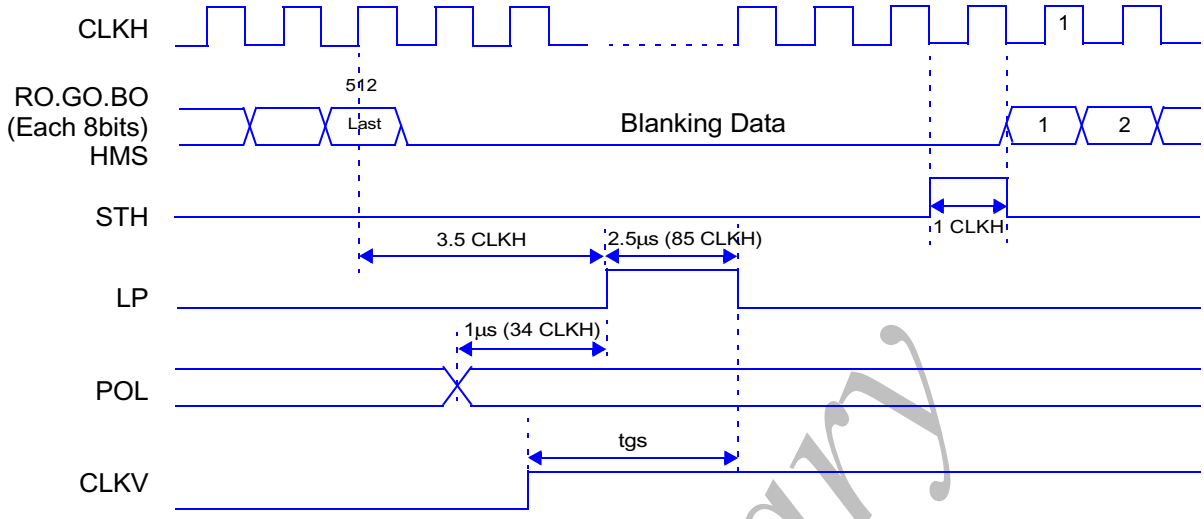


Figure-5

tgs: 2.5 ~ 4μs (0.5μs pitch)

POL: PLMD = L, revert once per HD
PLMD = H, revert once per 2HD
Revert once per VD

Horizontal Output Specification 1-2

ICMD1 = OPEN--(Toshiba T6L64C, Sharp LH168R) PNDCLK, PNHVD = OPEN, ICMD2 = OPEN

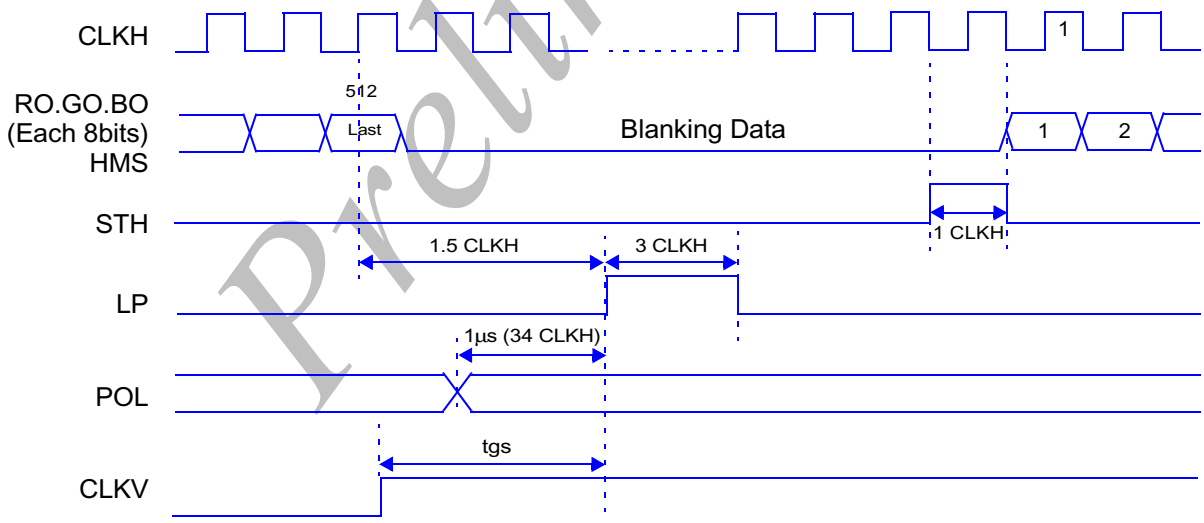


Figure-6

tgs: 2.5 ~ 4μs (0.5μs pitch)

POL: PLMD = L, revert once per HD
PLMD = H, revert once per 2HD
Revert once per VD

Horizontal Output 1-3

ICMD1 = LOW--**(Winbond WFP6815)** PNDCLK, PNHVD = OPEN, ICMD2 = LOW

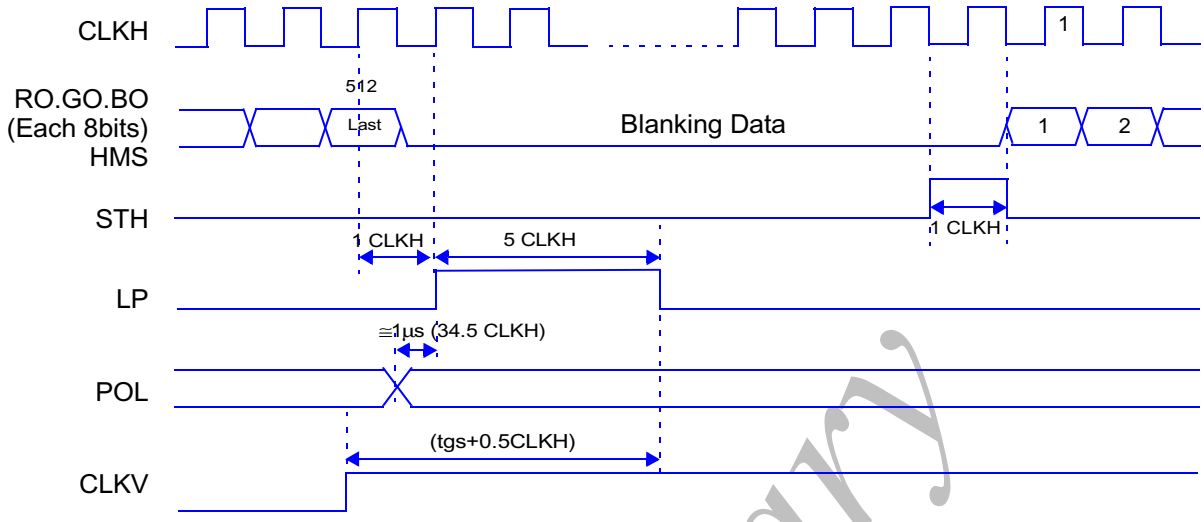


Figure-7

tgs: 2.5 ~ 4μs (0.5μs pitch)

POL: PLMD = L, revert once per HD
PLMD = H, revert once per 2HD
Revert once per VD

Horizontal Output 1-4

ICMD1 = OPEN--(**TI TMS57571B**) PNDCLK, PNHVD = OPEN, ICMD2 = LOW

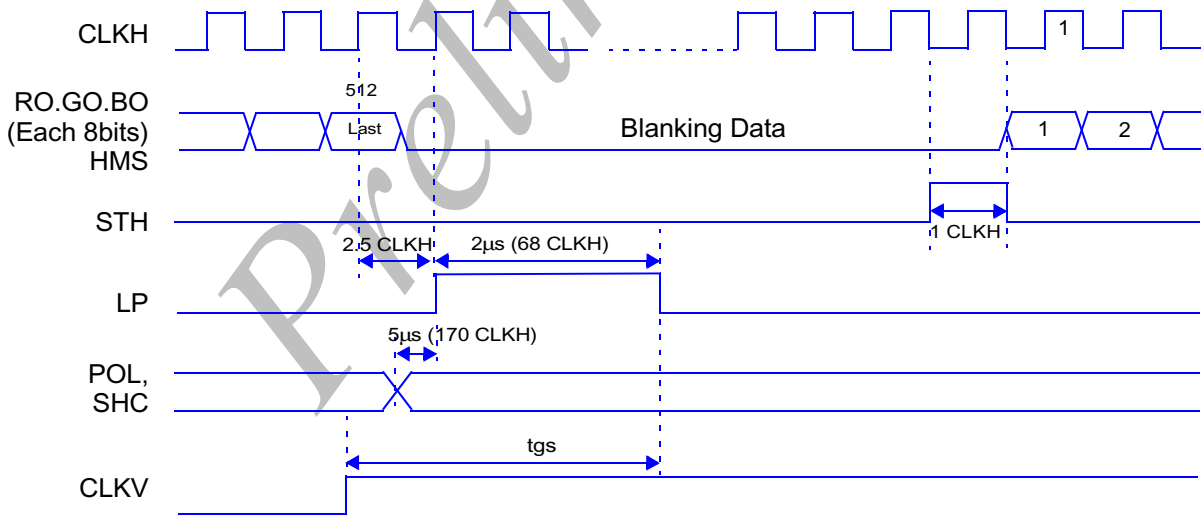


Figure-8

tgs: 2.5 ~ 4μs (0.5μs pitch)

POL: PLMD = L, revert once per HD
PLMD = H, revert once per 2HD
Revert once per VD
SHC: Revert once per HD only

Horizontal Output 2-1 (Data output specification)

ICMD1 = LOW--**(NEC μPD16750, Hitachi HD66350T)**, ICMD2 = OPEN

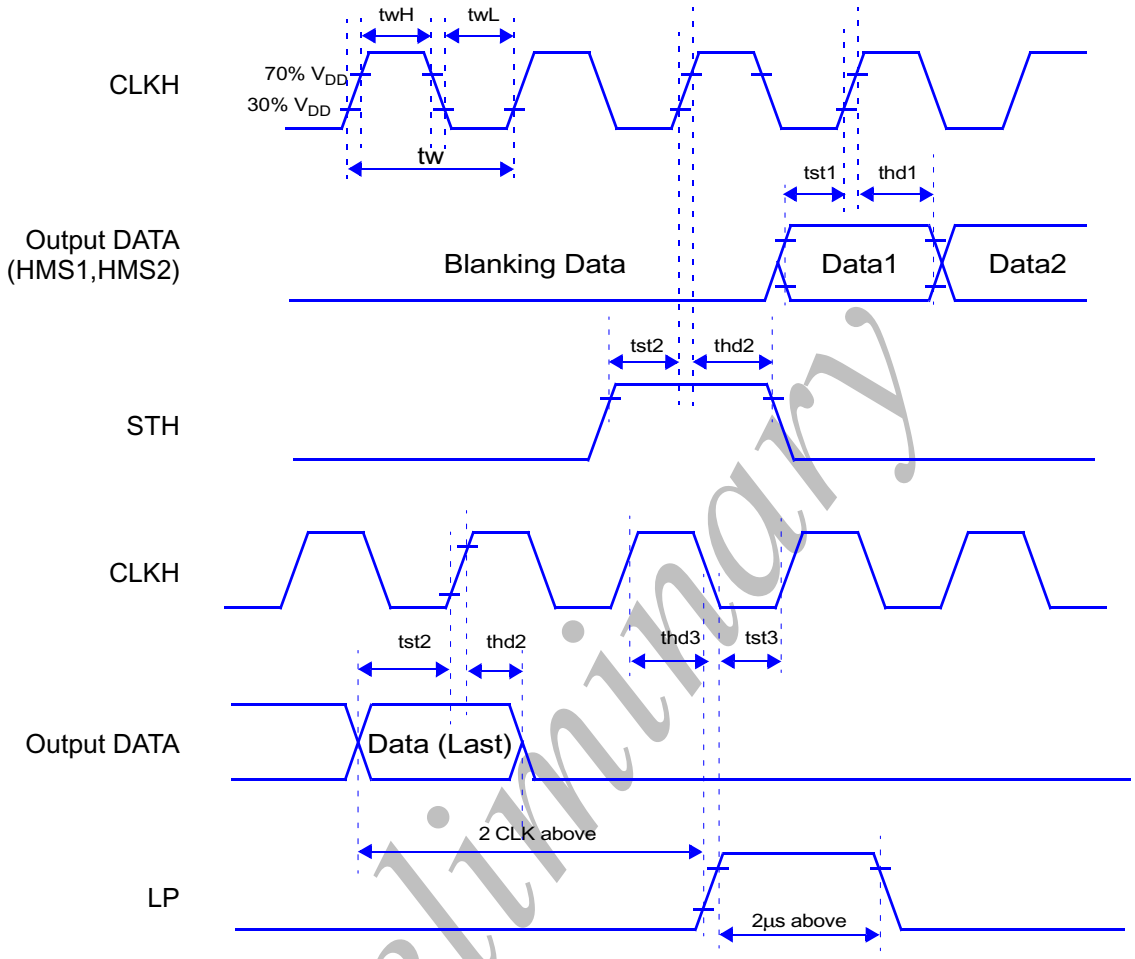


Figure-9

Symbol	Item	Specification			Unit
		Min	Typ	Max	
tw	CLK pulse width	14			ns
twH	CLK high pulse width	3			ns
twL	CLK low pulse width	3			ns
tst1	DATA setup time	1			ns
thd1	DATA hold time	2			ns
tst2	STH setup time	1			ns
thd2	STH hold time	2			ns
tst3	CLK-LP time	6			ns
thd3	LP-CLK time	6			

Horizontal Output 2-2 (Data output specification)

ICMD1 = OPEN--**(Toshiba T6L64C, Sharp LH168R)** ,ICMD2 = OPEN

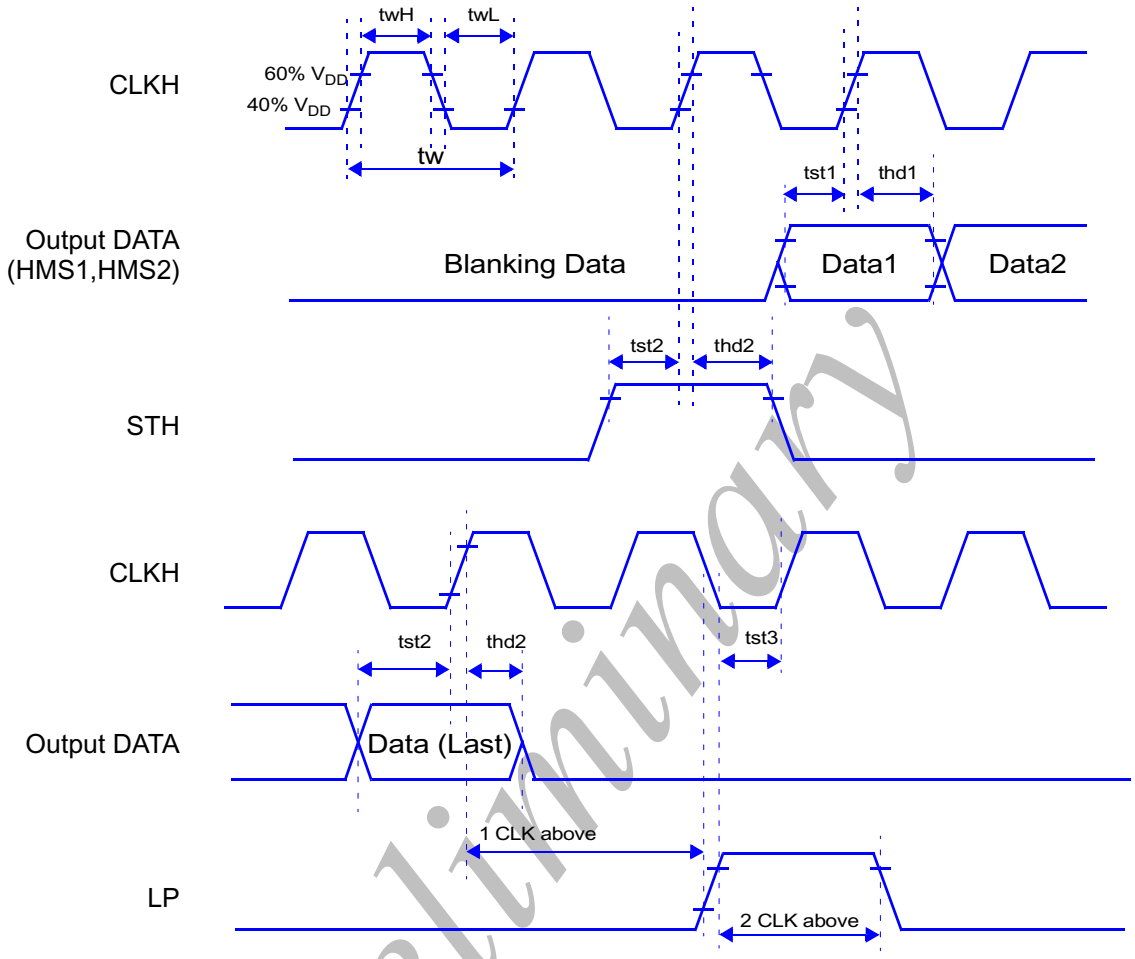


Figure-10

Symbol	Item	Specification			Unit
		Min	Typ	Max	
twH	CLK high pulse width	4			ns
twL	CLK low pulse width	4			ns
tst1	DATA setup time	4			ns
thd1	DATA hold time	0			ns
tst2	STH setup time	4			ns
thd2	STH hold time	0			ns
tst3	CLK-LP time	4			ns

Horizontal Output 2-3 (Data output specification)

ICMD1 = LOW--**(Winbond WFP6815)**, ICMD2 = LOW

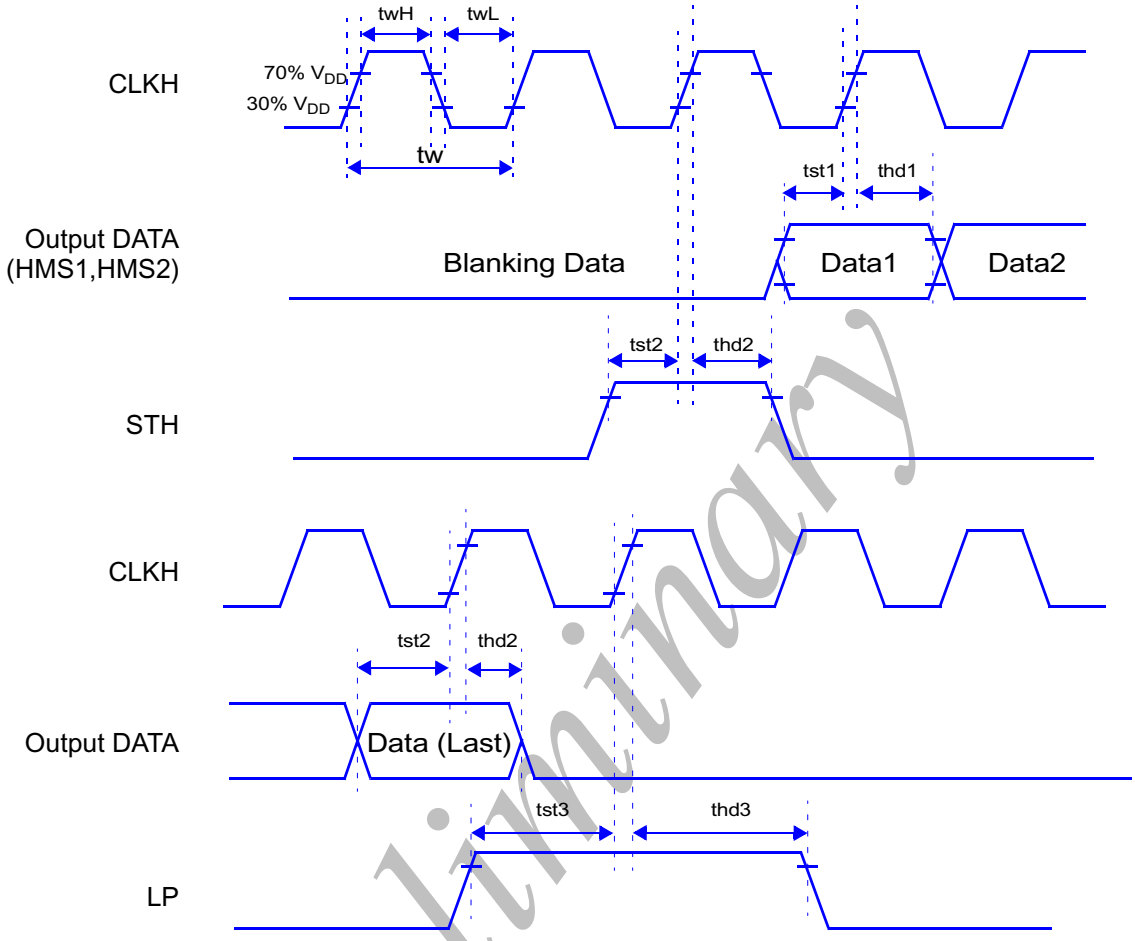


Figure-11

Symbol	Item	Specification			Unit
		Min	Typ	Max	
twH	CLK high pulse width	6			ns
twL	CLK low pulse width	6			ns
tst1	DATA setup time	3			ns
thd1	DATA hold time	0			ns
tst2	STH setup time	3			ns
thd2	STH hold time	0			ns
tst3	LP setup time	10			ns
thd3	LP hold time	2			tclk

Horizontal Output 2-4 (Data output specification)

ICMD1 = OPEN--**(TI TMS 57571B)**, ICMD2 = LOW

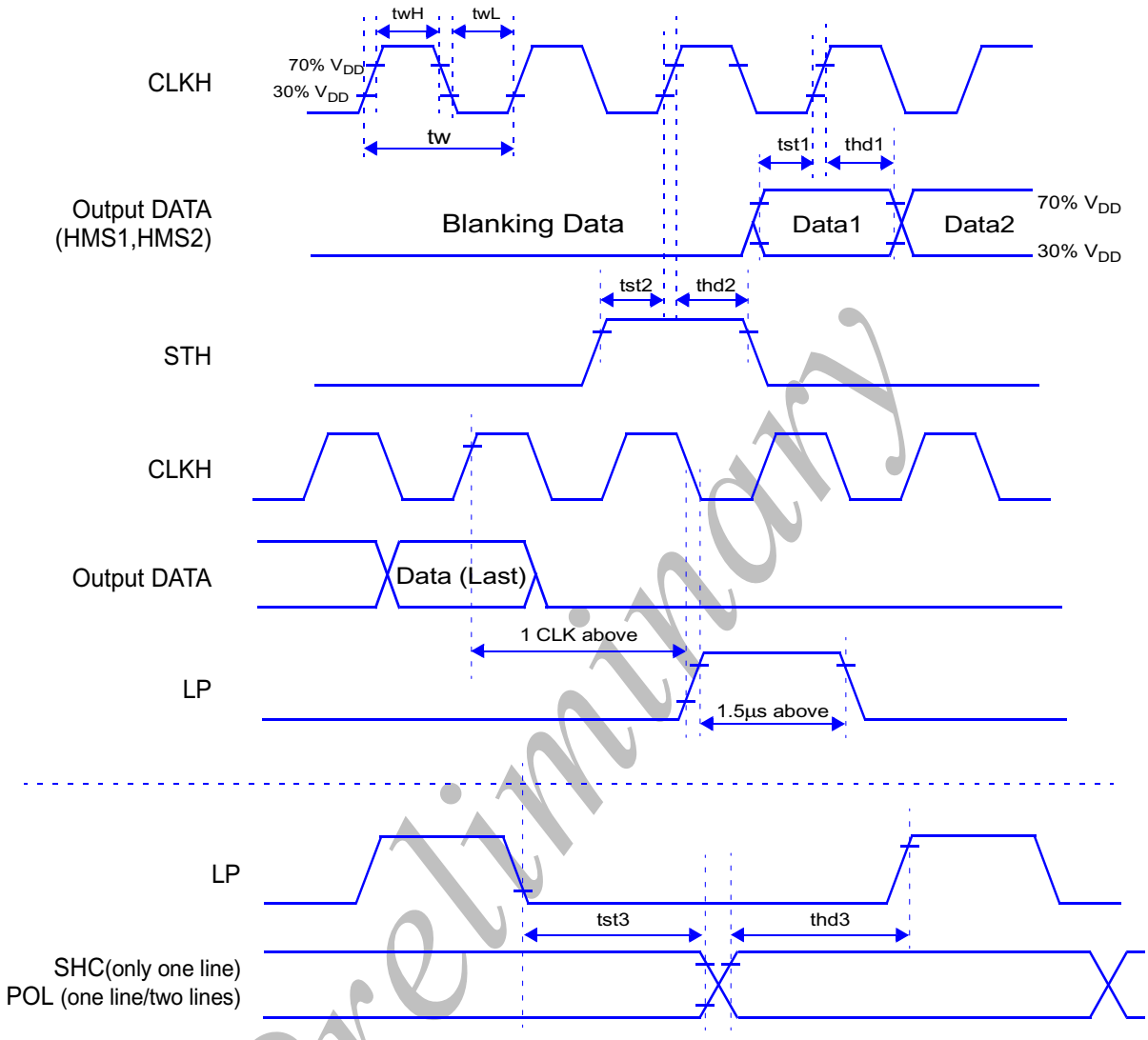


Figure-12

Symbol	Item	Specification			Unit
		Min	Typ	Max	
tw	CLK pulse width	18			ns
twH	CLK High pulse width	4			ns
twL	CLK Low pulse width	4			ns
tst1	DATA setup time	4			ns
thd1	DATA hold time	0			ns
tst2	STH setup time	4			ns
thd2	STH hold time	0			ns
tst3	CLK-LP time	4.5			µs
thd3	SHC hold time	4.5			µs

Vertical Output 3-1 (Data output specification)

(NEC μPD16750, Hitachi HD66350T, Toshibi T6L34C, Sharp LH168R, Winbond WFP6815)

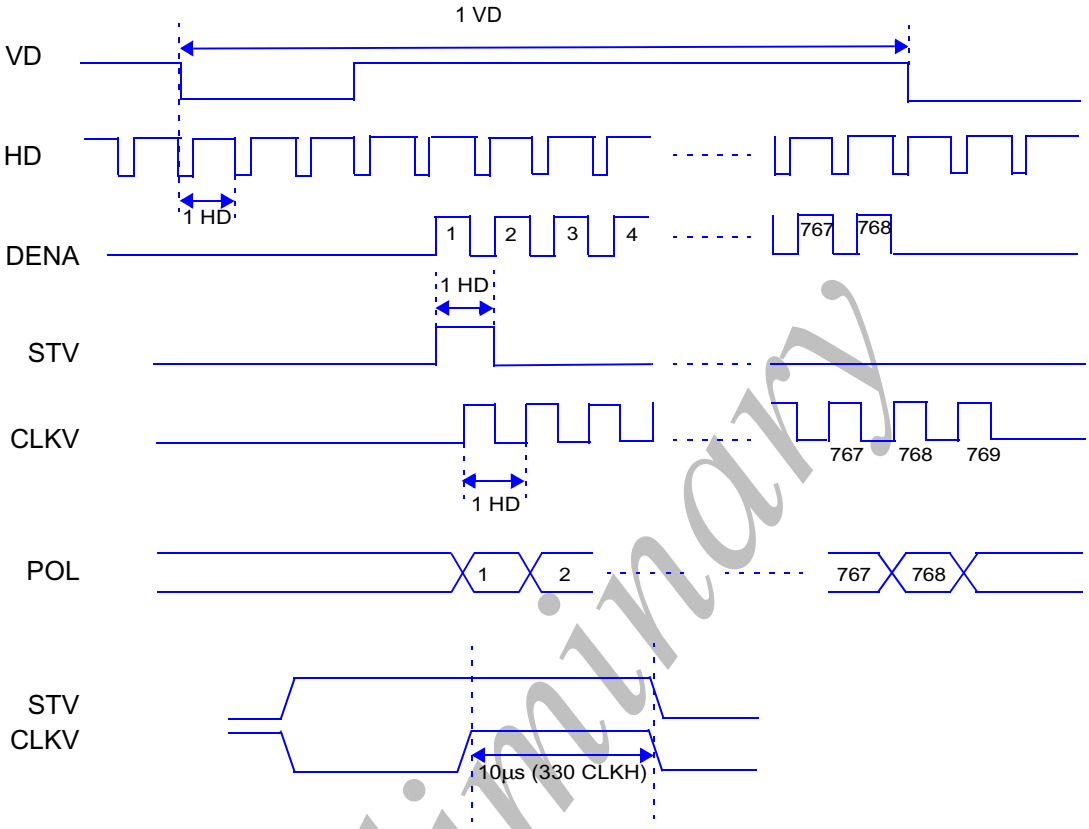


Figure-13

Vertical Output 3-2 (Data output specification)

(T.I. TMS57571)

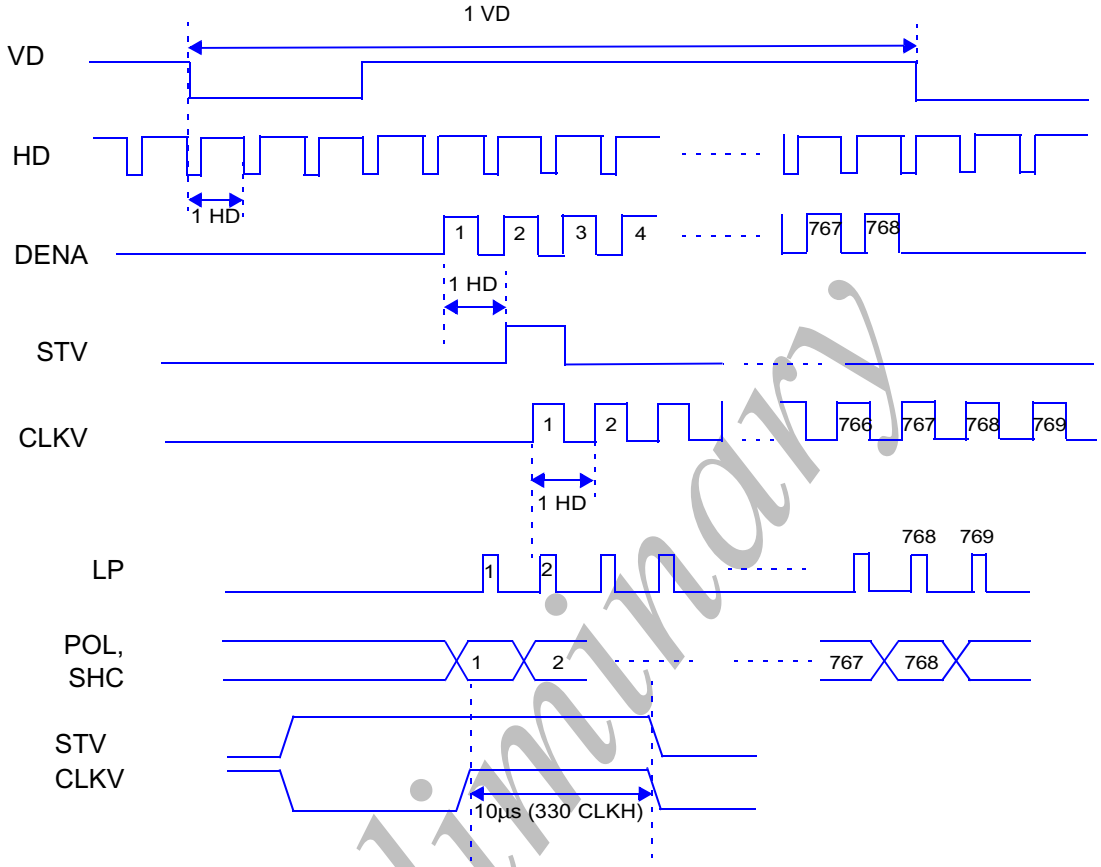


Figure-14

CLKV, STV Timing Specification

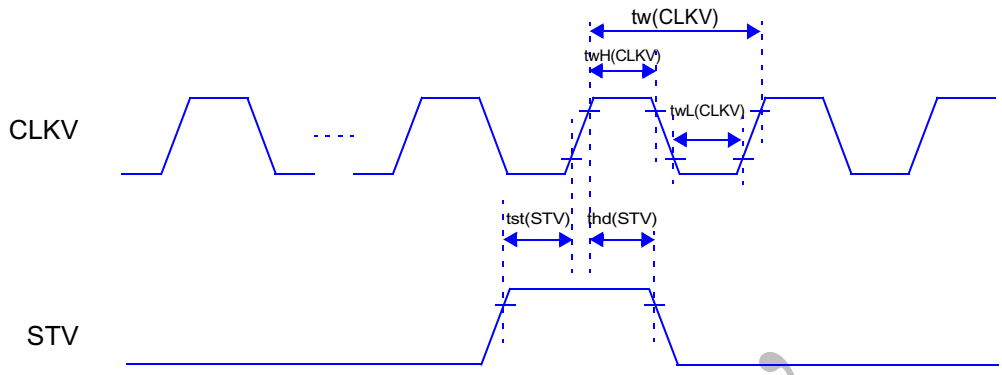


Figure-15

Symbol	Item	Specification			Unit
		Min	Typ	Max	
tst(STV)	STV set-up time	1			µs
thd(STV)	STV hold time	1			µs
tw(CLKV)	CLKV period	8			µs
twH(CLKV)	CLKV High width	3.5			µs
twL(CLKV)	CLKV Low width	3.5			µs

Data Polarity

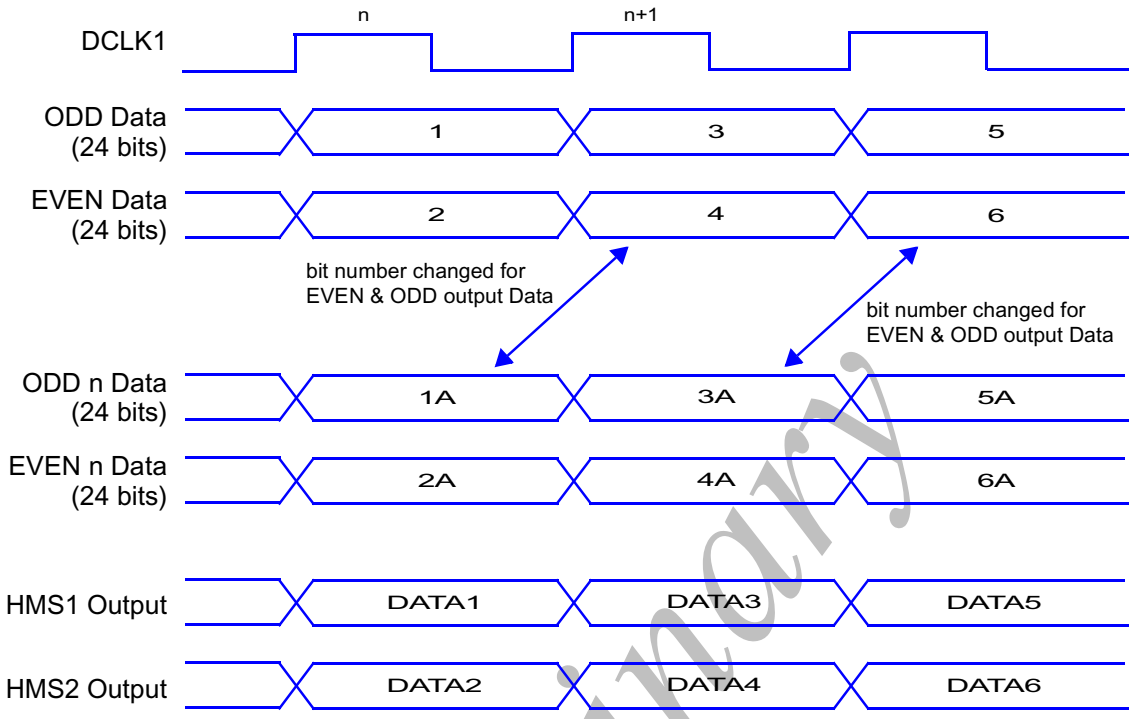


Figure-16

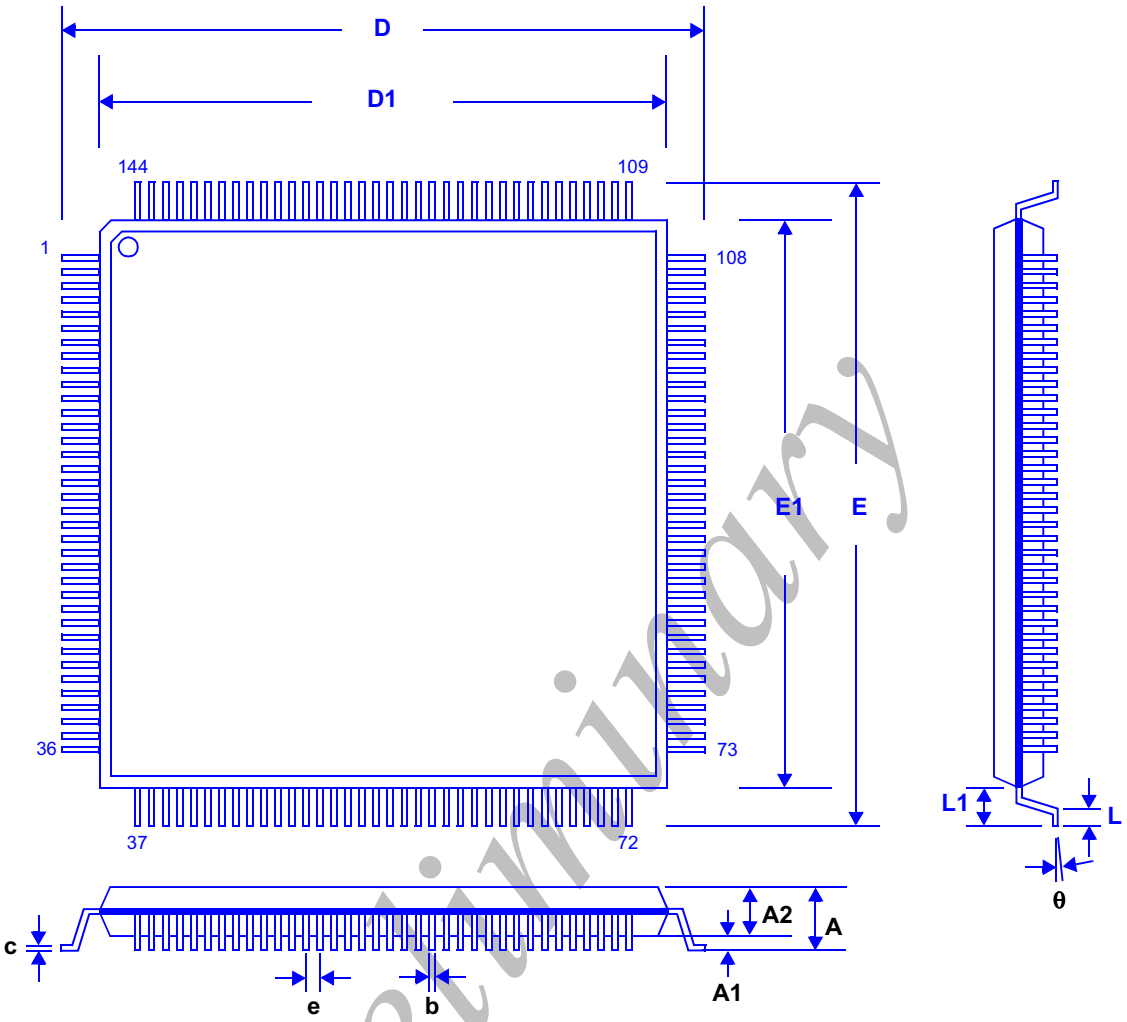
Above Polarity diagram indicates the relationship between HMS and ODD/EVEN DATA output is related to PIN "POLIN".

1. POLIN = LOW; Polarity function is disable.
HMS1, 2 output are INV; RGB data output is the same as RGB input data.

2. POLIN = OPEN; Polarity function is enable.

- ASIC will compare ODD DATA (1A) of number "n" with ODD DATA (3) of number "n+1":
- As the number of bits changed exceeds 13, HMS1 (DATA3) output HIGH and ODD DATA (3A) outputs are inversion of ODD DATA(3).
- As the number of bits changed is below 13, HMS1 (DATA3) output LOW and ODD DATA (3A) outputs are ODD DATA (3).
- ASIC will compare EVEN DATA (2A) of number "n" with EVEN DATA (4) of number "n+1":
- As the number of bits changed exceeds 13,HMS2 (DATA4) output HIGH and EVEN DATA (4A) outputs are inversion of EVEN DATA(4).
- As the number of bits changed is below 13, HMS2 (DATA4) output LOW and EVEN DATA (4A) outputs are EVEN DATA (4).

PACKAGE OUTLINE (144-pin LQFP)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	-	0.002	-	-
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.12	-	0.20	0.005	-	0.008
D	21.85	22.00	22.15	0.860	0.866	0.872
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	21.85	22.00	22.15	0.860	0.866	0.872
E1	19.90	20.00	20.10	0.783	0.787	0.791
e	-	0.50	-	-	0.020	-
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	-	1.00	-	-	0.039	-
θ	0°	3.5°	7°	0°	3.5°	7°

APPLICATION CIRCUIT SCHEMATIC

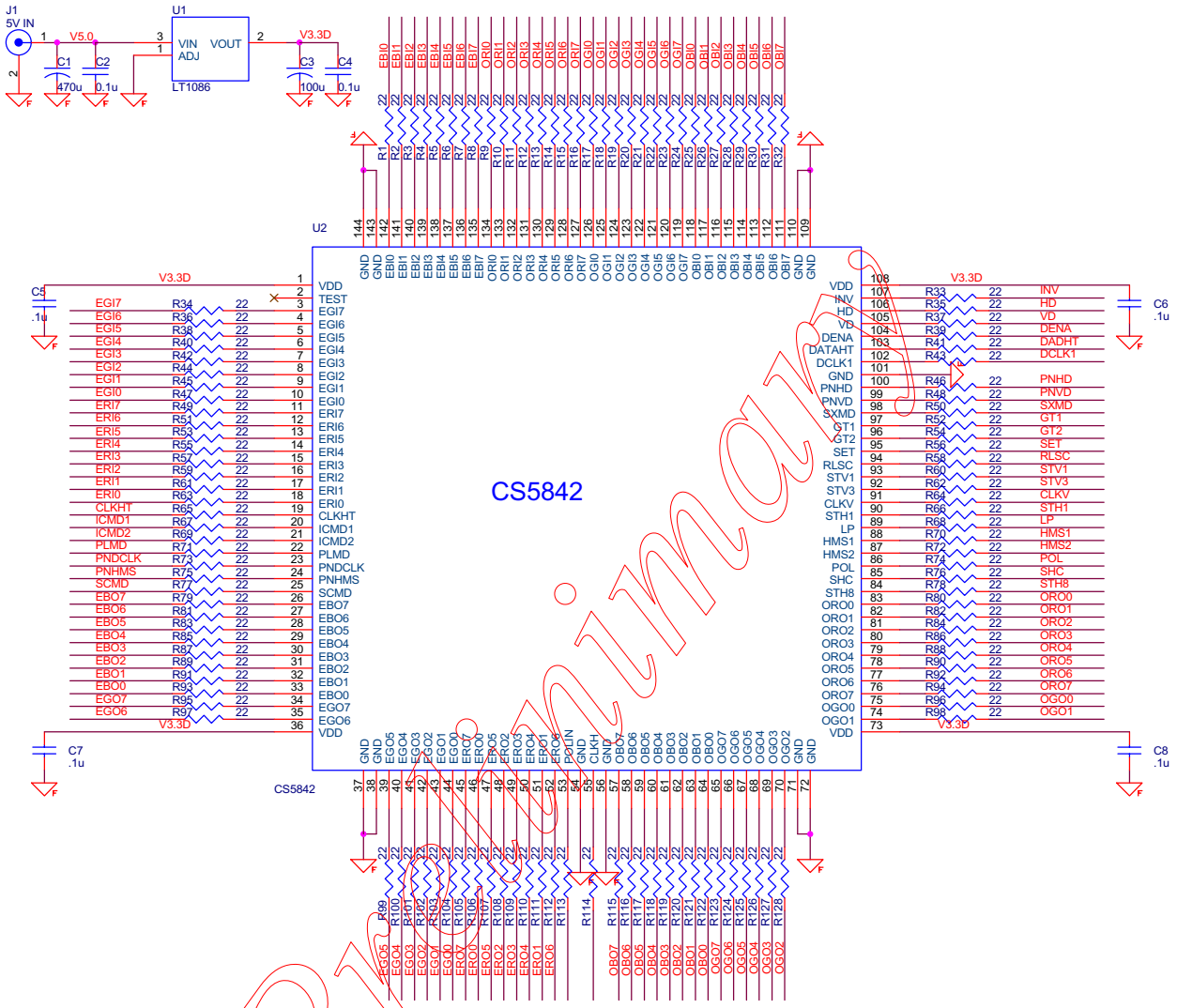


Figure-17 Using 144-pin LQFP