Genesys Logic, Inc.

GL860A

USB 2.0 UVC Camera Controller

Datasheet
Revision 1.00
May 09, 2007

Copyright:

Disclaimer:

ALL MATERIALS ARE PROVIDED "AS IS" WITHOUT EXPRESS OR IMPLIED WARRANTY OF ANY KIND. NO LICENSE OR RIGHT IS GRANTED UNDER ANY PATENT OR TRADEMARK OF GENESYS LOGIC INC.. GENESYS LOGIC HEREBY DISCLAIMS ALL WARRANTIES AND CONDITIONS IN REGARD TO MATERIALS, INCLUDING ALL WARRANTIES, IMPLIED OR EXPRESS, OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF INTELLECTUAL PROPERTY. IN NO EVENT SHALL GENESYS LOGIC BE LIABLE FOR ANY DAMAGES INCLUDING, WITHOUT LIMITATION, DAMAGES RESULTING FROM LOSS OF INFORMATION OR PROFITS. PLEASE BE ADVISED THAT THE MATERIALS MAY CONTAIN ERRORS OR OMMISIONS. GENESYS LOGIC MAY MAKE CHANGES TO THE MATERIALS OR TO THE PRODUCTS DESCRIBED THEREIN AT ANY TIME WITHOUT NOTICE.

Trademarks:

GENESYS LOGIC is a registered trademark of Genesys Logic, Inc.
All trademarks are the properties of their respective owners.

Office:

Genesys Logic, Inc.
12F, No. 205, Sec. 3, Beishin Rd., Shindian City,
Taipei, Taiwan
Tel: (886-2) 8913-1888
Fax: (886-2) 6629-6168

http://www.genesyslogic.com

Revision History

Revision	Date	Description
0.9	21/12/2006	First draft release
0.91	01/03/2007	Update register
1.00	09/05/2007	Add 46pin package information

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL DESCRIPTION

The GL860A is a high performance USB 2.0 Video class compliant controller for PC Camera and NB camera application. With the Genesys Logic's highly recognized self-developed USB high-speed transceiver, GL860A provides up to 30 fps at VGA or capture still images at 2 Mega pixels for fulfilling the mass bandwidth demand of video transferring. GL860A also support USB isochronous mode to provide certain bandwidth to insure user can get satisfied usage experience on video application even running high bandwidth consumption devices concurrently.

The GL860A, compliant with Video Class 1.1 in USB Device Class (UVC), can be worked with Microsoft native driver. It makes you use USB PC Camera as you use an USB flash disk. Additionally, the GL860A provides an alternative proprietary driver to meet better image performance requirement.

The GL860A integrates a highly flexible sensor interface to make it easily adopted with variety sensors in which include most popular CCD sensor module and CMOS sensors. The GL860A's low power consumption, low operation temperature characteristic also make it easy to implement a high quality PC Camera without worry about the noise signals of sensors to affect by high performance USB controller.

CHAPTER 2 FEATURES

- USB specification compliance
  - Complies with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Complies with 12Mbps Universal Serial Bus specification rev. 2.0.
  - Support USB 2.0 Isochronous Video pipe to 24MB/s.
- Sensor interface
  - Programmable interface for popular general CCD module/CMOS sensor
- Non-process video streaming (USB High-speed connection)
- Support 4 USB endpoints
  - Endpoint 0: Control PIPE.
  - Endpoint 1: Isochronous/Bulk data in (configurable).
  - Endpoint 2: Interrupt OUT.
  - Endpoint 3: Interrupt IN.
- Embedded 8052 micro-controller
  - Operate @ 15 MHz clock.
  - 8K ROM.
- Support USB remote wakeup..
- 3.3V/1.8V operation.
- 3.3V to 1.8V regulator is built-in.
- Capability to support on-line download program
- Available in 100-pin QFP and 48-pin LQFP package.
- Pass WHQL (Windows Hardware Quality Lab)
- Pass USB-IF (USB Implementers Forum) test
- Application — NB Cam, PC Cam, UMPC, Game Console
- Support OS — XP, Vista, MCE, XP64, Win2K
- USB Video Class V1.1 compliant
  - The sensor, UVC, property control setting stored in external EEPROM (24Cxxx). (<= 8K bytes)
  - Support alternative proprietary driver to enhance image performance.
  - Non-UVC mode (Non-EEPROM), worked with proprietary driver

    Support YUV/RGB/I420 format

    Video stream up to：12 fps in UXGA, 15 fps in SXGA, 30 fps in VGA
  - UVC Class mode (External EEPROM), worked with OS native driver

    Support UVC uncompressed YUY2 format

    Video stream up to：6 fps in UXGA, 9 fps in SXGA, 30 fps in VGA
  - Still image captured up to UXGA

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

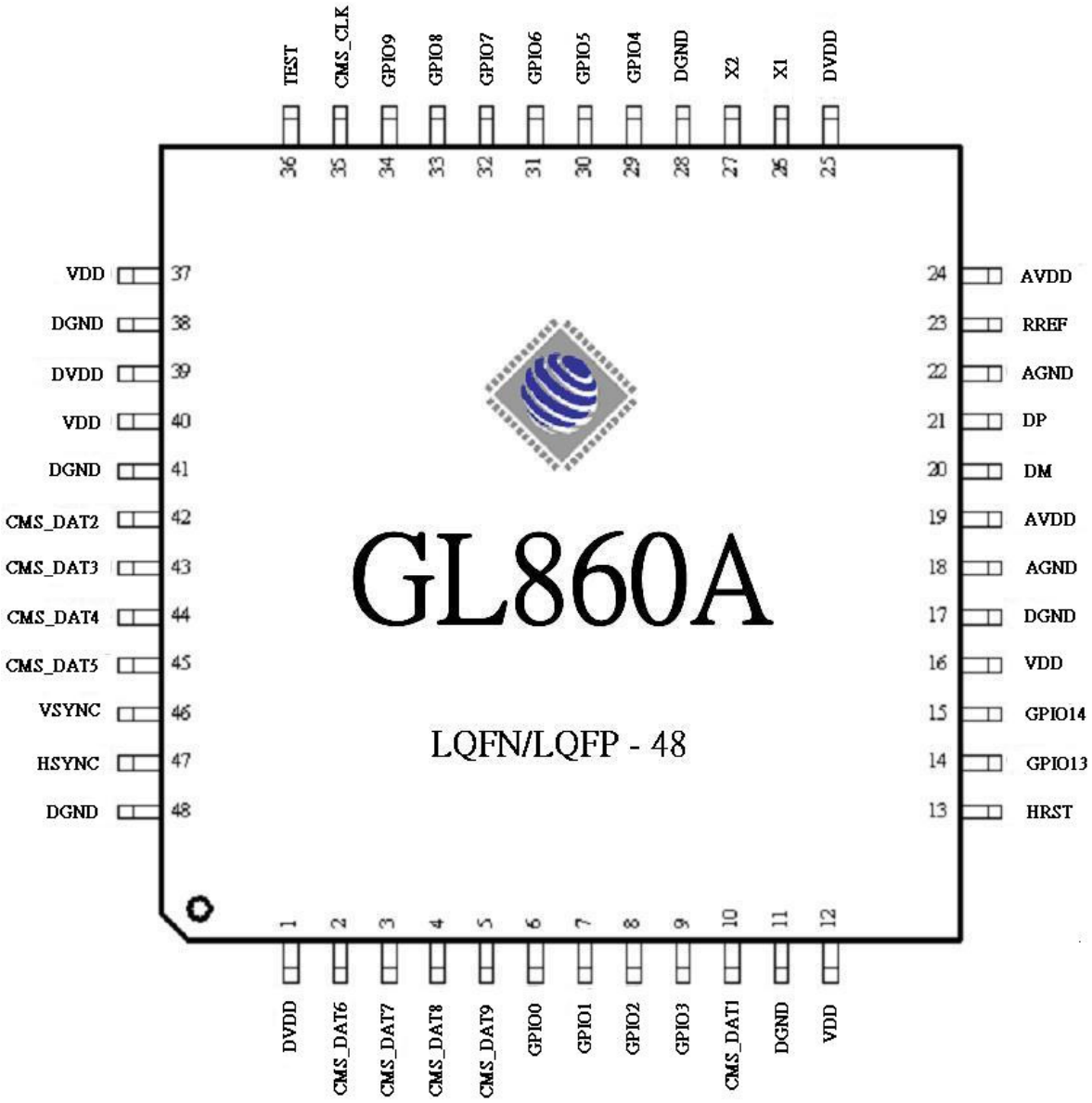


Figure 3.1 - 48 Pin LQFN/LQFP Pinout Diagram

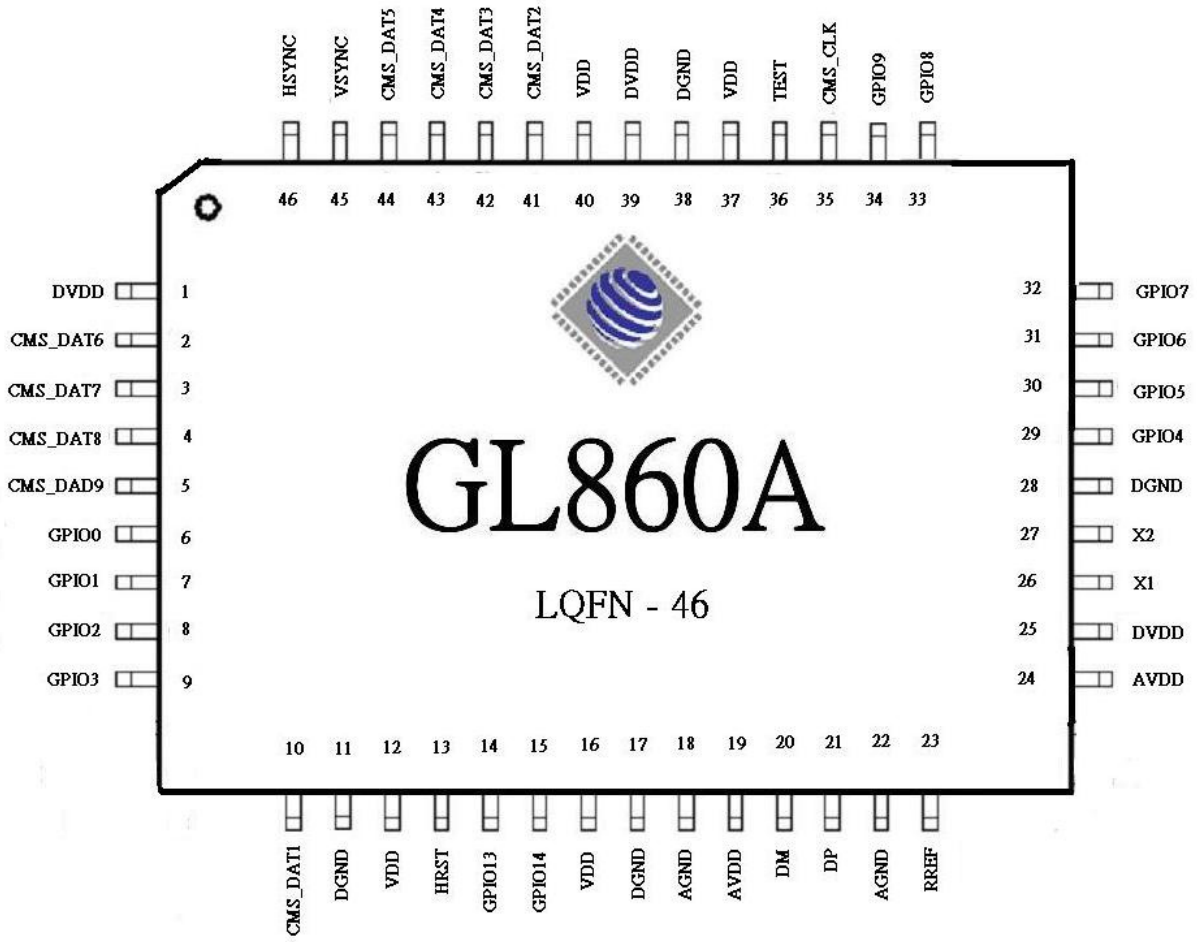


Figure 3.2 - 46 Pin LQFN Pinout Diagram

3.2 Pin List

Three type packages:

Case 1
- 48 pin
- 8 bit sensor interface
- 12 GPIO pins
- LQFP/LQFN package

Case 2
- 46 pin
- 8 bit sensor interface
- 12 GPIO pins
- LQFN package

Table 3.1 - 48-Pin LQFP/LQFN Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DVDD	P	13	HRST_	I	25	DVDD	P	37	VDD	P
2	CMS_DAT6	I	14	GPIO13	I/O	26	X1	I	38	DGND	P
3	CMS_DAT7	I	15	GPIO14	I/O	27	X2	I/O	39	DVDD	P
4	CMS_DAT8	I	16	VDD	P	28	DGND	P	40	VDD	P
5	CMS_DAT9	I	17	DGND	P	29	GPIO4	I/O	41	DGND	P
6	GPIO0	I/O	18	AGND	P	30	GPIO5	I/O	42	CMS_DAT2	I
7	GPIO1	I/O	19	AVDD	P	31	GPIO6	I/O	43	CMS_DAT3	I
8	GPIO2	I/O	20	DM	I/O	32	GPIO7	I/O	44	CMS_DAT4	I
9	GPIO3	I/O	21	DP	I/O	33	GPIO8	I/O	45	CMS_DAT5	I
10	CMS_DAT1	I/O	22	AGND	P	34	GPIO9	I/O	46	VSYNC	I/O
11	DGND	P	23	RREF	A	35	CMS_CLK	I/O	47	HSYNC	I/O
12	VDD	P	24	AVDD	P	36	TEST	I	48	DGND	P

Table 3.2 - 46-Pin LQFN Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DVDD	P	13	HRST_	I	25	DVDD	P	37	VDD	P
2	CMS_DAT6	I	14	GPIO13	I/O	26	X1	I	38	DGND	P
3	CMS_DAT7	I	15	GPIO14	I/O	27	X2	I/O	39	DVDD	P
4	CMS_DAT8	I	16	VDD	P	28	DGND	P	40	VDD	P
5	CMS_DAT9	I	17	DGND	P	29	GPIO4	I/O	41	CMS_DAT2	I
6	GPIO0	I/O	18	AGND	P	30	GPIO5	I/O	42	CMS_DAT3	I
7	GPIO1	I/O	19	AVDD	P	31	GPIO6	I/O	43	CMS_DAT4	I
8	GPIO2	I/O	20	DM	I/O	32	GPIO7	I/O	44	CMS_DAT5	I
9	GPIO3	I/O	21	DP	I/O	33	GPIO8	I/O	45	VSYNC	I/O
10	CMS_DAT1	I/O	22	AGND	P	34	GPIO9	I/O	46	HSYNC	I/O
11	DGND	P	23	RREF	A	35	CMS_CLK	I/O			
12	VDD	P	24	AVDD	P	36	TEST	I			

3.3 Pin Descriptions

Table 3.3 - 48-Pin LQFP/LQFN Pin Descriptions

Pin Name	Pin#	Type	Description
VDD	12,16,37,40	P	1.8V power for crystal
CMS_DAT1~9	10,42~45,2~5	I	Sensor data bit 1~9
GPIO0~9,13,14	6~9,29~34, 14,15	I/O (pd)	GPIO pins bit 0~9,13,14
GND	11,17,18,22 28,38,41,48	P	Ground
DVDD	1,25,39	P	3.3V core power
HRST	13	I (pu)	Hardware reset, low active
AVDD	19,24	P	3.3V analog power
DM	20	I/O	USB D-
DP	21	I/O	USB D±
RREF	23	A	Reference R
X1	26	I	12M crystal in
X2	27	I/O	12M crystal out
CMS_CLK	35	I/O	Sensor clock
TEST	36	I (pd)	Test mode
VSYNC	46	I/O	Sensor Vsync

HSYNC	47	I/O	Sensor Hsync
NC	10	-	No connection

Table 3.4 - 46-Pin LQFN Pin Descriptions

Pin Name	Pin#	Type	Description
VDD	12,16,37,40	P	1.8V power for crystal
CMS_DAT1~9	10,41~44,2~5	I	Sensor data bit 1~9
GPIO0~9,13,14	6~9,29~34, 14,15	I/O (pd)	GPIO pins bit 0~9,13,14
GND	11,17,18,22, 28,38	P	Ground
DVDD	1,25,39	P	3.3V core power
HRST	13	I (pu)	Hardware reset, low active
AVDD33	19,24	P	3.3V analog power
DM	20	I/O	USB D-
DP	21	I/O	USB D+
RREF	23	A	Reference R
X1	26	I	12M crystal in
X2	27	I/O	12M crystal out
CMS_CLK	35	I/O	Sensor clock
TEST	36	I (pd)	Test mode
VSYNC	45	I/O	Sensor Vsync
HSYNC	46	I/O	Sensor Hsync
NC	10	-	No connection

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 REGISTERS

4.1 Registers Base Address

Table 4.1 - Base Address for Registers

Mnemonic	Offset	Description	Default
GP1_DAT	00h	GPIO[7:0] data	--
GP1_INTPOL	01h	Interrupt polarity for GPIO[7:0]	8'h00
GP1_INTEN	02h	Interrupt enable for GPIO[7:0]	8'hFF
GP1_INT	03h	Interrupt indication for GPIO[7:0]	8'h00
ROMFLG	04h	Reserved for internal use.	8'hFF
GP1_OE	06h	Output enable for GPIO[7:0]	8'h00
GP2_DAT	07h	GPIO[14:8] data	--
GP2_INTPOL	08h	Interrupt polarity for GPIO[14:8]	8'h00
GP2_INTEN	09h	Interrupt enable for GPIO[14:8]	8'hFF
GP2_INTEN	0Ah	Interrupt indication for GPIO[14:8]	8'h00
GP2_OE	0Dh	Output enable for GPIO[14:8]	8'h00
GCTL	0Eh	Global control register	8'hFC
INT_MASK	0Fh	Interrupt mask for each sub-module	8'h00
CLKCTL	10h	Sensor clock control	8'h80
CPURST	11h	CPU reset register	8'h00
DEVCTL	40h	USB Device control	8'h04
UEVT1	41h	USB interrupt flag #1	8'h00
UEVT2	42h	USB interrupt flag #2	8'h00
UEVT1EN	43h	USB interrupt #1 enable	8'h00
UEVT2EN	44h	USB interrupt #2 enable	8'h00
UTMCTL	45h	UTMI control	8'h0C
UTMDATL	46h	UTMI data low byte	--
UTMDATH	47h	UTMI data high byte	--
DEVADR	48h	USB device address	8'h00
MISC	49h	Miscellaneous register	8'h10
EPCTL1	4Ah	Endpoint control 1	8'h00
EPCTL2	4Bh	Endpoint control 2	8'h00
EPCTL3	4Ch	Endpoint control 3	8'h00
EP0CTL	4Dh	Endpoint 0 control	8'h40
RX0CNT	4Eh	Endpoint 0 receive length	8'h00
FF0BUF	4Fh	Endpoint 0 FIFO data	8'h00
FF1BUF	50h	Endpoint 1 FIFO data	8'h00

FF2BUF	51h	Endpoint 2 FIFO data	8'h00
FF3BUF	52h	Endpoint 3 FIFO data	8'h00
EP12CTL1	53h	Endpoint1,2 control 1	8'h00
EP12CTL2	54h	Endpoint1,2 control 2	8'h00
EP12CTL3	55h	Endpoint1,2 control 3	8'h00
EP3CTL	56h	Endpoint3 control	8'h00
RX2CNT	57h	Endpoint 2 receive length	8'h00
WAKEN	5Fh	Wakeup source enable	8'h00
HEADCTL1	60h	Head function control 1	8'h00
HEADCTL2	61h	Head function control 2	8'h00
HEAD0	62h	Head 0 data	8'h00
HEAD1	63h	Head 1 data	8'h00
SEN_CTL	C0h	Sensor control	8'h00
MCK_SAMP	C1h	Master clock selection / Select of sampling phase	8'h03
CLKRG_ CLKFG	C2h	Falling/rising edge for MCLK	8'h00
HV_CC	C3h	Clock counter for Hsync/Vsync output	8'h00
RHNL	C4h	Pixel number for rising edge of Hsync output	8'h00
RHNH_ FHNH	C5h	Pixel number for rising/falling of Hsync output	8'h00
FHNL	C6h	Pixel number for falling edge of Hsync output	8'h00
RVPNL	C7h	Pixel number for rising edge of Vsync output	8'h00
RVPNH_ RVLNH	C8h	Pixel number for rising/falling of Vsync output	8'h00
RVLNL	C9h	Pixel number for falling edge of Vsync output	8'h00
FVPNL	CAh	Line number for rising edge of Vsync output	8'h00
FVPNH_ FVLNH	CBh	Line number for rising/falling of Vsync output	8'h00
FVLNL	CCh	Line number for falling edge of Vsync output	8'h00
MPNL	CDh	Maximum pixel number	8'h00
MPNH_ MLNH	CEh	Maximum pixel/line number	8'h00
MLNL	CFh	Maximum line number	8'h00
SALNL	D0h	Start line number of active window	8'h00
SALNH_ EALNH	D1h	Start/end line number of active window	8'h00
EALNL	D2h	End line number of active window	8'h00
SAPNL	D3h	Start pixel number of active window	8'h00
SAPNH_ EAPNH	D4h	Start/end pixel number of active window	8'h00
EAPNL	D5h	End pixel number of active window	8'h00
SENINT	D6h	Sensor interrupt	8'h00

SENINT_EN	D7h	Sensor interrupt enable	8'h00
SUB_SAMP	D8h	Sub-sampling mode	8'h00

Notation:

R/W	Read / Write
R/O	Read Only
W/O	Write Only
R/W1C	Read / Write "1" to Clear
R/W/C	Read / Write and hardware automatic Clear

4.2 Registers Descriptions

4.2.1 Global Control Register Part

Offset 00h – GP1_DAT

GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO[7:0] GPIO7~0 data.
0 GPIO7~0O write.
1 GPIO7~0I read.

Offset 01h – GP1_INTPOL …….…… Default value = 8'h00

GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO[7:0] GPIO7~0 interrupt polarity.
0 H2L
1 L2H

Offset 02h – GP1_INTEN …….…… Default value = 8'hFF

GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO[7:0] 0 Unmask int
1 Mask int

Offset 03h – GP1_INT …… Default value = 8'h00

GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C

7-0 GPIO[7:0] GPIO7~0 interrupt indication.

Offset 04h – ROMFLG ……..…… Default value = 8'hFF

ROMFLG7	ROMFLG6	ROMFLG5	ROMFLG4	ROMFLG3	ROMFLG2	ROMFLG1	ROMFLG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 ROMFLG[7:0] Reserved for internal use.

Offset 06h – GP1_OE …….…….……. Default value = 8'h00

GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO[7:0] GPIO7~0 control.
0 Input
1 Output

Offset 07h – GP2_DAT

--	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
--	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -

6-0 GPIO[14:8] GPIO14~8 data.
0 GPIO14~8O write.
1 GPIO14~8I read.

Offset 08h – GP2_INTPOL ……..…… Default value = 8'h00

--	GPIO14	GPIO13	EAPN11	SAPN11	GPIO10	GPIO9	GPIO8
--	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -

6-5 GPIO[14:13] GPIO14~13 interrupt polarity.
0 H2L
1 L2H

4 EAPN11 Pixel number of end active window

3 SAPN11 Pixel number of start active window

2-0 GPIO[10:8] GPIO10~8 interrupt polarity.
0 H2L
1 L2H

Offset 09h – GP2_INTEN ……..…… Default value = 8'hFF

--	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
--	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -

6-0 GPIO[14:8] 0 Unmask int
1 Mask int

Offset 0Ah – GP2_INT …… Default value = 8'h00

--	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
--	W1C	W1C	W1C	W1C	W1C	W1C	W1C

7 RESERVED -

6-0 GPIO[14:8] GPIO14~8 interrupt indication.

Offset 0Dh – GP2_OE …….……. Default value = 8'h00

--	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
--	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -

6-0 GPIO[14:8] GPIO14~8 control.
0 Input
1 Output

Offset 0Eh – GCTL ……..…… Default value = 8'hFC

--	--	--	--	--	SEN_EN	--	SEN_CLKEN
--	--	--	--	--	R/W	--	R/W

7-3 RESERVED -

2 SEN_EN Register enable to sensor interface.
0 Default/Reset state
1 Enable

1 RESERVED -

0 SEN_CLKEN 0 Stop clock to sensor interface
1 Enable clock to sensor interface

Offset 0Fh – INT_MASK ……..…… Default value = 8'h00

--	--	--	--	--	PIE_INTMASK	--	SEN_INTMASK
--	--	--	--	--	R/W	--	R/W

7-3 RESERVED -

2 PIE_INTMASK 0 Mask of SIE_INT
1 Unmask of SIE_INT

1 RESERVED -

0 SEN_INTMASK 0 Mask of SEN_INT
1 Unmask of SEN_INT

Offset 10h – CLKCTL ……..…… Default value = 8'h80

--	--		SEN_CLKCTL4	SEN_CLKCTL3	SEN_CLKCTL2	SEN_CLKCTL1	SEN_CLKCTL0
--	--		R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -

4 SEN_CLKCTL4 Operating clock of sensor interface is 48M

3	**SEN_CLKCTL3**	Operating clock of sensor interface is 7.5M
2	**SEN_CLKCTL2**	Operating clock of sensor interface is 15M
1	**SEN_CLKCTL1**	Operating clock of sensor interface is 30M
0	**SEN_CLKCTL0**	Operating clock of sensor interface is 60M

Offset 11h – CPURST …….……..……. Default value = 8'h00

--	--	--	--	--	--	--	CPU2SEN_RST
--	--	--	--	--	--	--	R/W

7-1	**RESERVED**	-	
0	**CPU2SEN_RST**	0	Unreset
		1	Reset SEN_TOP

4.2.2 USB Register Part

Offset 40h – DEVCTL1 ……..…… Default value = 8'h04

HS_SUSPD	CHIRP_DEN	TSTPKEN	TSTPKRST	--	DISGLUSB	DIS_SUS	PWRDN
R/W/C	R/W	R/W/C	W/O	--	R/W	R/W	R/W/C

7	**HS_SUSPD**	High Speed Suspend This bit can be set/cleared by uC. When chip is in high speed mode and suspends event is detected, uC can set HS_SUS and PWRDN bits to enter suspend mode. This bit will be cleared automatically when end of resume signaling (K to SE0) is detected.
6	**CHIRP_DEN**	Set this bit will enable HS-KJKJKJ chirp detection. After correct HS chirp sequence is detected, CHIRP_DET bit in USBEVT1 will be set.
5	**TSTPKEN**	Enable Endpoint 1 data packet transmission without receiving IN token. This bit is cleared by hardware when TSTPKTX interrupt is set.
4	**TSTPKRST**	Reset Read Pointer of TX FIFO0. Note: Write pointer & FIFO data keep unchanged.
3	**RESERVED**	-
2	**DISGLUSB**	When this bit is set to '1', D+ pin will be left floating so that no connect will be detected on the host side.
1	**DIS_SUS**	Disable suspend detection
0	**PWRDN** `	Power down mode If USB suspend is detected, firmware can set PWRDN to put the controller into power down mode. Power down mode stops oscillator and freezes at known states, and no more command can be executed. Hardware will automatically clear PWRDN upon hardware reset or interrupted event.

Offset 41h – UEVT1 ……..…… Default value = 8'h00

SOF	CHIRP_DET	URST	WAKEUP	RESUME	SUSPD	EP0TX	EP0RX
R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C

7	**SOF**	SOF token packet received event
6	**CHIRP_DET**	Chirp sequence “K-J-K-J-K-J” detected.
5	**SRST**	USB Reset (SE0 for 3ms) is detected. After receiving this event, uC should begin the HS detection handshake.
4	**WAKEUP**	Remote-wakeup event is detected during suspend state
3	**RESUME**	USB resume detected
2	**SUSPD**	USB suspend detected
1	**EP0TX**	Endpoint 0 transmits a data packet completely.
0	**EP0RX**	Endpoint 0 receives a data packet.

Offset 42h – UEVT2 …….…… Default value = 8’h00

SETUP	TSTPKTX	EP2NAK	EP1NAK	EP0NAK	EP3TX	EP2RX	EP1TX
R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C

7	**SETUP**	Device received a setup packet.
6	**TSTPKTX**	Test Packet is sent complete.
5-3	**EPnNAK**	Endpoint receiving or transmitting NAK flag. (n=2~0)
2	**EP3TX**	Endpoint 3 transmission done event
1	**EP2RX**	Endpoint 2 receive done event.
0	**EP1TX**	Endpoint 1 transmission done event.

Offset 43h – UEVT1EN …….…… Default value = 8’h00

SOFEN	CHIRPDEN	URSTEN	WKUPEN	RSMEN	SUSEN	EP0TXEN	EP0RXEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0	These are the interrupt enable bits for USB event interrupt #1 to uC. (Mask bits of USBEVT1)

Offset 44h – UEVT2EN …….…… Default value = 8’h00

SETUPEN	TSTPKTXEN	EP2NAKEN	EP1NAKEN	EP0NAKEN	EP3TXEN	EP2RXEN	EP1TXEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0	These are the interrupt enable bits for USB event interrupt #2 to uC. (Mask bits of USBEVT1)

Offset 45h – UTMCTL …….…… Default value = 8’h0C

VMI	VPI	OPMOD1	OPMOD0	FSPEED	HSTERM	TXVLDH/ RXVLDH	TXVLD/ RXACTV
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W

Write	To generate HS Chirp, set to 8’b0010_0111. To generate FS Remote-Wake-Up, set to 8’b0010_1111.
Read	RXACTV/RXVLDH will reflect the real-time status of the UTM interface.

Offset 46h – UTMDATL

UTMD7	UTMD6	UTMD5	UTMD4	UTMD3	UTMD2	UTMD1	UTMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset 47h – UTMDATH

UTMD15	UTMD14	UTMD13	UTMD12	UTMD11	UTMD10	UTMD9	UTMD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

UTMDATL/UTMDATH are used to set/read data to/from UTM interface.

Write Set the output data on UTM interface.
To issue chirp or remote-wake-up, these 2 registers should set to 4'h0000.

Read Reflect the real-time status of the UTM data bus.

Offset 48h – DEVADR …….…….…… Default value = 8'h00

--	DEVADR6	DEVADR5	DEVADR4	DEVADR3	DEVADR2	DEVADR1	DEVADR0
--	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RESERVED -

6-0 This register is used to store USB device address.

Offset 49h – MISC …….…….…… Default value = 8'h00

SUSPD	ADDR	DEFAULT	POWER	--	--	SF	SUS_DIS
R/O	R/O	R/O	R/O	--	--	R/W	R/W

7 SUSPD Device is in the suspend state.

6 ADDR Device is in the address state.

5 DEFAULT Device is in the default state.

4 POWER Device is in the powered state.

3-2 RESERVED -

1 SF Short frame mode, using in suspend detection.
0 Normal mode, needs 3ms bus idle to enter suspend mode
1 Short frame mode, needs only 200us to enter suspend mode

0 SUS_DIS Disable suspend detection.

Offset 4Ah – EPCTL1 …….…….…… Default value = 8'h00

EP1ISOEN	DISNYET	TATODEN	EP0TEST	BULK_RST	EP3EN	EP2EN	EP1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 EP1ISOEN 0 Endpoint 1 is BULK IN mode.
1 Endpoint 1 is ISO IN mode.

6 DISNYET Disable USB NYET response, instead of ACK response.

5 TATODEN Turn around time out detect enable.

4 EP0TEST 0 Normal mode, Endpoint 0 doesn't response to bulk IN/OUT packet.

1 Test mode, Endpoint 0 can response all packet.

3 BULK_RST EP1 bulk mode initial reset

2-0 EPnEN Endpoint 1, 2, 3 TX/RX enable. (n=3~1)
After device is configured, EPTX1EN, EPTX2EN,EP3TXEN, EPRX1EN, EPRX2EN,EP3RXEN write 1 to decide Endpoint 1,2,3 IN or OUT. Before endpoint is enabled, it won't response to any USB transaction.

Offset 4Bh – EPCTL2 …….……. Default value = 8'h00

--	EP3TGRST	EP2TGRST	EP1TGRST	--	EP3STL	EP2STL	EP1STL
--	W/O	W/O	W/O	--	R/W	R/W	R/W

7 RESERVED -

6-4 EPnTGRST Endpoint toggle reset. (n=3~1)

3 RESERVED -

2-0 EPnSTL Endpoint stall. (n=3~1)

Offset 4Ch – EPCTL3 …….……. Default value = 8'h00

EP3TOG	EP2TOG	EP1TOG	TX3FFPOP	FF3RST	RX0FFPSH	TX0FFPOP	FF0RST
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W

7-5 EPnTOG Toggle indication of DATA packet. (n=3~1)

4 TX3FFPOP uC pop endpoint 3 TXFIFO enable.

3 FF3RST Reset endpoint 3 FIFO read/write pointer. Data in FIFO remain unchanged.

2 RX0FFPSH uC push endpoint 0 RXFIFO enable

1 TX0FFPOP uC pop endpoint 0 TXFIFO enable.

0 FF0RST Reset endpoint 0 TXFIFO read/write pointer. Data in FIFO remain unchanged.

Offset 4Dh – EPCTL3 …….……. Default value = 8'h00

RX0DIS	RXSETUP	RXOUT	RXSEQ	EP0RXSTL	EP0TXSTL	TX0OE	TX0SEQ
R/W	R/O	R/O	R/W	R/W	R/W	R/W/C	R/W

7 RX0DIS Disable receiving capability on endpoint 0

Upon successfully receiving a data packet on endpoint 0, hardware will automatically set this bit to '1'. At this time, no more OUT data on endpoint 0 can be accepted, hardware will respond with NAK. Note, for SETUP transaction, hardware will always accept and respond with ACK.

0 Endp0 FIFO is available for data receiving.

1 Endp0 FIFO is not available

6 RXSETUP Endpoint 0 received token is SETUP.

5 RXOUT Endpoint 0 received token is OUT.

4 RXSEQ Endpoint 0 received data toggle.

0 The received data is DATA0

1 The received data is DATA1

3 EP0RXSTL Endpoint 0 receiving stall.

Endpoint 0 will respond with a STALL to a valid OUT transaction. This bit will

be cleared by SETUP transaction automatically.

2 EP0TXSTL Endpoint 0 transmitting stall.
Endpoint 0 will respond with a STALL to a valid IN transaction. This bit will be cleared by SETUP transaction automatically.

1 TX0OE Ready to transmit control data.

0 TX0SEQ Endpoint 0 transmission data toggle.
0 TX DATA0
1 TX DATA1

Offset 4Eh – RX0CNT ……..…… Default value = 8'h00

CTLRD	RX0CNT6	RX0CNT5	RX0CNT4	RX0CNT3	RX0CNT2	RX0CNT1	RX0CNT0
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O

7 CTLRD Control pipe(Endpoint 0) control to prevent response of bulk packet.
0 Host send OUT packet right after SETUP package. (Has a IN packet status)
1 Host send IN packet right after SETUP package. (Has a OUT packet status)

6-0 RX0CNT[6:0] The received DATA length of endpoint 0.

Offset 4Fh – FF0BUF ……..…… Default value = 8'h00

FF0DAT7	FF0DAT6	FF0DAT5	FF0DAT4	FF0DAT3	FF0DAT2	FF0DAT1	FF0DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FF0DAT[7:0] Data entry for endpoint 0 FIFO.
Writing this register will push data into endpoint 0 TXFIFO, and reading will pop data from endpoint 0 RXFIFO.

Offset 50h – FF1BUF ……..…… Default value = 8'h00

FF1DAT7	FF1DAT6	FF1DAT5	FF1DAT4	FF1DAT3	FF1DAT2	FF1DAT1	FF1DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FF1DAT[7:0] Data entry for endpoint 1 FIFO.
Writing this register will push data into endpoint 1 TXFIFO, and reading will pop data from endpoint 1 RXFIFO.

Offset 51h – FF2BUF ……..…… Default value = 8'h00

FF2DAT7	FF2DAT6	FF2DAT5	FF2DAT4	FF2DAT3	FF2DAT2	FF2DAT1	FF2DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FF2DAT[7:0] Data entry for endpoint 2 FIFO.
Writing this register will push data into endpoint 2 TXFIFO, and reading will pop data from endpoint 2 RXFIFO.

Offset 52h – FF3BUF …….…… Default value = 8'h00

FF3DAT7	FF3DAT6	FF3DAT5	FF3DAT4	FF3DAT3	FF3DAT2	FF3DAT1	FF3DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FF3DAT[7:0] Data entry for endpoint 3 FIFO.
Writing this register will push data into endpoint 3 TXFIFO, and reading will pop data from endpoint 3 RXFIFO.

Offset 53h – EP12CTL1 ……..…… Default value = 8'h00

--	--	--	--	--	TXASEL2	TXASEL1	TXASEL0
--	--	--	--	--	R/W	R/W	R/W

7-3 RESERVED -

2-0 TXASEL[2:0]
001 TXAFFSEL1 set 1
010 TXAFFSEL2 set 1
011 TXAFFSEL3 set 1
100 TXAFFSEL4 set 1
101 TXAFFSEL5 set 1
110 TXAFFSEL0 set 1

In normal operation, bulk FIFO is pushed/popped by DTV/SEN engine or USB SIE engine. But use the register, we can push/pop bulk FIFO by uC.

uC accessing ISO/Bulk IN FIFO:
Set TXFFPSH=1, and use TXAFFSEL to select DATA A FIFO, or use TXBFFSEL to select DATA B FIFO. Then write data to FF1BUF to begin pushing FIFO.
To pop data from FIFO, just set TXFFPSH = 0, set TXBFFSEL or TXAFFSEL to select DATA A/DATA B FIFO, and read data from FF1BUF to begin popping FIFO.
After pop/push is complete, uC must clear all FIFO select and control setting on FFCTL.

Offset 54h – EP12CTL2 ……..…… Default value = 8'h00

--	--	DTXEN	TXFMOD	TXFFRST	RXFFRST	TXFFPSH	RXFFPSH
--	--	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -
5 DTXEN Firmware set ENDP1 TX mode.
4 TXFMOD Firmware test EP1 FIFO, read/write byte mode.
3 TXFFRST Reset TXFIFO, cleared by hardware itself.
2 RXFFRST Reset RXFIFO, cleared by hardware itself.
1 TXFFPSH Push indication for TX FIFO
0 RXFFPSH Push indication for RX FIFO

Offset 55h – EP12CTL2 ……..…… Default value = 8'h00

ANK1_EN	--	--	--	--	ANAKEP2	EP2NAK	EP1NAK
R/W	--	--	--	--	R/W	R/W	R/W

7 ANK1_EN Force NAK of endpoint 1.

6-3	**RESERVED**	-
2	**ANAKEP2**	Automatic NAK of endpoint 2, after receiving a data packet. (Bit FNAKEP2 would be set to 1, after receiving a data packet.).
1	**EP2NAL**	Force NAK of endpoint 2.
0	**EP1NAK**	Force NAK of endpoint 1.

Offset 56h – EP3CTL ……..…….…… Default value = 8'h00

TXOE3	TX3CNT6	TX3CNT5	TX3CNT4	TX3CNT3	TX3CNT2	TX3CNT1	TX3CNT0
R/W/C	R/O	R/O	R/O	R/O	R/O	R/O	R/O

7	**TXOE3**	Ready to transmit endpoint 3 data
6-0	**TX3CNT[6:0]**	The transmit DATA length of endpoint 3

Offset 57h – RX2CNT ……..…….…… Default value = 8'h00

RX2DIS	RX2CNT6	RX2CNT5	RX2CNT4	RX2CNT3	RX2CNT2	RX2CNT1	RX2CNT0
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O

7	**RX2DIS**	Disable receiving capability on endpoint 2 Upon successfully receiving a data packet on endpoint 2, hardware will automatically set this bit to '1'. At this time, no more OUT data on endpoint 2 can be accepted, hardware will respond with NAK. 0 Endp2 FIFO is available for data receiving. 1 Endp2 FIFO is not available
6-0	**RX2CNT[6:0]**	The received DATA length of endpoint 2

Offset 5Fh – WAKEN ……..…….…… Default value = 8'h00

--	RAMDIS3	RAMDIS2	RAMDIS1	--	GP4EN	GP3EN	GP2EN
--	R/W	R/W	R/W	--	R/W	R/W	R/W

Enable falling edge event on corresponding pins as remote wakeup source.

7	**RESERVED**	-
6	**RAMDIS3**	Endp3 RAM disable.
5	**RAMDIS2**	Endp2 RAM disable.
4	**RAMDIS1**	Endp1 RAM disable.
3	**RESERVED**	-
2	**GP4EN**	Falling edge event on GPIO4 wakeup enable.
1	**GP3EN**	Falling edge event on GPIO3 wakeup enable.
0	**GP2EN**	Falling edge event on GPIO2 wakeup enable

Offset 60h – HEADCTL1 ……..…….…… Default value = 8'h00

--	--	--	--	--	--	FRAM_EN	HEAD_EN
--	--	--	--	--	--	R/W	R/W

7-2 RESERVED -
1 FRAM_EN Set 1 to enable, header function..
0 HEAD_EN Set 1 to add Header for each frame, Set 0 to add Header for each SOF.

Offset 61h – HEADCTL2 ……..…….…… Default value = 8'h00

--	--	--	--	HEADCNT0	HEADCNT0	HEADCNT0	HEADCNT0
--	--	--	--	R/W	R/W	R/W	R/W

7-4 RESERVED -
3-0 HEADCNT[3:0] Select header byte count from 0~8.

Offset 62h – HEAD0 ……..…… Default value = 8'h00

H0DAT7	H0DAT6	H0DAT5	H0DAT4	H0DAT3	H0DAT2	H0DAT1	H0DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 H0DAT[7:0] Head data 0.

Offset 63h – HEAD1 ……..…… Default value = 8'h00

H1DAT7	H1DAT6	H1DAT5	H1DAT4	H1DAT3	H1DAT2	H1DAT1	H1DAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 H1DAT[7:0] Head data 1.

4.2.3 Sensor Register Part

Offset C0h – SENCTL ……..……..…… Default value = 8'h00

INCTST	EDGESEL	CLKOE	VSATV	HSATV	HVOE	--	BITMODE
R/W	R/W	R/W	R/W	R/W	R/W	--	R/W

7 INCTST
0 No incremental data on CMSDAT[9:0]
1 Incremental data on CMSDAT[9:0] for debugging

6 EDGESEL Rising/Falling edge of PIX_CLK selection
0 The same with the PIX_CLK
1 Inverse with the PIX_CLK

5 CLKOE MAS_CLK output selection
0 Input clock (PIX_CLK)
1 Output clock (MAS_CLK)

4 VSATV Select of timing to reset internal line count when VSYNC is coming from sensor.
0 Falling edge
1 Rising edge

3 HSATV Select of timing to reset internal pixel count when HSYNC is coming from sensor.
0 Falling edge
1 Rising edge

2 HVOE HSYNC/VSYNC output enable

0 Output
1 Input

1 RESERVED -

0 BITMODE Pixel data bit number.
0 8bit pixel date
1 10bit pixel date (In this mode, 10 bit data will be transferred to USB by continuous two byte. The first byte is MSB 8 bit, and the next byte is LSB2 bit and 6'b0.)

Offset C1h – MCK_SAMP ……..…… Default value = 8'h03

SAMP4	SAMP3	SAMP2	SAMP1	SAMP0	MCK2	MCK1	MCK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-3 SAMP[4:0] Sampling phase of data bus.

2-0 MCK[2:0] Selection of master clock to sensor (MCLK)
000 MCLK is 60MHz
001 MCLK is 30MHz
010 MCLK is 20MHz
011 MCLK is 15MHz
100 MCLK is 12MHz
101 MCLK is 10MHz
110 MCLK is 8.57MHz
111 MCLK is 7.5MHz

Address	0x10	0xC1	CLOCK
Data	0x01	0x00	60MHz
		0x01	30
		0x02	20
		0x03	15
		0x04	12
		0x05	10
		0x06	8.57
		0x07	7.5

Address	0x10	0xC1	CLOCK
Data	0x02	0x00	30MHz
		0x01	15
		0x02	10
		0x03	7.5
		0x04	6
		0x05	5

		0x06	4.2857
		0x07	3.75

Address	0x10	0xC1	CLOCK
Data	0x04	0x00	15MHz
		0x01	7.5
		0x02	5
		0x03	3.75
		0x04	3
		0x05	2.5
		0x06	2.1429
		0x07	1.875

Address	0x10	0xC1	CLOCK
Data	0x08	0x00	7.5MHz
		0x01	3.75
		0x02	2.5
		0x03	1.875
		0x04	1.5
		0x05	1.25
		0x06	1.0714
		0x07	0.9375

Address	0x10	0xC1	CLOCK
Data	0x10	0x00	48MHz
		0x01	24
		0x02	16
		0x03	12
		0x04	9.6
		0x05	8
		0x06	6.8571
		0x07	6

Offset C2h – CLKRG_CLK …….…… Default value = 8'h00

--	--	CLKFG2	CLKFG1	CLKFG0	CLKRG2	CLKRG1	CLKRG0
--	--	R/W	R/W	R/W	R/W	R/W	R/W

5-3 CLKFG[2:0] Falling edge of MCLK.
2-0 CLKRG[2:0] Rising edge of MCLK.

Offset C3h – HV_CC …….…… Default value = 8'h00

--	--	VCC2	VCC1	VCC0	HCC2	HCC1	HCC0
--	--	R/W	R/W	R/W	R/W	R/W	R/W

5-3 VCC[2:0] Phase of output VSYNC.
2-0 HCC[2:0] Phase of output HSYNC.

Offset C4h – RHNL …….……..…… Default value = 8'h00

RHN7	RHN6	RHN5	RHN4	RHN3	RHN2	RHN1	RHN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset C5h – RHNH_FHNH …….……..…… Default value = 8'h00

--	--	FHN10	FHN9	FHN8	RHN10	RHN9	RHN8
--	--	R/W	R/W	R/W	R/W	R/W	R/W

RHN[10:0] Pixel number of the rising edge of HSYNC

Offset C6h – FHNL …….……..……..…… Default value = 8'h00

FHN7	FHN6	FHN5	FHN4	FHN3	FHN2	FHN1	FHN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FHN[10:0] Pixel number of falling edge of HSYNC

Offset C7h – RVPNL …….……..……..…… Default value = 8'h00

RVPN7	RVPN6	RVPN5	RVPN4	RVPN3	RVPN2	RVPN1	RVPN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset C8h – RVPNH_RVI …….…….. Default value = 8'h00

--	--	RVLN10	RVLN9	RVLN8	RVPN10	RVPN9	RVPN8
--	--	R/W	R/W	R/W	R/W	R/W	R/W

RVPN[10:0] Number of the rising pixel number

Offset C9h – RVLNL ……..……..…….. Default value = 8'h00

RVLN7	RVLN6	RVLN5	RVLN4	RVLN3	RVLN2	RVLN1	RVLN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RVLN[10:0] Line number for Rising edge of VSYNC line number

Offset CAh – FVPNL ……..…….. Default value = 8'h00

FVPN7	FVPN6	FVPN5	FVPN4	FVPN3	FVPN2	FVPN1	FVPN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset CBh – FVPNH_FVLNH ……..…….. Default value = 8'h00

--	--	FVLN10	FVLN9	FVLN8	FVPN10	FVPN9	FVPN8
--	--	R/W	R/W	R/W	R/W	R/W	R/W

FVPN[10:0] Pixel number for falling edge of VSYNC

Offset CCh – FVLNL ……..……..……..…….. Default value = 8'h00

FVLN7	FVLN6	FVLN5	FVLN4	FVLN3	FVLN2	FVLN1	FVLN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FVLN[7:0] Line number for falling edge of VSYNC

Offset CDh – MPNL ……..…….. Default value = 8'h00

MPN7	MPN6	MPN5	MPN4	MPN3	MPN2	MPN1	MPN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset CEh – MPNH_MLNH ……..……..……..…….. Default value = 8'h00

--	--	MLN10	MLN9	MLN8	MPN10	MPN9	MPN8
--	--	R/W	R/W	R/W	R/W	R/W	R/W

MPN[10:0] Pixel number for maximum window
MLN[10:0] Line number for maximum window

Offset CFh – MLNL …….……..……..……..…… Default value = 8'h00

MLN7	MLN6	MLN5	MLN4	MLN3	MLN2	MLN1	MLN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset D0h – SALNL ……..……..…… Default value = 8'h00

SALN7	SALN6	SALN5	SALN4	SALN3	SALN2	SALN1	SALN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SALN[10:0] Line number of start active window
EALN[10:0] Line number of end active window

Offset D1h – SALNH_EALNH ……..……..…… Default value = 8'h00

--	--	EALN10	EALN9	EALN8	SALN10	SALN9	SALN8
--	--	R/W	R/W	R/W	R/W	R/W	R/W

Offset D2h – EALNL ……..……..……..……..…… Default value = 8'h00

EALN7	EALN6	EALN5	EALN4	EALN3	EALN2	EALN1	EALN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset D3h – SAPNL ……..…..……..…… Default value = 8'h00

SAPN7	SAPN6	SAPN5	SAPN4	SAPN3	SAPN2	SAPN1	SAPN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SAPN[10:0] Pixel number of start active window
EAPN[10:0] Pixel number of end active window

Offset D4h – SAPNH_EAPNH ……..……..…… Default value = 8'h00

--	--	EAPN10	EAPN9	EAPN8	SAPN10	SAPN9	SAPN8
--	--	R/W	R/W	R/W	R/W	R/W	R/W

Offset D5h – EAPNL ……..……..……..……..…… Default value = 8'h00

EAPN7	EAPN6	EAPN5	EAPN4	EAPN3	EAPN2	EAPN1	EAPN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Offset D6h – SENINT ……..……...……..……..…… Default value = 8'h00

--	--	--	--	--	--	--	EOFINT
--	--	--	--	--	--	--	R/W1C

7-1 RESERVED -

0 EOFINT EOF (end of frame)
Indicate EOF

Offset D7h – SENINT_EN ……..……...……..……..…… Default value = 8'h00

--	--	--	--	--	--	--	EOFINT_EN
--	--	--	--	--	--	--	R/W1C

7-1 RESERVED -

0 EOFINT_EN 0 Disable EOFINT
1 Enable EOFINT

Offset D8h – SUB_SAMP ……..……...……..……..…… Default value = 8'h00

--	--	PSH_MODE	PSH_MODE	PCLK_CNT1	PCLK_CNT0	SUB_SAMP4	SUB_SAMP2
--	--	R/W	R/W	R/W	R/W	R/W	R/W

6-7 RESERVED -

5-**4 PSH_MODE[1:0]** "2" SEN2FF_PSH will separate 2 SEN_CLK60
"1" SEN2FF_PSH will separate 1 SEN_CLK60
"0" SEN2FF_PSH will continue

3-2 PCLK_CNT[1:0] 00 Incoming sensor data rate is the same as MCLK
01 Incoming sensor data rate is 1/2 times of MCLK
10 Incoming sensor data rate is 1/3 times of MCLK
11 Incoming sensor data rate is 1/4 times of MCLK

1 SUB_SAMP4 0 Unchanged
1 Frame size will reduce to 1/16. Pixel number which are sampled on horizontal and vertical direction separately reduce to 1/4 times. For example, a 640x480 image will be 160x120 if this bit is set.

0 SUB_SAMP2 0 Unchanged
1 Frame size will reduce to 1/4. Pixel number which are sampled on horizontal and vertical direction separately reduce to 1/2 times. For example, a 320x240 image will be 160x120 if this bit is set.

CHAPTER 5 FUNCTIONAL DESCRIPTION

5.1 Function Block

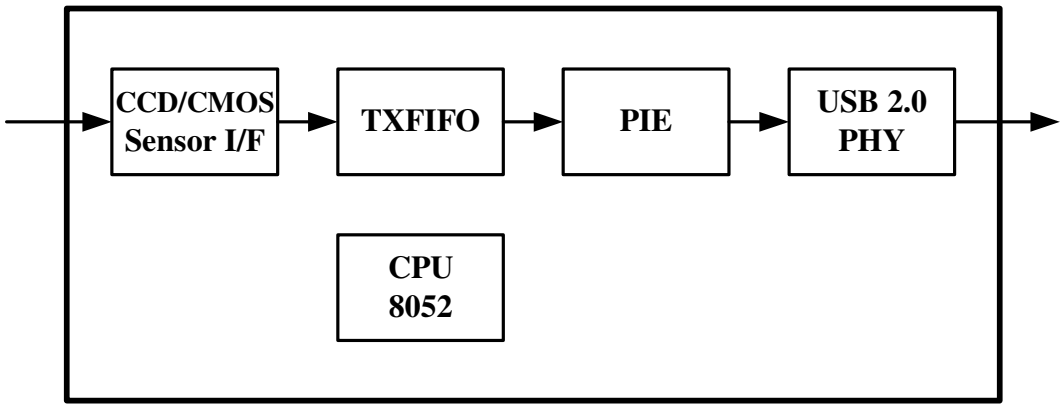


Figure 5.1 - Block Diagram

- **CCD Module/CMOS Sensor Interface**

  GL860A can link with popular CMOS sensor on market for PC camera application. GL860A can be configured by different sensor requirement. If sensor is acting as master, GL860A can accept HSYNC/VSYNC from sensor. If GL860A is configured as a master HSYNC/VSYNC will be provided by GL860A to sensor. GL860A keep the most flexibility to fit most of the sensors. The detail of configuration needs to refer to GL860A Application Note. For most sensors no matter of YUV format or RGB format, they can be easily transferred image data to PC by GL860A.

- **TXFIFO**

  GL860A build in 6K byte internal buffer for USB high bandwidth application. This 6K internal buffer can be used as transmitted buffer of isochronous pipe or bulk pipe. In USB specification, the highest bandwidth of isochronous pipe is 24M byte/second, that can be easily derived to maximum frame rate depending on configuration. For example, frame rate can be easily achieved to 30 frames per second if image size is 640 x 480 if raw data output and sensor clock is 15M.

- **PIE**

  PIE handles the USB protocol defined in chapter 8 of *USB specification Revision 2.0*. It co-works with CPU to play the role of the chip's kernel. The main functions of PIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB1.1, bit stuffing/de-stuffing is implemented in UTMI, not in PIE.

- **USB 2.0 PHY (UTMI)**

  UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB2.0 test modes, and serial/parallel conversion.

- **CPU**

  CPU is the micro-processor unit of GL860A. It is an 8-bit 8052 processor with 8K ROM and 256 bytes RAM. It operates at 15Mhz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, μC can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of chip. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, and PID/VID setting.

5.2 Operation Mode

For customized firmware, flash memory can use as external program memory of CPU. This is for customer to develop their firmware. This is only available for 100-pin package type.

5.2.1 with Flash Memory

- Only available in 100-pin QFP package
- Force EXTCPU = 0
- GPIO9 pull down
- GPIO13/GPIO14 used as serial bus to configure sensor

5.2.2 without Flash Memory

- If 100 pin, set EXTCPU = 0
- GPIO9 pull down
- GPIO13/GPIO14 are used as serial bus to configure sensor

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

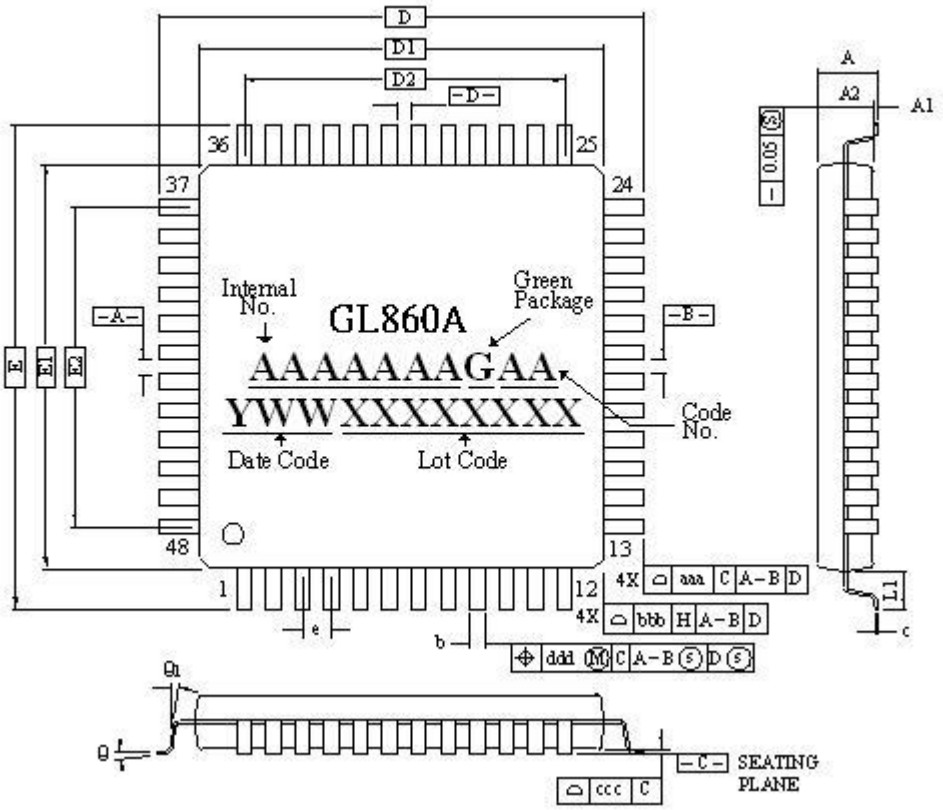
Symbol	Parameter	Min.	Max.	Unit
V_{IN}	3.3V Input Voltage	3.0	3.6	V
T_A	Ambient Temperature under bias	0	+100	°C
F_{OSC}	Frequency	12 MHz ± 500ppm		

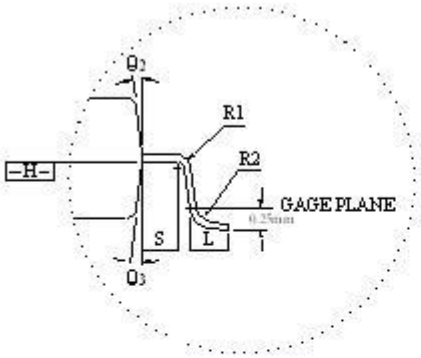
6.2 DC Characteristics

Table 6.2 - DC Characteristics Except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_D	Power Dissipation	-	-	-	mA
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-	-	0.9	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.36	1.48	1.62	V
V_{THL}	HIGH to LOW threshold voltage	1.36	1.48	1.62	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	-	µA
R_{DN}	Pad internal pull down resister	-	-	-	Ω
R_{UP}	Pad internal pull up resister	-	-	-	Ω

CHAPTER 7 PACKAGE DIMENSION





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 7.1 - GL860A 48 Pin LQFP Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.61 (24)	0.66 (26)	0.70 (28)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.13 (5) REF		
b	0.18 (7)	0.25 (10)	0.30 (12)
D	7.00 (276) BSC		
E	7.00 (276) BSC		
D2	5.10 (201)	5.20 (205)	5.30 (209)
E2	5.10 (201)	5.20 (205)	5.30 (209)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	0.08 (3)	---
k	0.20 (8)	---	---

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

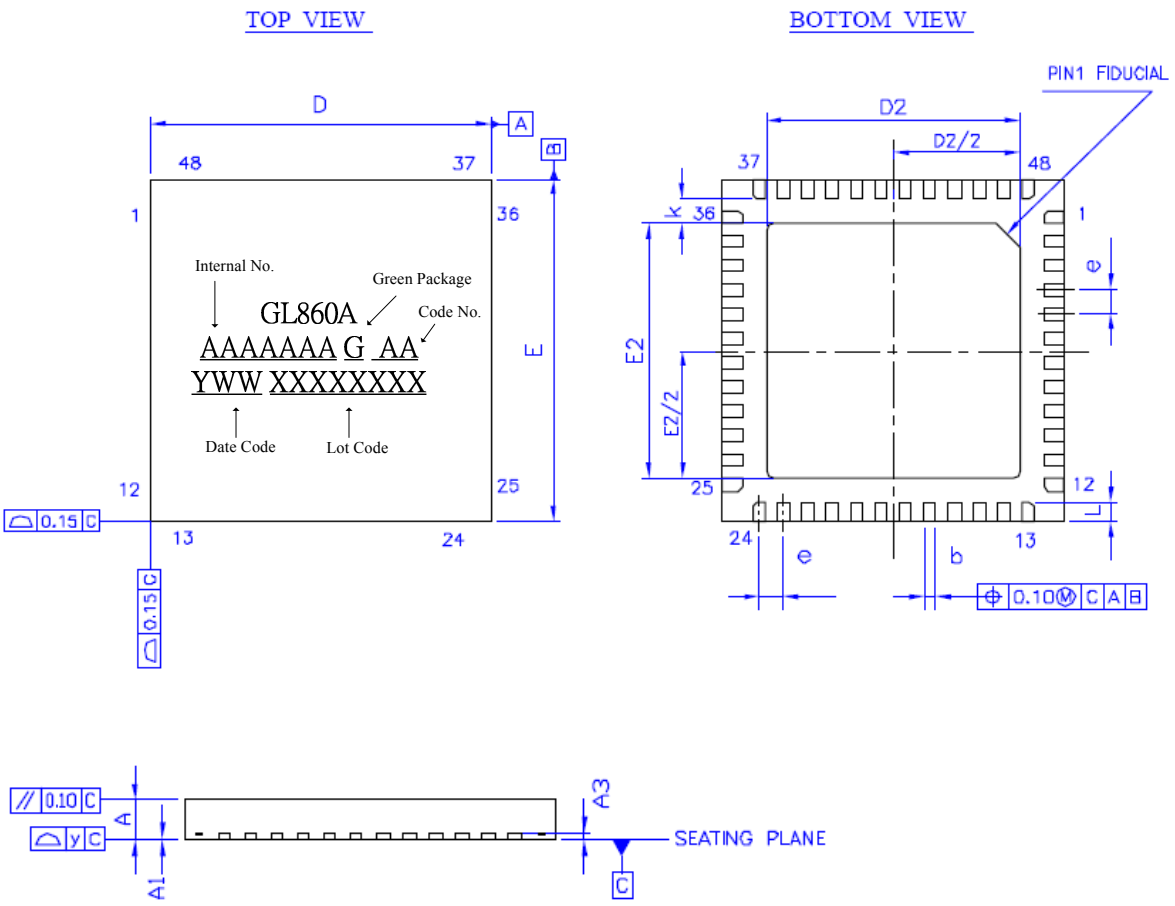


Figure 7.2 - GL860A 48 Pin LQFN Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.61 (24)	0.66 (26)	0.70 (28)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.13 (5) REF		
b	0.13 (5)	0.20 (8)	0.25 (10)
D	6.40 (252)	6.50 (256)	6.60 (260)
E	4.40 (173)	4.50 (177)	4.60 (181)
D2	5.00 (197)	5.10 (201)	5.20 (205)
E2	3.00 (118)	3.10 (122)	3.20 (126)
e	0.40 (16) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	0.08 (3)	---
k	0.30 (12)	---	---

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

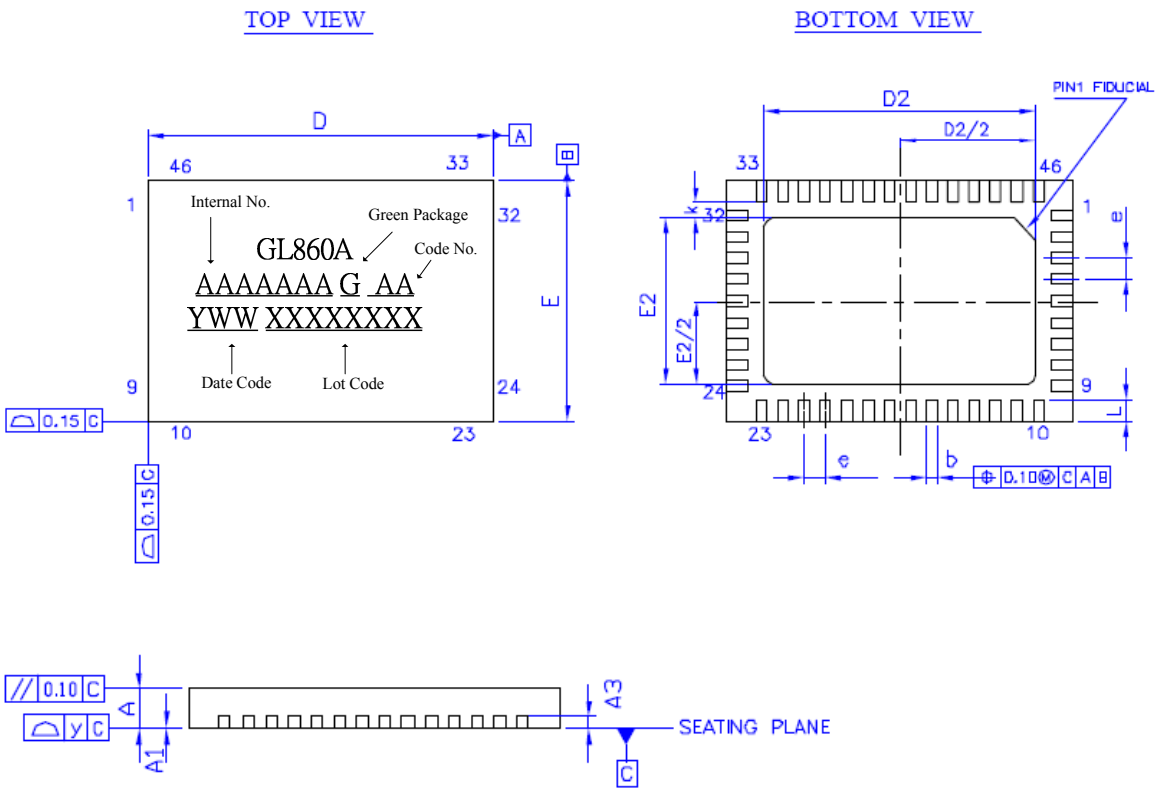


Figure 7.3 - GL860A 46 Pin LQFN Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green	Version	Status
GL860A-MNGXX	48-pin LQFP	Green Package	XX	Available
GL860A-PNGXX	48-pin LQFN	Green Package	XX	Available
GL860A-PMGXX	46-pin LQFN	Green Package	XX	Available

Appendix A. Application circuit

The schematic below represents a very basic example to the controller and is subject to variations depending on application intentions.